CLAIMS

What is claimed is:

1. A UWB receiver comprising:

an antenna for receiving wireless signals coupled to a signal processing circuit; and

the signal processing circuit comprising:

an RF front end circuit comprising:

a first amplifier coupled to the antenna;

a first filter coupled to the output of the first amplifier; and

a mixer coupled to the output of the first filter and receiving a clock signal;

first and second intermediate frequency processing circuits each coupled to one of an in phase output port and a quadrature output port of the mixer;

a summation circuit coupled to outputs of first squaring circuits within the first and second intermediate frequency processing circuits; and

a third intermediate frequency processing circuit coupled to the output of the summation circuit; wherein

the third intermediate frequency processing circuit comprises:

a third amplifier receiving the output of the summation circuit;

a third filter coupled to the output of the third amplifier;

a second squaring circuit coupled to the third filter; and

an integration circuit coupled to the output of the second squaring circuit.

2. The UWB receiver according to claim 1, wherein

each intermediate frequency processing circuit comprises:

a second amplifier receiving a down converted signal from the mixer;

a second filter coupled to the output of the second amplifier; and

a first squaring circuit for squaring a signal filtered by the second filter.

3. A UWB receiver comprising:

an antenna for receiving wireless signals coupled to a signal processing circuit; and

the signal processing circuit comprising:

an RF front end circuit comprising:

a first amplifier coupled to the antenna;

a first filter coupled to the output of the first amplifier; and

a mixer coupled to the output of the first filter and receiving a clock signal;

a first intermediate frequency processing circuit coupled to an in phase output port of the mixer;

a second intermediate frequency processing circuits coupled to the quadrature output port of the mixer;

a third intermediate frequency processing circuit coupled to the output of first intermediate frequency processing circuit; and

a fourth intermediate frequency processing circuit coupled to the output of the second intermediate frequency processing circuit; wherein

each of the third and fourth intermediate frequency processing circuits comprises:

a third amplifier receiving the output of the summation circuit;

a third filter coupled to the output of the third amplifier;

a second squaring circuit coupled to the third filter; and

an integration circuit coupled to the output of the second squaring circuit.

4. The UWB receiver according to claim 3, wherein

each of the first and second intermediate frequency processing circuits comprises:

a second amplifier receiving a down converted signal from the mixer;

a second filter coupled to the output of the second amplifier; and

a first squaring circuit for squaring a signal filtered by the second filter.

5. The UWB receiver according to claim 3, further comprising

a first analog-to-digital converter (ADC) coupled to the output of the third intermediate frequency processing circuit; and

a second ADC coupled to the output of the fourth intermediate frequency processing circuit.