

DEVICE COMPRISING A PLURALITY OF STATIC RANDOM-ACCESS MEMORY CELLS AND METHOD OF OPERATION THEREOF

FIELD OF THE PRESENT DISCLOSURE

Generally, the present disclosure relates to the field of integrated circuits, and more particularly to integrated circuits comprising static random-access memory devices.

DESCRIPTION OF THE PRIOR ART

Types of semiconductor memory include dynamic random-access memory (DRAM) and static random-access memory (SRAM). DRAM comprises memory cells having a relatively simple structure, in particular memory cells wherein an amount of charge stored in a capacity is used to represent a bit of information. Due to the simple structure of DRAM cells, a high density of integration can be obtained. However, due to leakage currents in the capacities, DRAM typically requires constant refresh cycles to avoid a loss of information.

In SRAM devices, cross-coupled inverters are used for storing information. In SRAM devices, refresh cycles need not be performed, and they typically allow a greater speed of operation than DRAM devices. However, SRAM comprises memory cells which typically have a more complex structure than the memory cells of DRAM devices, which may limit the density of integration that can be obtained in SRAM devices.

An SRAM device 100 will be described with reference to Fig. 1.

The SRAM device 100 comprises an SRAM cell 101, a bit line 102, an inverse bitline 103, a wordline 104, a high voltage power supply line 105 and a low voltage power supply line 106.

In the operation of the device 100, the high voltage power supply line 105 can be maintained at a higher voltage than the low voltage power supply line 106. Accordingly, the voltage of the high voltage power supply line 105 will be denoted as "high voltage" and the voltage of the low voltage power supply line 106 will be denoted as "low voltage", although the high voltage is typically on an order of magnitude of a few volts.

The SRAM cell 101 comprises a first inverter 107 having an input 113 and an output 111, and a second inverter 108 having an input 114 and output 112. The output 111 of the first inverter 107 is electrically connected to the input 114 of the second inverter 108, and

the output 112 of the second inverter 108 is electrically connected to the input 113 of the first inverter 107.

Each of the inverters 107, 108 comprises a pull-up transistor, wherein the pull-up transistor of the first inverter 107 is denoted by reference numeral 115, and the pull-up transistor of the second inverter 108 is denoted by reference numeral 116. Moreover, each of the inverters 107, 108 comprises a pull-down transistor, wherein reference numeral 117 denotes the pull-down transistor of the first inverter 107, and reference numeral 118 denotes the pull-down transistor of the second inverter 108.

The pull-up transistors 115, 116 can be p-channel transistors, which can be switched from an on state, wherein they have a relatively high conductivity to an off state, wherein there is only a relatively low leakage conductivity by applying the high voltage to their gate electrodes. The pull-down transistors 117, 118 can be n-channel transistors which can be switched from an off state wherein there is only a relatively low leakage conductivity to an on state wherein they have a relatively high conductivity by applying the high voltage to their gate electrodes.

The SRAM cell 101 further comprises pass-gate transistors 109, 110. The pass-gate transistor 109 is electrically connected between the inverse bitline 103 and the output 111 of the first inverter, and the second pass-gate transistor 110 is electrically connected between the bitline 102 and the output 112 of the second inverter 108. Gate electrodes of the pass-gate transistors 109, 110 are electrically connected to the wordline 104. The pass-gate transistors 109, 110 can be n-channel transistors which can be switched from an off state to an on state by applying the high voltage to their gate electrodes. Accordingly, if the high voltage is applied to the wordline 104, an electrical connection is established between the inverse bitline 103 and the output 111 of the first inverter, and between the bitline 102 and the output 112 of the second inverter 108.

The device 100 can comprise a plurality of SRAM cells having a structure corresponding to the structure of SRAM cell 101, and can also comprise a plurality of low voltage power supply lines similar to power supply lines 105, 106, a plurality of wordlines similar to wordline 104, and a plurality of bitlines and inverse bitlines similar to bitline 102 and inverse bitline 103. Typically, there is an array of SRAM cells having rows and columns of SRAM cells, wherein the power supply lines and wordlines extend along the rows of the array, and the bitlines and inverse bitlines extend along the columns of the array. Individual SRAM cells of the device 100 can be addressed by applying the high voltage to the wordline to which the SRAM cell is connected to switch the pass-gate transistors

of the respective cell into the on state and by applying and/or reading voltages from the bitline and the inverse bitline to which the SRAM cell is connected. The other wordlines can be maintained at the low voltage. Bitlines and inverse bitlines are typically kept at the high voltage during standby mode and are left electrically floating during reading.

The SRAM cell 101 can have three modes of operation. In a standby mode, the voltage of wordline 104 is low, so that pass-gate transistors 109, 110 are in the off state and the inverters 107, 108 are electrically disconnected from bitline 102 and inverse bitline 103. Since the output 111 of the first inverter 107 is electrically connected to the input 114 of the second inverter 108, and the output 112 of the second inverter 108 is electrically connected to the input 113 of the first inverter 107, the inverters 107, 108 can reinforce each other, so that they substantially maintain their respective state. Accordingly, there is a first state of the SRAM cell 101, wherein the output 111 of the first inverter 107 is substantially at the low voltage and the output 112 of the second inverter 108 is substantially at a the high voltage, and a second state, wherein the output 111 of the first inverter 107 is substantially at the high voltage, and the output 112 of the second inverter 108 is substantially at the low voltage. These two states can be used to store one bit of information.

For reading the bit of information stored in the SRAM cell 101, the bitline 102 and the inverse bitline 103 can be pre-charged to the high voltage. Then, the bitline 102 and the inverse bitline 103 are left electrically floating and the wordline 104 is switched from low voltage to high voltage, so that the pass-gate transistors 109, 110 establish an electrical connection between the bitline 102 and the output 112 of the second inverter 108, and an electrical connection between the inverse bitline 103 and the output 111 of the first inverter 107. Depending on the state of the SRAM cell 101, a voltage difference between the bitline 102 and the inverse bitline 103 is created, which can be sensed by a sense amplifier (not shown) to determine the state of SRAM cell 101.

An issue in reading data from SRAM cell 101 can be avoiding the occurrence of a read disturbance wherein the state of the SRAM cell 101 is inadvertently flipped during the read operation. The stability of the SRAM cell 101 with respect to a read disturbance can be dependent on the so-called beta ratio between the conductivity of pull-down transistors 117, 118 in the on state and the conductivity of pass-gate transistors 109, 110 in the on state. A greater beta ratio can be helpful for increasing the stability of SRAM cell 101 with respect to read disturbances. Since the conductivity of a channel of a field effect transistor in the on state typically increases with an increasing width of the channel

of the transistor, from the point of view of stability during the read operation, it can be of advantage if a width of the channel regions of the pass-gate transistors 109, 110 is relatively low compared to a width of the channel regions of the pull-down transistors 117, 118.

For writing data to the SRAM cell 101, the high voltage can be applied to one of the bitline 102 and the inverse bitline 103, and the low voltage can be applied to the other one of the bitline 102 and the inverse bitline 103, depending on the state of the SRAM cell 101 to be obtained after the write operation. Thereafter, the voltage of the wordline 104 can be switched from low to high to switch the pass-gate transistors 109, 110 into the on state. Thereby, the voltages applied to the bitline 102 and the inverse bitline 103 are applied to the inputs 113, 114 of the inverters 107, 108. If the initial state of SRAM cell 101 is different from the state to be written to SRAM cell 101, this typically causes the inverters 107, 108 to change their state.

An issue in writing data to SRAM cell 101 can be avoiding a write failure, wherein the SRAM cell 101 does not change its state, although the state to be written to the SRAM cell 101 is different from the initial state. The likelihood of a write failure occurring can be related to a ratio between a conductivity of pass-gate transistors 109, 110 in the on state, and a conductivity of pull-up transistors 115, 116 in the on state, which is denoted as "gamma ratio". In general, a greater gamma ratio can reduce the likelihood of a write failure occurring.

Accordingly, for avoiding write failures, it can be advantageous if the conductivities of the pass-gate transistors 109, 110 in the on state (and, accordingly, a width of the channel regions of these transistors) are relatively large compared to the conductivities of the pull-up transistors 115, 116 in the on state (and, accordingly, a width of the channel regions of these transistors).

Hence, there can be a trade off between the stability of SRAM cell 101 with respect to read disturbances, and a writability of the SRAM cell 101, which is related to the occurrence of write failures occurring. A greater conductivity of the pass-gate transistors 109, 110 in the on state can be helpful for reducing the likelihood of write failures occurring but, at the same time, may increase the likelihood of read disturbances.

For avoiding these issues, it has been proposed to modify the design of SRAM cells by separating the write and read path though an additional port. However, such solutions typically require two additional transistors per SRAM cell, and also require an additional

read wordline per row of the device 100, as well as an additional read bitline per column of the device 100. This can substantially increase the area of the device 100 that is required for storing one bit of information.

In view of the situation described above, the present disclosure is related to a method of writing data to one or more SRAM cells and a device comprising a plurality SRAM cells that allows to obtain a relatively high stability with respect to read disturbances and a relatively low likelihood of write failures occurring, while substantially avoiding or at least reducing an increase of the area of the device required for storing one bit of information.

SUMMARY OF THE DISCLOSURE

An illustrative method disclosed herein comprises writing data to one or more static access random memory (SRAM) cells. Writing data to the one or more SRAM cells comprises applying a data signal to at least one bitline electrically connected to the one or more SRAM memory cells, electrically disconnecting at least one of a first power supply terminal and a second power supply terminal of each of the one or more SRAM cells from a power supply, and applying a wordline signal to a wordline connected to the one or more SRAM cells. Thereafter, the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells is electrically connected to the power source.

An illustrative device as disclosed herein comprises a plurality of bitlines, a plurality of wordlines, a plurality of static random-access memory (SRAM) cells, a plurality of first switching devices and a data writing circuit. Each SRAM cell is electrically connected to one of the bitlines and one of the wordlines. Moreover, each SRAM cell has a first power supply terminal and a second power supply terminal. Each first switching device is electrically connected between the first power supply terminal of at least one of the SRAM cells and a power source. The data writing circuit is adapted for applying a data signal to each bitline connected to the at least one of the SRAM cells, operating at least one of the first switching devices for electrically disconnecting the first power supply terminal of at least one of the plurality of SRAM cells from the power source, and applying a wordline signal to a wordline connected to the at least one of the SRAM cells.

BRIEF DESCRIPTION OF THE DRAWINGS

Further embodiments are defined in the appended claims and will become more apparent with the following detailed description when taken with reference to the accompanying drawings, in which:

Fig. 1 schematically illustrates an SRAM device;

Fig. 2 schematically illustrates a device according to an embodiment;

Fig. 3 schematically illustrates an SRAM cell of the device shown in Fig. 2;

Fig. 4a schematically illustrates signals applied in a method of operating the device of Fig. 2 according to an embodiment; and

Fig. 4b schematically illustrates signals applied in a method of operating the device of Fig. 2 according to another embodiment.

DETAILED DESCRIPTION

While the present disclosure is described with reference to the embodiments as illustrated in the following detailed description as well as in the drawings, it should be understood that the following detailed description as well as the drawings are not intended to limit the subject matter disclosed herein to the particular illustrative embodiments disclosed, but rather the described illustrative embodiments merely exemplify the various aspects of the present disclosure, the scope of which is defined by the appended claims.

Embodiments provide devices comprising SRAM cells and methods for operating devices comprising SRAM cells with an enable function that allows to disconnect a high voltage provided by a power supply (sometimes denoted "VDDA") and/or a low voltage (sometimes denoted "VSS") provided by the power supply from SRAM cells during a write operation. In this case, the data writing circuit does not need to overpower pull-up transistors and pull-down transistors of the SRAM cells. During a read operation, wherein data are read from the device, the power supply can remain connected to the SRAM cells.

In embodiments, VDDA and/or VSS segmentation along wordlines of the device can be used. Thus, all cells along an activated wordline can be written simultaneously, while the other cells of the device can remain in the stand-by mode. The disconnection of VDDA and/or VSS can be achieved by a single transistor per wordline domain (if one of VDDA and VSS is disconnected during the write operation) or two transistors per wordline

domain (if both VDDA and VSS are disconnected during the write operation). For disconnecting VDDA, a p-channel transistor can be used, and an n-channel transistor can be used for disconnecting VSS. Since p-channel transistors can be switched from an electrically conductive on-state to a substantially nonconductive off-state if a high voltage is applied to their gate electrode, and n-channel transistors can be switched from a substantially nonconductive off-state to an on-state, if a high voltage is applied to the gate electrode, signals applied to gate electrodes of the p-channel transistors can be inverse to signals applied to gate electrodes of the n-channel transistors so that a low voltage is applied to the gate electrode of the p-channel transistor associated with a specific wordline domain when a high voltage signal is applied to the gate electrode of the n-channel transistor of the wordline domain, and vice versa.

By disconnecting the SRAM cells from VDDA and/or VSS during the write operation, the influence of device targeting on the writability of the SRAM cell can be eliminated or at least reduced. Accordingly, the SRAM cells can be optimized for stability with respect to read disturbances, while substantially avoiding or at least reducing an adverse influence on the writability of the SRAM cells. Since, for doing so, no additional transistors are needed in individual SRAM cells, substantially no additional area is needed for the individual SRAM cells.

In some embodiments, the enable signal for disconnecting the SRAM cells from VDDA and VSS and a wordline signal for switching the pass-gate transistors of these SRAM cells into the on-state can be applied substantially simultaneously. In other embodiments, a separate timing can be used for the enable signal and the wordline signal, wherein the wordline signal can be applied later than the enable signal. This may help to further improve the writability of the SRAM cells, since the voltage difference between the high voltage side and the low voltage side of the SRAM cells can decrease in the time interval between the point of time at which the enable signal is applied and the point of time at which the wordline signal is applied.

Further embodiments will be described with respect to Figs. 2, 3, 4a and 4b.

Fig. 2 schematically illustrates a device 200 according to an embodiment comprising an array 220 of SRAM cells 201a, 201b, 201c and 201d.

The array 220 comprises a plurality of rows 221a, 221b, wherein row 221a comprises SRAM cells 201a, 201b, and row 221b comprises SRAM cells 201c, 201d. The array 220 further comprises a plurality of columns 222a, 222b, wherein SRAM cells 201a, 201c are

provided in column 222a, and SRAM cells 201b, 201d are provided in column 222b. Accordingly, each of SRAM cells 201a-201d is located in one row of the array 220 and in one column of the array 220.

The device 200 need not comprise four SRAM cells, as shown in Fig. 2. In embodiments, a greater number of SRAM cells can be provided, and the array 220 can comprise more than two rows and more than two columns.

The device 200 comprises a plurality of wordlines 204a, 204b, wherein each wordline is associated with one of the rows 221a, 221b of the array 220. In particular, wordline 204a is associated with row 221a, and wordline 204b is associated with row 221b. Each of SRAM cells 201a-201d is electrically connected to the wordline associated with the row wherein the SRAM cell is provided. In particular, SRAM cells 201a, 201b are electrically connected to wordline 204a associated with the row 221a by wordline connections 207a and 207b, respectively, and SRAM cells 201c, 201d are electrically connected to wordline 204b associated with row 221b by wordline connections 207c, 207d.

The device 200 further comprises a plurality of high voltage power supply lines 205a, 205b. Each high voltage power supply line is associated with one of the rows 221a, 221b of the array 220. In particular, high voltage power supply line 205a is associated with row 221a, and high voltage power supply line 205b is associated with row 221b. Each of SRAM cells 201a-201d is electrically connected to the high voltage power supply line associated with the row wherein the SRAM cell is provided. In particular, SRAM cells 201a, 201b are electrically connected to high voltage power supply line 205a by first power supply terminals 208a and 208b, respectively, and SRAM cells 201c, 201d are connected to the high voltage power supply line 205b by first power supply terminals 208c and 208d, respectively.

The device 200 further comprises a plurality of low voltage power supply lines 206a, 206b. Each low voltage power supply line is associated with one of the rows 221a, 221b. In particular, low voltage power supply line 206a is associated with row 221a and low voltage power supply line 206b is associated with row 221b.

Each of SRAM cells 201a-201d is electrically connected to one of the low voltage power supply lines 206a, 206b, associated with the row wherein the SRAM cell is provided. In particular, SRAM cells 201a, 201b are electrically connected to low voltage power supply line 206a associated with the row 221a by second power supply terminals 209a and

209b, respectively, and SRAM cells 201c, 201d are electrically connected to low voltage power supply line 206b by second power supply terminals 209c and 209d, respectively.

The device 200 further comprises a plurality of bitlines 202a, 202b and a plurality of inverse bitlines 203a, 203b, each bitline and each inverse bitline being associated with one of the columns 222a, 222b of the array 220. In particular, bitline 202a and inverse bitline 203a are associated with column 222a, and bitline 202b and inverse bitline 203b are associated with column 222b. Each of SRAM cells 201a-201d is electrically connected to a bitline associated with the column wherein the SRAM cell is provided, and one of the inverse bitlines associated with the column wherein the SRAM cell is provided. In particular, SRAM cells 201a and 201c are electrically connected to bitline 202a associated with column 222a by bitline terminals 211a and 211c, respectively, and are electrically connected to inverse bitline 203a by inverse bitline terminals 210a and 210c, respectively. SRAM cells 201b and 201d are electrically connected to bitline 202b by bitline terminals 211b and 211d, respectively, and are electrically connected to inverse bitline 203b by inverse bitline terminals 210b and 210d, respectively.

The device 200 further comprises a plurality of high voltage switching devices 212a, 212b. Each of the high voltage switching devices 212a, 212b is electrically connected between one of the high voltage power supply lines 205a, 205b and a high voltage terminal 215 of a power source 214. In particular, high voltage switching device 212a is electrically connected between high voltage terminal 215 and high voltage power supply line 205a, and high voltage switching device 212b is electrically connected between high voltage terminal 215 and high voltage power supply line 205b. Accordingly, there is one high voltage switching device associated with each of the rows 221a, 221b of the array 220. In embodiments, the high voltage switching devices 212a, 212b can be p-channel field effect transistors.

The device 200 further comprises a plurality of low voltage switching devices 213a, 213b which, in embodiments, can be n-channel field effect transistors. Each of the low voltage switching devices 213a, 213b is electrically connected between a low voltage terminal 216 of power supply 214 and one of the low voltage power supply lines 206a, 206b. In particular, low voltage switching device 213a is electrically connected between low voltage terminal 216 and low voltage power supply line 206a, and low voltage switching device 213b is electrically connected between low voltage terminal 216 and low voltage power supply line 206b. Accordingly, each of the low voltage switching devices is associated with one of the rows 221a, 221b of the array 220.

Further high voltage switching devices and low voltage switching devices can be associated with other rows of array 220 which are not shown in Fig. 2.

The device 200 further comprises a control circuit 217 that is electrically connected to the wordlines 204a, 204b, the bitlines 202a, 202b and the inverse bitlines 203a, 203b, and is adapted for controlling voltages applied thereto. Furthermore, the control circuit is electrically connected to the high voltage switching devices 212a, 212b and the low voltage switching devices 213a, 213b for switching the high voltage switching devices 212a, 212b and the low voltage switching devices 213a, 213b between an electrically conductive on-state and a substantially nonconductive off-state. Accordingly, the control circuit 217 can be adapted for connecting and disconnecting an electrical connection between the high voltage power supply lines 205a, 205b and the high voltage terminal 215 of power supply 214 by operating the high voltage switching devices 212a, 212b, wherein each of the high voltage power supply lines 205a, 205b can be electrically disconnected from the high voltage terminal 215 individually by operating the respective high voltage switching device.

Similarly, the control circuit 217 can be adapted for operating the low voltage switching devices 213a, 213b for connecting and disconnecting an electrical connection between the low voltage power supply lines 206a, 206b and the low voltage terminal 216 of the power supply 214, wherein each of the low voltage power supply lines 206a, 206b can be electrically disconnected from the low voltage terminal 216 individually by operating the respective low voltage switching device.

In embodiments wherein the high voltage switching devices 212a, 212b comprise p-channel field effect transistors and the low voltage switching devices 213a, 213b comprise n-channel field effect transistors, the control circuit 217 can be connected to the gate electrodes of the switching devices 212a, 212b, 213a, 213b. The high voltage switching devices 212a, 212b can be switched from the on-state to the off-state by increasing the voltage applied to the gate electrode, for example by switching the voltage applied to the gate electrode from the low voltage provided from power source 214 to the high voltage provided by the power source 214. The n-channel transistors of the low voltage switching devices 213a, 213b can be switched from the on-state to the off-state by reducing the voltage applied to the gate electrode thereto, for example from switching from the high voltage provided by the power supply 214 to the low voltage provided by the power supply.

The control circuit 217 can comprise a write control circuit 218 and a read control circuit 219, as schematically indicated in Fig. 2. In embodiments, some components of the control circuit 217 can be shared between the read control circuit 218 and the write control circuit 219, and optionally further elements of the control circuit.

In embodiments, the high voltage provided by the power supply 214 can be in a range from about 0.5 V to about 2.0 V, and the low voltage provided by the power supply 214 can be about 0 V. In some embodiments, the voltage levels can be adapted to a mode of operation, for example in accordance with temperature and/or power saving requirements. The configuration of SRAM cell 201a according to an embodiment will be described with reference to Fig. 3.

The SRAM cell 201a has a high voltage power supply terminal 208a and a low voltage power supply terminal 209a.

The SRAM cell 201a further comprises a first inverter 307 and a second inverter 308. The high voltage power supply terminal 208a is provided on a high voltage side of the inverters 307, 308, and the low voltage power supply terminal 209a is provided on a low voltage side of the inverters 307, 308.

In embodiments, the high voltage power supply terminal 208a can be provided in form of two separate electrically conductive features, for example electrically conductive lines in an integrated circuit, as schematically shown in Fig. 3, wherein one electrically conductive feature connects the first inverter 307 to the high voltage power supply line 205a, and the other electrically conductive feature connects the second inverter 308 to the high voltage power supply line 205a.

Similarly, in embodiments the low voltage power supply terminal 209a can be provided in form of two separate electrically conductive features, for example electrically conductive lines in an integrated circuit, which connect the low voltage sides of inverters 307, 308 to the low voltage power supply line 206a.

In other embodiments, the high voltage power supply terminal 208a can be provided in form of a single electrically conductive feature and/or the low voltage power supply terminal 209a can be provided in form of a single electrically conductive feature.

The first inverter 307 comprises a pull-up transistor 315, which can be a p-channel field effect transistor and a pull-down transistor 317, which can be an n-channel field effect transistor. The first inverter 307 comprises an output 311. A pass-gate transistor 309 is

electrically connected between the inverse bitline terminal 210a and the output 311 of the first inverter 307. The gate of pass-gate transistor 309 is electrically connected to the wordline connection 207a.

Similarly, the second inverter 308 has an output 312, an input 314, a pull-up transistor 316 and a pull-down transistor 318. A pass-gate transistor 310 is electrically connected between the output 312 and the bitline terminal 211a, a gate electrode of the pass-gate transistor 310 being electrically connected to the wordline connection 207a.

Similar to the power supply terminals 208a, 209a, the wordline connection 207a can comprise two separate electrically conductive features providing an electrical connection between the gate electrodes of pass-gate transistors 309, 310 and the wordline 204a, or the wordline connection 207a can be provided in form of a single electrically conductive feature.

The output 311 of the first inverter 307 is electrically connected to an input 314 of the second inverter 308, and the output 312 of the second inverter 308 is electrically connected to an input 313 of the first inverter 307.

The SRAM cell 201a is formed by six transistors (two pull-up transistors 315, 316, two pull-down transistors 317, 318 and two pass-gate transistors 309, 310). Accordingly, SRAM cell 201a is a six transistor SRAM cell.

Further features of SRAM cell 201a can correspond to those of SRAM cell 101 described above with reference to Fig. 1.

The SRAM cells 201b, 201c, 201d and optional further SRAM cells of device 200 can have a configuration corresponding to the configuration of SRAM cell 201a.

In the following, the operation of device 200 according to an embodiment will be described with reference to Fig. 4a.

Fig. 4a is a graph illustrating signals which can be applied in the device 200 when data are written to SRAM cells. A first coordinate axis 401 denotes time, and a second coordinate axis 402 denotes a voltage of the signals. For simplicity, in Fig. 4a, curves showing the voltage of signals have been shifted in the vertical direction, so that there is no overlap between the curves. Each of the signals shown in Fig. 4a can have a voltage substantially equal to the low voltage provided by the power source 214 or a voltage

substantially equal to the high voltage provided by the power source 214, and optionally can be switched between the low voltage and the high voltage.

Accordingly, in Fig. 4a, a rising edge of a signal indicates a transition from the low voltage to the high voltage, and a falling edge indicates a transition from the high voltage to the low voltage.

Fig. 4a shows an illustrative embodiment wherein data are written to SRAM cells 201a, 201b in the row 221a of the array 220 of SRAM cells.

During a time interval between a point of time 403 and a point of time 406, a data signal 407 is applied to bitline 202a, and a data signal 409 is applied to bitline 202b. The signals 407, 409 correspond to data which are to be written to SRAM cells 201a, 201b.

In Fig. 4a, a situation is shown wherein the state of SRAM cell 201a to be obtained in the write procedure is a state wherein the output of the second inverter of SRAM cell 201a (that is electrically connected to bitline 202a) is at the high voltage, and the state of SRAM cell 201b to be obtained is a state wherein the output of the second inverter of SRAM cell 201b (that is electrically connected to bitline 202b) is at the low voltage.

Before the point of time 403 and after the point of time 406, bitlines 202a, 202b can be at the high voltage. The voltages applied to bitlines 202a, 202b in the time interval between the points of time 403, 406 correspond to the voltages of the outputs of the second inverters of SRAM cells 201a, 201b to be obtained after the writing procedure. Hence, in the example shown in Fig. 4a, data signal 407 remains at the high voltage, and data signal 409 is switched from the high voltage to the low voltage during the time interval.

If the state of SRAM cell 201a to be obtained after writing data to SRAM cell 201a were a state wherein the output of the second inverter of SRAM cell 201a is at the low voltage, the bitline 202a would be switched to the low voltage during the time interval between point of time 403 and point of time 406, and if the state of SRAM cell 201b to be obtained after the write procedure would be a state wherein the output of the second inverter of SRAM cell 201b is at the high voltage, bitline 202b would be maintained at the high voltage during the time interval.

During the time interval from point of time 403 to point of time 406, an inverse data signal 408 can be applied to inverse bitline 203a, and an inverse data signal 410 can be applied to inverse bitline 203b. Inverse data signal 408 is inverse to data signal 407, wherein inverse data signal 408 is low if data signal 407 is high, and inverse data signal 408 is

high if data signal 407 is low. Inverse data signal 410 is inverse to data signal 409, wherein inverse data signal 410 is low if data signal 409 is high, and inverse data signal 410 is high if data signal 409 is low. Before point of time 403 and after point of time 406, the inverse bitlines 203a, 203b can be maintained at the high voltage.

During the time interval from point of time 403 to point of time 406, further data signals and inverse data signals can be applied to bitlines and inverse bitlines which are connected to SRAM cells other than SRAM cells 201a, 201b in row 221a of the array 220 which are not shown in Fig. 2 for writing data to all SRAM cells in row 221a.

At a point of time 404, which can be after point of time 403 and before point of time 406, an enable signal 412 can be applied to low voltage switching device 213a for electrically disconnecting the low voltage power supply line 206a from the low voltage terminal 216 of the power supply 214. In embodiments wherein the low voltage switching device 213a comprises an n-channel field effect transistor, the enable signal 412 can be applied by switching a voltage applied to the gate electrode of the n-channel field effect transistor from the high voltage to the low voltage.

At substantially the same point of time 404, an inverse enable signal 413 can be applied to the high voltage switching device 212a for electrically disconnecting the high voltage power supply line 205a from the high voltage terminal 215 of the power supply 214. In embodiments wherein the high voltage switching device 212a comprises a p-channel field effect transistor, the inverse enable signal can be applied by switching a voltage applied to the gate electrode of the p-channel field effect transistor from the low voltage to the high voltage.

By applying the enable signal 412 to the low voltage switching device 213a and the inverse enable signal 413 to the high voltage switching device 212a, the high voltage power supply line 205a and the low voltage power supply line 206a are electrically disconnected from the power source 214. Since the high voltage power supply terminals 208a, 208b of the SRAM cells 201a, 201b in the row 221a are electrically connected to the power source 214 via the high voltage power supply line 205a, the high voltage power supply terminals 208a, 208b are thus electrically disconnected from the power source 214. Similarly, the low voltage power supply terminals 209a, 209b of SRAM cells 201a, 201b are electrically disconnected from power source 214.

A wordline signal 411 can be applied to the wordline 204a associated with the row 221a of the array 220 wherein the SRAM cells 201a, 201b are provided. This can be done by

switching the voltage of the wordline 204a from low to high. In embodiments, the wordline signal 411 can be applied at the same time 404 at which the high voltage power supply line 205a and the low voltage power supply line 206a are electrically disconnected from the power source 214.

By applying the wordline signal 411 to wordline 204a, the pass-gate transistors of SRAM cells 201a, 201b are switched into the electrically conductive on-state, so that the voltage applied to the respective bitline electrically connected to each SRAM cell in row 221a is applied to the input of one of the inverters of the SRAM cell, and the voltage applied to the respective inverse bitline electrically connected to each SRAM cell is applied to the input of the other inverter.

In particular, by applying the wordline signal 411, the voltage applied to bitline 202a is applied to the input 313 of the first inverter 307 of SRAM cell 201a, and the voltage applied to inverse bitline 203a is applied to the input 314 of the second inverter 308 of SRAM cell 201a. Moreover, as can be seen from the circuit diagram shown in Fig. 3, the voltage of bitline 202a is applied to the output 312 of the second inverter 308, and the voltage of the inverse bitline 203a is applied to the output 311 of the first inverter 307.

Since the SRAM cells 201a, 201b were electrically disconnected from the power source 214 by applying the enable signal 412 and the inverse enable signal 413, there is substantially no electrical connection between the inputs and outputs of the inverters of the SRAM cells 201a, 201b and the power source 214 of the device 200 when the wordline signal 411 is applied. Accordingly, the voltages applied to the bitlines 202a, 202b and inverse bitlines 203a, 203b need not overcome the voltage of the power source 214 applied to the input and outputs of the inverters via the pull-up transistors and pull-down transistors.

Hence, compared to the device described above with reference to Fig. 1, the writability of the device 200 can be improved. In contrast to proposals according to the state of the art, wherein more than six transistors are provided in each SRAM cell, an improved writability can be obtained in embodiments of the present disclosure wherein each of the SRAM cells 201a-201d is a six transistor SRAM cell, as described above with reference to Figs. 2 and 3.

However, the structure of the SRAM cells is not limited to the six-transistor configuration described above with reference to Figs. 2 and 3. In other embodiments, different

configurations of SRAM cells which can optionally comprise more than six transistors can be employed.

Concerning the high voltage switching devices 212a, 212b and the low voltage switching devices 213a, 213b, as described above, in embodiments, a single high voltage switching device and a single low voltage switching device can be provided for each of the rows 221a, 221b of the array 220 of SRAM cells, and each row 221a, 221b can comprise a relatively large number of individual SRAM cells. Thus, the high voltage switching devices 212a, 212b and the low voltage switching devices 213a, 213b do not substantially increase the area on a substrate occupied by device 200, or increase the area of device 200 only to a relatively low extent.

At a point of time 405, which is later than the point of time 404 and earlier than the point of time 406, the enable signal 412 and the inverse enable signal 413 are no longer applied to the high voltage switching device 212a and the low voltage switching device 213a, and, instead, the high voltage switching device 212a and the low voltage switching device 213a can be operated for electrically connecting the high voltage power supply line 205a to the high voltage terminal 215 of power source 214, and for electrically connecting the low voltage power supply line 206a to the low voltage terminal 216 of the power source 214. In embodiments wherein the high voltage switching device 212a comprises a p-channel field effect transistor and the low voltage switching device 213a comprises an n-channel field effect transistor, this can be done by applying the high voltage to the n-channel field effect transistor and applying the low voltage to the p-channel field effect transistor.

Additionally, the wordline signal 411 is no longer applied to wordline 204a, so that the pass-gate transistors of the SRAM cells 201a, 201b in the row 221a of the array 220 electrically disconnect the inputs and outputs of the inverters of the SRAM cells from the bitlines 202a, 202b and the inverse bitlines 203a. Thus, the SRAM cells 201a, 201b are switched into the stand-by mode, wherein the SRAM cells 201a, 201b maintain the state into which they were set during the write procedure.

Fig. 4b shows a graph illustrating signals applied in a method of writing data to SRAM cells in the device 200 according to an embodiment.

Different from the embodiment of Fig. 4a, in the embodiment of Fig. 4b, the wordline signal (denoted by reference numeral 416 in Fig. 4b) is applied at a point of time 414 which is later than the point of time 404 at which the enable signal 412 and the inverse

enable signal 413 are applied. Moreover, the wordline signal 416 can be applied until a point of time 415, which is between the point of time 405 at which the enable signal 412 and the inverse signal 413 are no longer applied, and the point of time 406 at which the data signals and inverse data signals are no longer applied. Thus, in the embodiment of Fig. 4b, applying the enable signal 412 and the inverse enable signal 413 on the one hand, and applying the wordline signal 416, on the other hand, are not performed substantially simultaneously.

Further features of the embodiment of Fig. 4b can correspond to the embodiment described above with reference to Fig. 4a.

Due to the capacitance of the high voltage power supply line 205a and the low voltage power supply line 206a, the voltage at the high power supply terminals 208a, 208b of SRAM cells 201a, 201b may require an amount of time for decreasing to a voltage that is substantially lower than the high voltage provided by the power supply 214. Applying the wordline signal 416 at the point of time 414 that is later than the point of time 404 at which the enable signal 412 and the inverse enable signal 413 are applied may help to ensure that the wordline signal 416 is applied at a point of time at which the voltage difference between the high voltage power supply terminals 208a, 208b and the low voltage power supply terminals 209a, 209b has decreased to a sufficient extent. This may help to further improve the writability of the SRAM cells.

In embodiments, the time interval between the point of time 404 and point of time 415 may have a duration that is selected in accordance with a clock speed of the device 200, which can be in a range from about 1 MHz to about 10 GHz.

Applying the wordline signal 416 longer than the enable signal 412 and the inverse enable signal 413 until point of time 415 can help to ensure that the SRAM cells 201a, 201b are in their intended state when the SRAM cells 201a, 201b are electrically connected to the power supply 214 at point of time 415. It could be possible that when the SRAM cells 201a, 201b are electrically connected to the power source 214 at the same time at which the wordline signal 416 is turned off, the state of the SRAM cells 201a, 201b can be influenced by leakage currents, and leak away faster than the inverters of SRAM cells 201a, 201b can be powered. Although the likelihood thereof might be relatively low, maintaining the wordline signal 416 longer can eliminate the issue.

In the method described above with reference to Fig. 4a, as well as in the method described above with reference to Fig. 4b, data can be written to the SRAM cells in a row of the array 220 of SRAM cells other than the row 221a by applying the enable signal 412 to the low voltage switching device associated with the respective row, applying the inverse enable signal to the high voltage switching device associated with the respective row, and applying the wordline signal 411 or 416, respectively, to the wordline associated with the respective row of the array 220.

The control circuit 217 can be adapted for carrying out the above-described methods of writing data to SRAM cells in the device 200. In particular, the write control circuit 218 can be adapted for applying the data signals, inverse data signals, enable signal, inverse enable signal and wordline signal.

For reading data from one or more of the SRAM cells 201a-201d of the device 200, the bitline and the inverse bitline connected to the SRAM cell can be pre-charged to the high voltage. For example, for reading data from the SRAM cell 201a, the bitline 202a and the inverse bitline 203a can be pre-charged to the high voltage.

Thereafter, the bitline 202a and the inverse bitline 203a can be left electrically floating, and a wordline signal similar to the wordline signal 411 described above with reference to Fig. 4a can be applied to wordline 204a. Thus, the pass-gate transistors 309, 310 are switched into an electrically conductive on-state state, so that the bitline 202a is electrically connected to the output 312 of the second inverter 308, and the inverse bitline 203a is electrically connected to the output 311 of the first inverter 307. This causes a voltage difference between bitline 202a and inverse bitline 203a that depends on the state of the SRAM cell 201a. The voltage difference can be sensed by a sense amplifier (not shown) in control circuit 217 to determine the state of the SRAM cell 201a.

For reading the state of another SRAM cell in the device 200, similar steps can be performed, wherein the bitline, inverse bitline, and wordline connected to the respective SRAM cell are used. In embodiments, all SRAM cells in one of the rows 221a, 221b of the array 220 can be read simultaneously.

In embodiments, during the read operation, the high voltage switching devices 212a, 212b and the low voltage switching devices 213a, 213b are not operated, so that the SRAM cells from which data are to be read remain electrically connected to the power source 214.

Further features of methods of reading data from the SRAM cells 201a-201d of the device 200 can correspond to features of the method of reading data from device 100 described above with reference to Fig. 1.

The read control circuit 219 can be adapted to perform the above-described method of reading data.

In embodiments, SRAM cells 201a-201d of device 200 can be optimized for stability. As detailed above, the device 200 can have an improved writability as compared to, for example, the device described above with reference to Fig. 1. Accordingly, the gamma ratio, being a ratio between a conductivity of pass gate transistors 309, 310 in the on state, and a conductivity of pull-up transistors 315, 316 in the on state, which can be critical in a write operation as described above with reference to Fig. 1 is not critical any more in device 200, or at least less critical. Hence, SRAM cells 201a-201d can be provided with a relatively high beta ratio, being a ratio between the conductivity of their pull-down transistors 317, 318 in the on state and the conductivity of their pass-gate transistors 309, 310 in the on state, which can be helpful for increasing the stability of SRAM cells 201a-201d with respect to read disturbances. Moreover, an alpha ratio of SRAM cells 201a-201d, being a ratio between a conductivity of their pull up transistors 315, 316 in the on state and a conductivity of their pull down transistors 317, 318 in the on state can be freely optimized for achieving a desired signal to noise margin. The conductivities of the transistors 201a-201d can be adapted by adapting the width of the channel regions of the transistors.

The present disclosure is not limited to embodiments wherein both a high voltage power supply line and a low voltage power supply line are electrically disconnected from the power source 214 when data are written to SRAM cells. In other embodiments, the low voltage switching devices 213a, 213b can be omitted and the low voltage power supply lines 206a, 206b can remain electrically connected to the low voltage terminal 216 of the power supply 214 when data are written to SRAM cells. In such embodiments, the high voltage switching devices 212a, 212b can be used for electrically disconnecting the high voltage power supply lines 205a, 205b from the high voltage terminal 215 of the power source 214 when data are written to SRAM cells.

In further embodiments, the high voltage switching devices 212a, 212b can be omitted, and the high voltage power supply lines 205a, 205b can remain electrically connected to the high voltage terminal 215 of the power supply 214 when data are written to SRAM cells. In such embodiments, the low voltage switching devices 213a, 213b can be used

for electrically disconnecting the low voltage power supply lines 206a, 206b from the low voltage terminal 216 of the power source 214 when data are written to SRAM cells.

Moreover, the present disclosure is not limited to embodiments wherein the device 200 is operated as described above with reference to Figs. 4a and 4b. In other embodiments, the wordline signal 416 can be applied before the enable signal 412 and the inverse enable signal 413 are applied, the enable signal 412 and the inverse enable signal 413 being applied longer than the wordline signal 416. In further embodiments, the wordline signal 416 can be applied before the enable signal 412 and the inverse enable signal 413 are applied, the wordline signal 416 being applied longer than the enable signal 412 and the inverse enable signal 413. In further embodiments, the wordline signal 416 can be applied after the enable signal 412 and the inverse enable signal 413 are applied, the enable signal 412 and the inverse enable signal 413 being applied longer than the wordline signal 416.

Further modifications and variations of the present disclosure will be apparent to those skilled in the art in view of this description. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the principles disclosed herein. It is to be understood that the forms shown and described herein are to be taken as the presently preferred embodiments.

CLAIMS

1. A method, comprising:

writing data to one or more static random access memory (SRAM) cells, wherein writing data to the one or more SRAM cells comprises applying a data signal to at least one bit line electrically connected to the one or more SRAM memory cells, electrically disconnecting at least one of a first power supply terminal and a second power supply terminal of each of the one or more SRAM cells from a power supply, and applying a word line signal to a word line electrically connected to the one or more SRAM cells; and

thereafter electrically connecting the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells to the power source.

2. The method of claim 1, wherein electrically disconnecting the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells from the power supply and applying the word line signal to the word line are performed substantially simultaneously.

3. The method of claim 2, wherein the word line signal is provided to the word line at least until the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells is electrically connected to the power source.

4. The method of claim 1, wherein the word line signal is applied to the word line after electrically disconnecting the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells from the power supply.

5. The method of claim 4, wherein the word line signal is provided to the word line for a time interval, and wherein the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells is electrically connected to the power source before the end of the time interval.

6. The method of claim 1, wherein the data signal is applied to the at least one bit line before electrically disconnecting the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells from the power supply.

7. The method of claim 6, wherein the data signal is provided to the at least one bit line at least until the at least one of the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells is electrically connected to the power source.

8. The method of claim 1, wherein writing data to the one or more SRAM cells further comprises:

applying an inverse data signal to at least one inverse bit line electrically connected to the one or more SRAM cells, the data signal and the inverse data signal being applied substantially simultaneously.

9. The method of claim 8, further comprising reading data from the one or more SRAM cells, wherein reading data from the one or more SRAM cells comprises:

pre-charging the at least one bit line and the at least one inverse bit line;

applying a word line signal to the word line electrically connected to the one or more SRAM cells; and

for each of the one or more SRAM cells, sensing a voltage difference between one of the at least one bit line electrically connected to the SRAM cell and one of the at least one inverse bit line electrically connected to the SRAM cell;

wherein the first power supply terminal and the second power supply terminal of each of the one or more SRAM cells remain electrically connected to the power source while the data are read.

10. The method of claim 1, wherein each SRAM cell is a six transistor SRAM cell.

11. A device, comprising:

a plurality of bit lines;

a plurality of word lines;

a plurality of static random access memory (SRAM) cells, each SRAM cell being electrically connected to one of the bit lines and one of the word lines, each SRAM cell having a first power supply terminal and a second power supply terminal;

a plurality of first switching devices, each first switching device being electrically connected between the first power supply terminal of at least one of the SRAM cells and a power source; and

a data writing circuit adapted for applying a data signal to each bit line electrically connected to the at least one of the SRAM cells, operating at least one of the first switching devices for electrically disconnecting the first power supply terminal of at least one of the plurality of SRAM cells from the power source, and applying a word line signal to a word line electrically connected to the at least one of the SRAM cells.

12. The device of claim 11, further comprising: a plurality of second switching devices, wherein each second switching device is electrically connected between the second power supply terminal of the at least one of the SRAM cells and the power source.

13. The device of claim 11, wherein the plurality of SRAM cells comprises an array of SRAM cells, the array of SRAM cells comprising a plurality of rows, each row comprising two or more SRAM cells, each word line being associated with one of the rows, each SRAM cell being electrically connected to the word line associated with the row wherein the SRAM cell is provided.

14. The device of claim 13, further comprising a plurality of high voltage power supply lines, each high voltage power supply line being associated with one of the rows, the first power supply terminal of each SRAM cell being electrically connected to the high voltage power supply line associated with the row wherein the SRAM cell is provided, each of the first switching devices being electrically connected between one of the high voltage power supply lines and the power source.

15. The device of claim 14, wherein the first power supply terminals of the SRAM cells are high voltage terminals, and wherein each of the first switching devices comprises a P-channel field effect transistor.

16. The device of claim 14, further comprising a plurality of low voltage power supply lines, each low voltage power supply line being associated with one of the rows, the second power supply terminal of each SRAM cell being electrically connected to the low voltage power supply line associated with the row wherein the SRAM cell is provided, the device further comprising a plurality of second switching devices, each of the second switching devices being electrically connected between one of the low voltage power supply lines and the power source.

17. The device of claim 16, wherein the second power supply terminals of the SRAM cells are low voltage terminals, and wherein each of the second switching devices comprises an N-channel field effect transistor.

18. The device of claim 11, further comprising a plurality of inverse bit lines, each SRAM cell being electrically connected to one of the inverse bit lines, wherein said data writing circuit is adapted to apply an inverse data signal to each inverse bit line electrically connected to the at least one of the SRAM cells, wherein the data signal and the inverse data signal are applied substantially simultaneously.

19. The device of claim 18, further comprising a read circuit adapted for precharging the bit line and the inverse bit line electrically connected to at least one of the plurality of SRAM cells, applying a word line signal to a word line electrically connected to the at least one of the plurality of SRAM cells, and sensing a voltage difference between the bit line and the inverse bit line for each of the at least one of the plurality of SRAM cells, wherein the first power supply terminal and the second power supply terminal of each of the at least one of the plurality of SRAM cells remain electrically connected to the power source.

20. The device of claim 11, wherein each SRAM cell is a six transistor SRAM cell.

21. A device having a SRAM cell, wherein data is written to the SRAM through a method of any one of claims 1-10.

22. The device of any one of claim 11-20 wherein data is written to the SRAM through a method of any one of claims 1-10.