

SHOWERHEAD OR SHOWER-PEDESTAL EDGE RING FOR FILM EDGE THICKNESS MODULATION

INCORPORATION BY REFERENCE

[0001] A PCT Request Form is filed concurrently with this specification as part of the present application. Each application that the present application claims benefit of or priority to as identified in the concurrently filed PCT Request Form is incorporated by reference herein in their entireties and for all purposes.

BACKGROUND

[0002] Semiconductor manufacturing processes often occur within a chamber in which a semiconductor wafer or semiconductor wafers are supported on one or more wafer supports during wafer processing operations. Such a semiconductor wafer may be positioned facing (e.g., underneath or above) a corresponding process gas distribution system, e.g., a showerhead or a shower-pedestal, that may be used to distribute process gases across the side of the semiconductor wafer facing the showerhead or shower-pedestal, i.e., the side of the wafer to be processed.

[0003] For example, in frontside deposition systems, the wafer is positioned on a pedestal underneath the showerhead, and the side of the wafer to be processed is facing upwards. In backside deposition systems, the wafer is elevated away from a shower-pedestal, which is a hybrid of a pedestal and a showerhead that is directed to flow one or more process gases in an upward direction instead of the downward direction that a showerhead is configured to flow process gases in, by wafer support structures, with the side of the wafer to be processed facing downwards toward the shower-pedestal.

[0004] Disclosed herein are gas distribution systems that may provide enhanced tunability of gas flow across the surface of a wafer for use in such processing chambers.

SUMMARY

[0005] Details of one or more implementations of the subject matter described in this specification are set forth in the accompanying drawings and the description below. Other features, aspects, and advantages will become apparent from the description, the drawings, and the claims.

[0006] In some implementations, an apparatus may be provided that includes a wafer support defining a wafer support plane and configured to support a semiconductor wafer having a

diameter of 300 mm, such that when the semiconductor wafer is supported by the wafer support, an underside of the semiconductor wafer is coincident with the wafer support plane. The apparatus may also include a showerhead with one or more sets of gas distribution ports distributed throughout a first region on a first side of the showerhead facing the wafer support plane when the showerhead and wafer support plane are placed in a first configuration. The apparatus may further include a first flow conductance tuning surface with a radial cross-section profile spanning between a first location on the showerhead and a second location offset from the first location by a first distance in a direction perpendicular to, and toward, the wafer support plane, wherein the first location, the second location, and the first flow conductance tuning surface are all in an annular zone centered on the first region and having an inner diameter of 290 mm and an outer diameter of 310 mm, and wherein the first distance is between 10% and 20% of a second distance representing a gap through which process gas flows out of a processing region at the first location, and with the second distance being measured in the direction perpendicular to, and toward, the wafer support plane.

[0007] In some further implementations, the second location may be further from the center axis of the showerhead than the first location.

[0008] In some further implementations, the first location and the second location may be equal in distance from the center axis of the showerhead.

[0009] In some further implementations, the first location and second location may be connected by the first flow conductance tuning surface.

[0010] In some further implementations, the cross-section profile of the first flow conductance tuning surface may be non-linear.

[0011] In some further implementations, the cross-section profile of the first flow conductance tuning surface may feature at least one curved portion.

[0012] In some further implementations, the cross-section profile of the first flow conductance tuning surface may feature: a first curved portion adjacent to the first region and tangent to the showerhead at the first location, and a second curved portion tangent to a surface parallel to the wafer support plane at the second location.

[0013] In some further implementations, the cross-section profile of the first flow conductance tuning surface may feature a wall vertical to the first region.

[0014] In some further implementations, the cross-section profile of the first flow conductance tuning surface may feature a wall with a 30-degree slope to the first region.

[0015] In some further implementations, the first flow conductance tuning surface may be provided by a flow conductance tuning component separate from the showerhead.

[0016] In some further implementations, the first flow conductance tuning surface may be provided by a ring that extends around all of the first region.

[0017] In some further implementations, the first flow conductance tuning surface may be provided by a ring segment that extends only partially about the first region.

[0018] In some further implementations, the apparatus may further include a second flow conductance tuning surface spanning between a third location on the showerhead and a fourth location offset from the third location by a third distance in a direction perpendicular to, and toward, the wafer support plane, wherein the third location, the fourth location, and the second flow conductance tuning surface are all in the annular zone centered on the first region and having an inner diameter of 290 mm and an outer diameter of 310 mm, and wherein the third distance is between 10% and 20% of a fourth distance between the third location of the showerhead and the wafer support plane in the direction perpendicular to, and toward, the wafer support plane.

[0019] In some further implementations, the third distance may be different from the first distance.

[0020] In some further implementations, the first region may be non-planar and bulges toward the wafer support plane, and wherein the first flow conductance tuning surface may connect to the showerhead at the first location.

[0021] In some further implementations, the apparatus may further include a controller configured to cause one or both of the showerhead and the wafer support to be positioned in the first configuration during at least a portion of a semiconductor processing operation in which one or more first process gases are flowed from the gas distribution ports in at least one set of the gas distribution ports, wherein, in the first configuration, the second distance may be between 6 mm and 16 mm.

[0022] In some further implementations, the apparatus may further include a processing chamber and a pedestal, wherein: the first region of the showerhead may be positioned within the processing chamber, and the pedestal may be positioned beneath the showerhead and provides the wafer support.

[0023] In some further implementations, the apparatus may further include a processing chamber and a pedestal, where the first region of the showerhead may be positioned within the processing chamber, and the pedestal may be positioned beneath the showerhead and provides the wafer support.

[0024] In some further implementations, the apparatus may include a wafer support defining a wafer support plane and configured to support a semiconductor wafer having a diameter of 300

mm, such that when the semiconductor wafer is supported by the wafer support, an underside of the semiconductor wafer is coincident with the wafer support plane. The apparatus may further include a showerhead pedestal with one or more sets of gas distribution ports distributed throughout a first region on a first side of the showerhead pedestal facing the wafer support plane when the showerhead pedestal and wafer support plane are placed in a first configuration. The apparatus may further include a first flow conductance tuning surface spanning between a first location on the showerhead pedestal and a second location offset from the first location by a first distance in a direction perpendicular to, and toward, the wafer support plane, wherein the first location, the second location, and the first flow conductance tuning surface are all in an annular zone centered on the first region and having an inner diameter of 290 mm and an outer diameter of 310 mm, and wherein the first distance is between 10% and 20% of a second distance representing a gap through which process gas flows out of a processing region at the first location, and with the second distance being measured in the direction perpendicular to, and toward, the wafer support plane.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] Reference to the following Figures is made in the discussion below; the Figures are not intended to be limiting in scope and are simply provided to facilitate the discussion below.

[0026] FIGS. 1A and 1B depict schematics of example semiconductor processing tools of different configurations in which the gas distribution system disclosed herein may be used, according to some implementations.

[0027] FIG. 2 depicts a schematic of a first surface of the gas distribution system facing the exposed side of the semiconductor wafer to be processed, according to some implementations.

[0028] FIGS. 3A–3H depict schematics of different cross-sectional profile configurations of a flow conductance tuning surface configured to modulate the process gases distributed by the gas distribution system, according to some implementations.

[0029] FIGS. 4A and 4B illustrate example distributions of the flow conductance tuning surface with respect to the first surface of the gas distribution system facing the exposed side of the semiconductor wafer to be processed, according to some implementations.

[0030] FIG. 5A presents simulation results illustrating the effects of the gas distribution system, according to some implementations.

[0031] FIG. 5B presents example data illustrating the effects of the gas distribution system, according to some implementations.

[0032] FIG. 6 shows a schematic of an example processing system that may be used to perform the methods described herein, according to some implementations.

[0033] The above-described Figures are provided to facilitate understanding of the concepts discussed in this disclosure and are intended to be illustrative of some implementations that fall within the scope of this disclosure but are not intended to be limiting—implementations consistent with this disclosure and which are not depicted in the Figures are still considered to be within the scope of this disclosure.

[0034] Like reference symbols in the various drawings indicate like elements in accordance with certain example implementations. For example, an element 110 in different implementations may be indicated as 110A, 110B, 110C, or 110-1, 110-2, 110-3, etc. When referring to such an element using only the first number, any instance of the element is to be understood (e.g., element 110 in the previous example would refer to elements 110A, 110B, 110C, or 110-1, 110-2, 110-3).

DETAILED DESCRIPTION

[0035] As discussed above, semiconductor wafer processing operations are often performed on semiconductor wafers while such wafers are supported within a processing chamber on a pedestal or wafer support, e.g., a structure typically designed to support a semiconductor wafer. Process gas(es) are usually flowed through ports located on the side of the gas distribution system facing a semiconductor wafer to be processed (e.g., a first surface of the gas distribution system, such as an underside of a showerhead in a frontside deposition system or a top side of a shower-pedestal in a backside deposition system), and then be distributed across the semiconductor wafer.

[0036] In chemical vapor deposition (CVD) processing operations, non-uniformities in edge thickness may occur on semiconductor wafers, particularly close to the periphery of the wafer. These non-uniformities can be attributed, at least in part, to the flow of process gas, which may, due to increasing diffusivity of the process gas towards the wafer edge, cause a decrease in the film deposition rate toward the wafer's edge. For example, instead of maintaining a consistent thickness up to the edge, the gas distribution systems in existing CVD tools often produce films that see a significant reduction in thickness near the wafer's edge. Such non-uniformities can adversely affect the yield of semiconductor wafer production (e.g., the outer 1 cm of the wafer (representing 13% of the total wafer area on one side of the wafer) may see decreased deposition thickness that may make patterning in this region unusable, thereby potentially reducing the wafer yield by some amount, e.g., potentially 13% or more).

[0037] Disclosed herein are gas distribution systems that may provide enhanced tunability of gas flow across the surface of a wafer and are configured to increase the film deposition rate at the wafer edge in CVD processing tools and other contexts. The gas distribution system designs may incorporate flow conductance tuning surface(s) that are offset from a predetermined region on the first surface of the gas distribution system by a predetermined amount. The flow conductance tuning surfaces may be positioned adjacent to the first surface of the gas distribution system and may be located a distance of between $\pm 8\%$, $\pm 5\%$, or, in some implementations, $\pm 3.5\%$ of the wafer radius from the wafer edge when the wafer is present. It was found that the effect of processing gas flow modulation on wafer edge uniformity may diminish with increasing distance of the flow conductance tuning surface(s) from the wafer edge. Positioning the flow conductance tuning surface(s) within $\pm 3.5\%$ of the wafer radius from the wafer edge was found to offer noticeable benefits in edge uniformity tuning, although the effect may also exist—although perhaps to a lesser degree—at distances that are within $\pm 5\%$ or $\pm 8\%$ of the wafer radius from the wafer edge. The flow conductance tuning surfaces have a height that is between 10% and 20% of the gap distance between the first surface of the gas distribution system and the face of the wafer facing toward the flow conductance tuning surface(s) (as discussed below, the gap distance may be defined slightly different in backside deposition systems where carrier rings are used). Flow conductance tuning surfaces having such dimensional and positional characteristics were found to have a beneficial effect in terms of allowing the edge uniformity of the wafer processing operations to be modulated or controlled, thereby giving the tool operator the ability to compensate for edge non-uniformities that might arise from process irregularities, chamber irregularities, etc. The flow conductance tuning surface may be used to modulate process gas distribution, effectively "pushing" the gas flow more toward the wafer's edge, which in turn increases density of such gas near wafer edge and increases the deposition thickness at the edge of the semiconductor wafer.

[0038] Moreover, in plasma-enhanced chemical vapor deposition (PECVD) processes, radio frequency (RF) power may be applied to a process gas or gases in order to generate a plasma used to deposit layers onto the wafer. It was found that the flow conductance tuning surface configurations disclosed herein may modulate the distribution of the process gas in a desired way while having a negligible effect on plasma formation/generation.

[0039] **FIGS. 1A and 1B** depict schematics of example semiconductor processing tools of different configurations in which the gas distribution system disclosed herein may be used, according to some implementations. For example, FIG. 1A depicts a schematic of an example semiconductor processing tool 100 with a frontside configuration, configured to process the

“front” side of a wafer, which is generally considered to be the surface of the wafer facing upwards during processing and having active device layers. The semiconductor processing tool 100 may include a semiconductor processing chamber 105 that includes an interior volume that houses one or more semiconductor processing stations 115 for frontside processing. Each semiconductor processing station 115 may include a wafer support, such as a pedestal 120, that may be used to support a wafer 130 (e.g., a semiconductor wafer or wafer that is to be processed).

[0040] In some implementations, the wafer 130, which may have a diameter of 300 mm, may have a front side 130A facing a showerhead assembly 140 and a back side 130B that, when the wafer 130 is being supported by the pedestal 120, coincides with a wafer support plane 120-1 defined by the pedestal 120. The wafer 130 may be processed within the semiconductor processing chamber 105 underneath a gas distribution system, such as the showerhead assembly 140. In some implementations, the showerhead assembly 140 may be configured to distribute gases over the surface of the wafer 130, such as the front side 130A from a first surface 141-1 of the showerhead assembly 140 facing the front side 130A of the wafer 130 and through a plurality of gas distribution ports 108 (discussed in more detail below).

[0041] In some implementations, the semiconductor processing chamber 105 may also include one or more load ports (not shown), and each load port may be configured to allow the wafer 130 to be inserted into or withdrawn from the semiconductor processing chamber 105. The load ports may be located in a wall of the semiconductor processing chamber 105.

[0042] As another example, instead of including one or more semiconductor processing stations 115 for frontside processing, the semiconductor processing chamber 105 may include one or more processing stations 116 for backside processing. For example, FIG. 1B depicts a schematic of an example processing station 116 with a backside configuration having a shower-pedestal 121 configured to deliver process gas(es) to a “back” side of the wafer 130, which is generally considered to be the surface of the wafer facing downwards during processing. Each semiconductor processing station 116 may include the showerhead assembly 140 and the shower-pedestal 121 as well as one or more wafer support structures 138 that may be used to support the wafer 130. One or more wafer support structures 138 may be integral to the showerhead-pedestal 121 or may be standalone component replaceable and/or detachable from other components of the chamber 105, for example, the showerhead-pedestal 121. The shower-pedestal 121 may be configured to distribute one or more process gases to perform deposition on the back side (or underside) of the wafer 130 while the showerhead assembly 140 may be configured to distribute gas(es) that is or are non-reactive with the one or more process gases

across the top or front of the wafer, thereby helping to prevent migration of the one or more process gases to the top side of the wafer and encouraging deposition to only occur on the underside of the wafer. The wafer 130 may be processed within the semiconductor processing chamber 105 while positioned above the shower-pedestal 121.

[0043] In some embodiments, the semiconductor processing station 116 may include a plurality of wafer support structures 138 that may be positioned at locations around a first surface 141-2 of the shower-pedestal 121 for supporting the wafer 130. For the backside processing configuration, the wafer is typically support from the back side so as keep the front side of the wafer, on which the active layers and device patterns are formed typically, intact.

[0044] Wafer support structures, as used herein, refer to structures that are configured to have a wafer placed thereupon and to support such a wafer at an elevated location relative to the shower-pedestal, i.e., such that there is a gap between the underside of the wafer 130 which may be the side of the wafer to be processed, and the top of the shower-pedestal such as the first surface 141-2 of the shower-pedestal 121 facing the side of the wafer to be processed. The wafer support structures may be either fixed structures, e.g., static, tower-like structures that protrude from the top surface of the shower-pedestal; or static, tower-like structures that extend downward from a showerhead positioned above the shower-pedestal; or static cantilevered structures that extend radially inward from the walls of a semiconductor processing chamber; or dynamic structures, e.g., similar structures that are connected with actuators that allow such structures to be moved between different positions, at least one of which correlates with a position in which a wafer may be supported thereby such that the gap exists between the underside of the wafer and the top side of the shower-pedestal.

[0045] The wafer support structures 138 define a wafer support plane 120-1, defined by the portion of the wafer support structures 138 contacting the underside of the wafer 130, such that when the wafer 130 is supported by the wafer support 138, the locations where the underside 130B of the wafer 130 contacts the wafer support plane 120-1 coincident with the wafer support plane 120-1.

[0046] In some implementations, the wafer support structures 138 may include or be used with carrier rings to support the wafer 130 over the shower-pedestal 121 to form the gap between the underside of the wafer 130 such as the back side 130B and the first surface 141-2 of the shower-pedestal 121. When positioned, the carrier rings contact the underside of the wafer 130, e.g., along an annular region extending radially inward from the wafer edge which rests on a corresponding annular region of the carrier ring, or at multiple smaller regions that rest on tabs that extend radially inward from the inner perimeter of the carrier ring. In either case, the

surfaces that the wafer 130 rests on make planar contact with the underside of the wafer 130. As will be disclosed in detail below, in systems where the carrier rings are included, the gap for the process gas flow (e.g., a second distance) may be defined as a distance between the first surface 141-2 of the shower-pedestal 121 and an underside of the regions of the carrier ring that the wafer 130 rests on (e.g., a distance 305' in FIG. 3A, described in more detail below).

[0047] As shown in FIGS. 1A and 1B, the gas distribution system (e.g., the showerhead assembly 140 or shower-pedestal 121, configured for distributing process gas(es)) houses a plenum 110 and the plurality of gas distribution ports 108 that extend from the first surface 141 of the gas distribution system (e.g., the first surface 141-1 of the showerhead assembly 140 or the first surface 141-2 of the shower-pedestal 121) to the plenum 110. The gas distribution ports 108 may fluidically connect the plenum 110 with a processing region located in between the first surface 141 and, when present, the surface of the wafer 130 that faces the corresponding first surface.

[0048] Gas distribution ports, as the term is used herein, refer to small ports, orifices, holes, or openings in a shower-pedestal or showerhead, depending on the context, through which gases may exit the shower-pedestal or showerhead, as appropriate, after being provided to the shower-pedestal or showerhead via a gas inlet or gas inlets. A large number of gas distribution ports, e.g., dozens, hundreds, or, in some cases, thousands, may be distributed across the surface of a shower-pedestal or showerhead that faces toward a wafer (e.g., the first surface 141, such as the first surface 141-1 of the showerhead assembly 140 or the first surface 141-2 of the shower-pedestal 121) so as to deliver process gases to the wafer in a desired manner. During semiconductor processing operations, the first plenum 110 may be provided one or more process gases via a gas inlet 112, which is fluidically connected to one or more process and/or non-reactive gases. In some implementations, the shower-pedestal or showerhead may be a multi-plenum system, with different gases being delivered by different sets of ports and internal plenums within the shower-pedestal or showerhead.

[0049] In some implementations, the pedestal 120, the showerhead assembly 140, and/or the shower-pedestal 121 may be positioned in different configurations for different processing operations, such as with different sizes of processing regions, defined by the gap between the side of the wafer 130 to be processed and the first surface 141 of the gas distribution system (e.g., the showerhead assembly 140 or the shower-pedestal 121). The relative positioning of the pedestal 120, the showerhead assembly 140, and/or the shower-pedestal 121 in accordance with the configurations disclosed herein, may be caused/controlled by the controller (will be discussed in detail below).

[0050] FIG. 2 depicts a schematic of the first surface 141 of the gas distribution system 200 facing the exposed side of the semiconductor wafer to be processed, according to some implementations. The gas distribution system 200 may correspond to the showerhead assembly 140 or the shower-pedestal 121 in FIGS. 1A and 1B. The first surface 141 of the gas distribution system 200 may correspond to the first surface 141-1 of the showerhead assembly 140 or the first surface 141-2 of shower-pedestal 121 in FIGS. 1A and 1B. As shown in FIG. 2, a first region 204 may define a region within which the gas distribution ports 108 are distributed. An annular zone 210 defined by an inner circle 210-1 and an outer circle 210-2 represents a region where the flow conductance tuning surface(s) may be located within. The annular zone 210 may share the same central axis with the first region 204.

[0051] As noted above, a large number of gas distribution ports 108, e.g., dozens, hundreds, or, in some cases, thousands, of gas distribution ports may be distributed across the first surface 141 throughout the first region 204 so as to deliver process gases to the wafer (not shown) in a desired manner during processing operations. Although the gas distribution ports 108 are shown to be sized and distributed uniformly in Fig. 2 as an example, the size and/or distribution of the gas distribution ports 108 may not be uniform across the first surface 141 of the gas distribution system 200 and be designed to be optimized for the target operations. Although as shown in the example implementations that the first region 204 has a substantially 300 mm diameter for processing 300 mm wafers, implementations are not limited thereto. The first region 204 may have various other suitable diameters for enabling a uniform (or substantially uniform) amount of gas flow over the wafers.

[0052] To increase the thickness of deposition along the semiconductor wafer edge, the gas distribution system 200 may include flow conductance tuning surface(s) that modulate the distribution of the process gas in the vicinity of the wafer edge. For example, the flow conductance tuning surface(s) may "push" the process gas flow toward the semiconductor wafer edge and thereby increasing the local density (and thus deposition rate) of the process gas near the wafer edge. The flow conductance tuning surface(s) may be located within the annular zone 210 centered on the first region 204. For systems that process 300 mm wafers, for example, the annular zone 210 may have an inner diameter of 290 mm and an outer diameter of 310 mm (e.g., approximately $\pm 3.5\%$ of the wafer radius for a 300mm wafer). That said, in some implementations, the flow conductance tuning surface(s) (e.g., both the first and the second locations) may overlap with the wafer support (e.g., the pedestal 120 in front-side deposition systems) when viewed along an axis normal to the wafer support plane (e.g., the wafer support plane 120-1, along z-axis).

[0053] FIGS. 3A-3H depict schematics of different cross-section profile configurations of a flow conductance tuning surface configured to modulate the process gases distributed by the gas distribution system, according to some implementations.

[0054] For example, as shown in FIG. 3A, the flow conductance tuning surface may have a profile that spans between a first location 301 on or adjacent to the first surface 141 and a second location 302 offset from the first location 301 by a first distance 306 (e.g., a height) in a direction perpendicular to, and toward, the wafer 130, along z-axis in FIGS. 2 and 3A. The first location 301 and the second location 302 are, as with the flow conductance tuning surface(s), within the annular zone 210. As will be discussed in detail below, the first flow conductance tuning surface 300 may have different cross-section profile configurations, and the first distance 306 may be between 10% and 20% of the process gas flow gap between the side of the wafer to be processed such as the side facing the first surface 141 and the first surface 141, approximate to a distance between the first location of the first surface 141 and the wafer support plane 120-1 (discussed with respect to FIGS. 1A and 1B), in the direction perpendicular to, and toward, the wafer support plane 120-1, along z-axis in FIG. 2 during the processing operation that the gas distribution system 200 performs.

[0055] In some implementations, as noted above, if carrier rings are used to support the wafer 130, the gap and or the second distance 305' may instead be measured as distance between the first surface 141 and an underside of the carrier ring. For example, if the wafer support structure shown in FIG. 3A include carrier rings 324, when positioned, the carrier rings 324 contact the underside of the wafer 130, e.g., along an annular region extending radially inward from the wafer edge which rests on a corresponding annular region such as a notch 358 of the carrier ring 324, or at multiple smaller regions that rest on tabs that extend radially inward from the inner perimeter of the carrier ring 324. In either case, the surfaces that the wafer 130 rests on make planar contact with the underside such as the back side 130B of the wafer 130. In systems where the carrier rings 324 are included, the gap for the process gas flow (e.g., the second distance) may be defined as a distance between the first surface 141-2 of the shower-pedestal 121 and an underside such as underside 324B of the regions of the carrier ring that the wafer 130 rests on (e.g., the second distance 305'). In backside deposition systems in which a carrier ring 324 is not used, the wafer 130 may instead rest directly on supports extending up from the shower-pedestal and the second distance 305' may be evaluated between the underside of the wafer 130 and the first surface 141-2.

[0056] As shown in FIG. 3A, in some implementations, the first flow conductance tuning surface 300 may feature a wall-like cross-sectional profile, perpendicular to the first region

204. In this configuration, the first location 301 and the second location 302 may have the same radial distance from a center axis 303 of the gas distribution system 200.

[0057] Additionally or alternatively, according to the configurations shown in FIGS. 3B–3E, the second location 302 may be further from or closer to (not shown) the center axis 303 of the gas distribution system than the first location 301. Additionally or alternatively, according to the configurations shown in FIG. 3C–3E, the first flow conductance tuning surface 300 may feature a non-linear cross-section profile.

[0058] Specifically, as shown in FIG. 3B, the cross-section profile of the first flow conductance tuning surface 300B may feature a wall with a slope such as a 30-degree, 45-degree, 60-degree, etc. slope to the first region 204. For example, an angle 309 between the first flow conductance tuning surface 300B and the first surface 141 may be about 30-degree.

[0059] As shown in FIG. 3C, the cross-section profile of the first flow conductance tuning surface 300C may feature a convex curved portion, such as a portion curving away from the center axis 303 and with a decreasing slope with respect to the first surface 141 with increasing distance from the first surface 141.

[0060] As shown in FIG. 3D, the cross-section profile of the first flow conductance tuning surface 300D may feature a concave curved portion, such as a portion curving towards the center axis 303 and with increasing slope with respect to the first surface 141 with increasing distance from the first surface 141..

[0061] As shown in FIG. 3E, the cross-section profile of the first flow conductance tuning surface 300E may feature a curved portion having a concave curved surface oriented towards the center axis adjacent to the first surface 141 and a convex curved surface oriented towards the center axis above the concave curved surface. For example, the curved portion may have a first curved portion adjacent to the first region 204 and tangent to the first surface 141 at the first location 301E and a second curved portion tangent a surface 320E parallel to the wafer support plane (not shown) at the second location 302E.

[0062] It is appreciated that in any of the configurations disclosed herein, the transition at the first location 301 and the second location 302 may be rounded.

[0063] It is noted that, although FIGS. 3A–3E show the first location 301 and the second location 302 connected by the first flow conductance tuning surface 300 (where the first flow conductance tuning surface 300 contacts the first surface 141 at the first location 301), there may be instances where the first flow conductance tuning surface 300 is separated from the first surface 141. For example, there may be a gap between the first flow conductance tuning surface 300 and the first surface 141. For example, as illustrated in FIG. 3F, the first flow

conductance tuning surface 300F may be separated from the first surface 141 by a gap of 310, e.g., the first location 301F is proximate to, but not on, the first surface 141. For ease of illustration, the implementations where the first flow conductance tuning surface 300 and the first surface 141 are separated will not be discussed in detail.

[0064] Generally speaking, the flow conductance tuning surfaces discussed herein may be provided by features that are contiguous elements of the showerhead or shower-pedestal that they are used in conjunction with or may be provided by features on components that are separate from the showerhead or shower-pedestal with which they are used, e.g., the flow conductance tuning surface(s) may be part of rings or ring segments that are installed onto, or adjacent to, the showerhead or shower-pedestal that the flow conductance tuning surface(s) are used with. Additionally or alternatively, the flow conductance tuning surface(s) may also have non-ring shapes that produce a varying flow resistance to tune out a corresponding asymmetry in wafer deposition thickness uniformity.

[0065] In some implementations, as shown in FIG. 3G, the gas distribution system (e.g., the shower-pedestal 121) may have a first surface 141-2 that is not planar, e.g., in which the first region 204 may be non-planar and may bulge towards the wafer support plane 120-1 that coincides with the side of the wafer 130 to be processed when the wafer 130 is present (e.g., the first surface 141 and the wafer support plane 120-1 are not parallel.). As noted above, the first flow conductance tuning surface 300 may or may not connect to the first surface 141 at the first location 301 (e.g., may or may not have a gap 310 as shown in FIG. 3F). Similar to previously discussed, in this configuration, the first distance 306 may be between 10% and 20% of the distance such as the second distance 305 from the first location 301 to the side of the wafer 130 to be processed such as the side facing the first surface 141-2 in a direction perpendicular to, and toward, the wafer support plane 120-1. Also as noted above, in situations where carrier rings are used, the second distance 305' may instead be measured as a distance between the first location 301 and an underside of the carrier ring.

[0066] It is understood that while the examples in FIGS. 3A–3G show the backside deposition systems, the concepts/implementations discussed herein may be similarly applied to frontside deposition systems and/or the systems that perform both the frontside and backside depositions. For example, as shown in FIG. 3H, the first location 301, the second location 302, and the first flow conductance tuning surface 300 may all be within the annular zone 210 centered on the first region 204. The first flow conductance tuning surface 300 may span between the first location 301 and the second location 302. The second location 302 may be offset from the first location 301 by a first distance 306 in a direction perpendicular to, and toward, the wafer 130,

along z-axis. The first distance 306 such as the height of the first flow conductance tuning surface 300 may be between 10% and 20% of the gap between the side of the wafer to be processed such as the side facing the first surface 141; coincides with the wafer support plane 120-1, and the first surface 141, such as the second distance 305.

[0067] To achieve various gas flow modulation effects, such as adjusting wafer edge thickness uniformly around the entire wafer, uniformly at selected wafer locations, or by different amounts at different wafer locations, the gas distribution system 200 may include flow conductance tuning surfaces with different configurations. For instance, as shown in **FIG. 4A**, the first flow conductance tuning surface 300 may be provided as part of a ring 410 that encircles the entire first region 204. In other words, the first flow conductance tuning surface 300 could form a complete circle such as the ring 410 centered on the first region 204, designed to uniformly adjust or correct the wafer edge thickness around the entire wafer.

[0068] In some implementations, as shown in **FIG. 4B**, the first flow conductance tuning surface 300 may be provided by a portion of a ring that extends around all of the first region 204, such as a ring segment 420-1, and the gas distribution system 200 may feature more than one flow conductance tuning surface. For example, the gas distribution system 200 may feature a second and a third flow conductance tuning surfaces, provided by the ring segments 420-2 and 420-3 respectively. In some embodiments, the second and/or the third flow conductance tuning surfaces may feature the same cross-section profile configuration as the first flow conductance tuning surface 300, or the second and/or the third flow conductance tuning surfaces may feature any of the cross-section profile configurations discussed herein. In other words, the flow conductance tuning surfaces provided by ring segments 420-1, 420-2, and 420-3 may be configured as needed to correct wafer edge thickness at selected locations of the wafer uniformly, as if those different locations along the wafer edge have different levels of non-uniformity. For one specific example, because of the presence of the transfer device (e.g., the load port configured to allow the wafer to be inserted into or withdrawn from the semiconductor processing chamber), the process gas may be influenced such that a sector facing the transfer device corresponding to the ring segment 420-3, sectors next to the transfer device corresponding to the ring segments 420-1 and 420-2, and the sector corresponding to the transfer device may experience density of such gas near wafer edge differently. Therefore, to enhance the uniformity of wafer edge, the third flow conductance tuning surface may have a different height, cross-section profile configuration, and/or corresponding central angle than the first flow conductance tuning surface 300 and/or the second flow conductance tuning surface provided by ring segments 420-2. In some embodiments, although not shown, the ring

segments providing the first, second, and third flow conductance tuning surfaces may not be subject to a same ring. That said, the first, second, and third flow conductance tuning surfaces may be located at different distances away from a central axis of the first region 204.

[0069] Additionally or alternatively, the more than one flow conductance tuning surface may be offset from the first region 204 by different amounts measured along the z-axis such as with different height; spanning between third and fourth locations, with the fourth location offset from the third location by a distance different from the first distance and may be configured to adjust the wafer edge thickness differently at selected locations on the wafer. For example, a wafer that has a first level of decreased film thickness at the wafer edge in a first sector corresponding to the ring segment 420-1 and a second level of decreased film thickness at the wafer edge in a second sector corresponding to the ring segment 420-2 and with second level being greater than the first level might have a first flow conductance tuning surface in the first sector that is lower in height than a second flow conductance tuning surface in the second sector. As a result, the second flow conductance tuning surface with the greater height may cause more deposition than the first flow conductance tuning surface near the wafer edge, thereby bringing the two sectors of the wafer edge into alignment with regard to deposition thickness.

[0070] **FIG. 5A** presents simulation results illustrating the effects of the gas distribution system, according to some implementations. The arrow surface represents a cross-sectional view of a backside deposition system, where the x-axis denotes length, and the y-axis denotes height. The absolute value of the y axis is omitted. Graph 501 illustrates a simulation result of gas flow modulation of a gas distribution system with a wall-like first flow conductance tuning surface 300 (e.g., the first flow conductance tuning surface configuration shown in FIG. 3A). As illustrated in graph 501, the gas flux at the circled portion 502 is enhanced due to the first flow conductance tuning surface 300. The first flow conductance tuning surface 300 “pushes” the process gases toward the edge of wafer 130, as indicated by the arrows representing the gas flux at portion 502. These arrows now point towards the edge of the wafer rather than pointing out of the processing region, which would be the case if the first flow conductance tuning surface 300 were not used. Thus, using the first flow conductance tuning surface 300 results in a greater amount of process gases reaching the edge of the wafer 130.

[0071] **FIG. 5B** presents example data illustrating the effects of the gas distribution system in certain implementations. Graph 503 compares normalized thickness after the deposition across various positions of a 300 mm wafer, highlighting the impact of process gas modulations using flow conductance tuning surfaces such as are discussed herein. Line 504 shows data from the

system that does not implement the flow conductance tuning surface discussed herein, line 505 shows data from the same system and process conditions but with a flow conductance tuning surface having a height of 5 mm (e.g., offset from a predetermined region on the first surface of the gas distribution system by 5 mm), and line 506 shows data from the same system and process conditions but with a flow conductance tuning surface having a height of 8 mm (e.g., offset from a predetermined region on the first surface of the gas distribution system by 8 mm). [Add that for 505 and 506, same profile/shape of the surface is used, except the height, if that's the case.] As seen in graph 503, all lines show a stable normalized thickness about 1.00 between 135 mm and 140 mm from the wafer center (and, while not shown, between the wafer center and 135 mm). Past this point, however, the lines diverge: line 504 demonstrates a significant decrease in thickness, falling below 0.9 near the 147 mm mark, indicating a significant reduced edge thickness when the process gas modulation by the flow conductance tuning surface is not applied. In contrast, lines 505 and 506 maintain more uniform thickness with flow conductance tuning surfaces (e.g., for the system with 5 mm height flow conductance tuning surfaces, the wafer thickness is still about 1 at 147 mm, and for the system with 8 mm height flow conductance tuning surfaces, the wafer thickness is slightly greater than 1 at 147 mm), indicating that the process gas modulation disclosed herein helps enhance or maintain edge thickness at the wafer's periphery.

[0072] It is noted that while the above examples have focused on deposition, similar uniformity benefits may also be obtained in the context of other semiconductor processing operations, such as etching operations and that the concepts discussed herein can be implemented in etch tools as well. It is appreciated that for the gas flow modulation purposes disclosed herein, the flow conductance tuning surface, or the structures providing such surfaces, may be made using any suitable materials, such as aluminum or its alloys, ceramics such as aluminum nitride (AlN) or aluminum oxide (Al₂O₃), yttrium-based materials like Y₂O₃, or SiC-based materials.

[0073] It is also noted that the first distance and/or the second distance are for a particular processing configuration, and that those distances may change during wafer load/unload operations. As will be appreciated, a controller as discussed herein may be configured to move the pedestal, the showerhead, and/or the showerhead-pedestal to a particular configuration during processing. The first and or the second distance may be defined with respect to such a configuration.

[0074] **FIG. 6** is a schematic of a processing system suitable for conducting deposition processes, such as frontside or backside deposition processes, in accordance with embodiments. The system 600 includes a transfer module 603. The transfer module 603

provides a clean, pressurized environment to minimize risk of contamination of substrates being processed as they are moved between various reactor modules. Mounted on the transfer module 603 is a multi-station reactor 609 capable of performing ALD, treatment, and CVD according to various embodiments. Multi-station reactor 609 may include multiple stations 611, 613, 615, and 617 that may sequentially perform operations in accordance with disclosed embodiments. Stations may include a heated pedestal or substrate support, one or more gas inlets or showerhead or dispersion plate.

[0075] Mounted on the transfer module 603 may be one or more single or multi-station modules 607 capable of performing plasma or chemical (non-plasma) pre-cleans, other deposition operations, or etch operations. The module may also be used for various treatments to, for example, prepare a substrate for a deposition process. The system 600 also includes one or more wafer source modules 601, where wafers are stored before and after processing. An atmospheric robot (not shown) in the atmospheric transfer chamber 619 may first remove wafers from the wafer source modules 601 to loadlocks 621. A wafer transfer device (generally a robot arm unit) in the transfer module 603 moves the wafers from loadlocks 621 to and among the modules mounted on the transfer module 603.

[0076] In various embodiments, a system controller 642 is employed to control process conditions during deposition. The system controller 642 will typically include one or more memory devices and one or more processors. A processor may include a CPU or computer, analog and/or digital input/output connections, stepper motor controller boards, etc.

[0077] The system controller 642 may control all the activities of the deposition apparatus. The system controller 642 executes system control software, including sets of instructions for controlling the timing, mixture of gases, chamber pressure, chamber temperature, wafer temperature, radio frequency (RF) power levels, wafer chuck or pedestal position, and other parameters of a particular process. Other computer programs stored on memory devices associated with the system controller 642 may be employed in some embodiments.

[0078] The depicted embodiment includes a user interface associated with the system controller 642. The user interface may include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices such as pointing devices, keyboards, touch screens, microphones, etc.

[0079] System control logic may be configured in any suitable way. In general, the logic can be designed or configured in hardware and/or software. The instructions for controlling the drive circuitry may be hard coded or provided as software. The instructions may be provided by "programming." Such programming is understood to include logic of any form, including

hard coded logic in digital signal processors, application-specific integrated circuits, and other devices which have specific algorithms implemented as hardware. Programming is also understood to include software or firmware instructions that may be executed on a general-purpose processor. System control software may be coded in any suitable computer readable programming language.

[0080] The computer program code for controlling the processes in a process sequence can be written in any conventional computer readable programming language: for example, assembly language, C, C++, Pascal, Fortran, or others. Compiled object code or script is executed by the processor to perform the tasks identified in the program. Also as indicated, the program code may be hard coded.

[0081] The controller parameters relate to process conditions, such as, for example, process gas composition and flow rates, temperature, pressure, cooling gas pressure, substrate temperature, and chamber wall temperature. These parameters are provided to the user in the form of a recipe and may be entered utilizing the user interface.

[0082] Signals for monitoring the process may be provided by analog and/or digital input connections of the system controller 642. The signals for controlling the process are output on the analog and digital output connections of the system 600.

[0083] The system software may be designed or configured in different ways. For example, various chamber component subroutines or control objects may be written to control operation of the chamber components necessary to carry out the deposition processes in accordance with the disclosed embodiments. Examples of programs or sections of programs for this purpose include substrate positioning code, process gas control code, pressure control code, and heater control code.

[0084] In some implementations, a system controller 642 is part of a system, which may be part of the above-described examples. Such systems can include semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be referred to as the "controller," which may control various components or subparts of the system or systems. The system controller 642, depending on the processing requirements and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of process gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings in some

systems, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

System Controllers

[0085] Semiconductor processing tools having gas distribution systems that may provide enhanced tunability of gas flow across the surface of a wafer such as those discussed above may also include, or be connected with, a controller that may be configured to control various functionalities associated with such semiconductor processing tools. The controller, depending on the processing requirements and/or the type of system, may be programmed to control any of the processes disclosed herein, such as processes for controlling the flow of coolant (or heating fluid) through the pedestal and/or electrical power through the resistive heater element, as well as other processes or parameters not discussed herein, such as the delivery of process gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a chamber and other transfer tools and/or load locks connected to or interfaced with a specific system.

[0086] Broadly speaking, the controller may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operations, enable cleaning operations, enable endpoint measurements, and the like. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application-specific integrated circuits (ASICs), and/or one or more microprocessors or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some examples, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

[0087] The controller, in some implementations, may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, the controller may be in the "cloud" or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The

computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g., a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control. Thus, as described above, the controller may be distributed, such as by comprising one or more discrete controllers that are networked together and working toward a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0088] Without limitation, example pedestal assemblies according to the present disclosure may be mounted in or part of semiconductor processing tools with a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a chemical vapor deposition (CVD) chamber or module, an ALD chamber or module, an ALE chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0089] As noted above, depending on the process step or steps to be performed by the tool, the controller might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0090] The use, if any, of ordinal indicators, e.g., (a), (b), (c)... or (1), (2), (3)... or the like, in this disclosure and claims is to be understood as not conveying any particular order or sequence, except to the extent that such an order or sequence is explicitly indicated. For example, if there are three steps labeled (i), (ii), and (iii), it is to be understood that these steps may be performed in any order (or even concurrently, if not otherwise contraindicated) unless indicated otherwise. For example, if step (ii) involves the handling of an element that is created in step (i), then step (ii) may be viewed as happening at some point after step (i). Similarly, if step (i) involves the handling of an element that is created in step (ii), the reverse is to be understood. It is also to be understood that use of the ordinal indicator "first" herein, e.g., "a first item," should not be read as suggesting, implicitly or inherently, that there is necessarily a "second" instance, e.g., "a second item."

[0091] It is to be understood that the phrases "for each <item> of the one or more <items>," "each <item> of the one or more <items>," or the like, if used herein, are inclusive of both a single-item group and multiple-item groups, i.e., the phrase "for ... each" is used in the sense that it is used in programming languages to refer to each item of whatever population of items is referenced. For example, if the population of items referenced is a single item, then "each" would refer to only that single item (despite the fact that dictionary definitions of "each" frequently define the term to refer to "every one of two or more things") and would not imply that there must be at least two of those items. Similarly, the term "set" or "subset" should not be viewed, in itself, as necessarily encompassing a plurality of items—it will be understood that a set or a subset can encompass only one member or multiple members (unless the context indicates otherwise).

[0092] The term "between," as used herein and when used with a range of values, is to be understood, unless otherwise indicated, as being inclusive of the start and end values of that range. For example, between 1 and 5 is to be understood to be inclusive of the numbers 1, 2, 3, 4, and 5, not just the numbers 2, 3, and 4.

[0093] The term "operatively connected" is to be understood to refer to a state in which two components and/or systems are connected, either directly or indirectly, such that, for example, at least one component or system can control the other. For example, a controller may be described as being operatively connected with a resistive heating unit, which is inclusive of the controller being connected with a sub-controller of the resistive heating unit that is electrically connected with a relay that is configured to controllably connect or disconnect the resistive heating unit with a power source that is capable of providing an amount of power that is able to power the resistive heating unit so as to generate a desired degree of heating. The controller

itself likely cannot supply such power directly to the resistive heating unit due to the currents involved, but it will be understood that the controller is nonetheless operatively connected with the resistive heating unit.

[0094] For the purposes of this disclosure, the term "fluidically connected" is used with respect to volumes, plenums, holes, etc., that may be connected with one another, either directly or via one or more intervening components or volumes, in order to form a fluidic connection, similar to how the term "electrically connected" is used with respect to components that are connected together to form an electric connection. In the context of the first and second passage segments discussed in this application, however, it will be understood that when reference is made to such a passage segment fluidically connecting with other passage segments, such fluidic connections are to be understood to be direct couplings between such passage segments, e.g., the end of such a passage segment is directly connected to the ends of the other passage segments (as opposed to being connected with such other passage segments via one or more other intervening passage segments). The term "fluidically interposed," if used, may be used to refer to a component, volume, plenum, or hole that is fluidically connected with at least two other components, volumes, plenums, or holes such that fluid flowing from one of those other components, volumes, plenums, or holes to the other or another of those components, volumes, plenums, or holes would first flow through the "fluidically interposed" component before reaching that other or another of those components, volumes, plenums, or holes. For example, if a pump is fluidically interposed between a reservoir and an outlet, fluid that flowed from the reservoir to the outlet would first flow through the pump before reaching the outlet. The term "fluidically adjacent," if used, refers to placement of a fluidic element relative to another fluidic element such that there are no potential structures fluidically interposed between the two elements that might potentially interrupt fluid flow between the two fluidic elements. For example, in a flow path having a first valve, a second valve, and a third valve placed sequentially therealong, the first valve would be fluidically adjacent to the second valve, the second valve fluidically adjacent to both the first and third valves, and the third valve fluidically adjacent to the second valve.

[0095] It is understood that the examples and implementations described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art. Although various details have been omitted for clarity's sake, various design alternatives may be implemented. Therefore, the present examples are to be considered as illustrative and not restrictive, and the disclosure is not to be limited to the details given herein but may be modified within the scope of the disclosure.

[0096] It is to be understood that the above disclosure, while focusing on a particular example implementation or implementations, is not limited to only the discussed example, but may also apply to similar variants and mechanisms as well, and such similar variants and mechanisms are also considered to be within the scope of this disclosure.

CLAIMS

What is claimed is:

1. An apparatus comprising:
 - a wafer support defining a wafer support plane and configured to support a semiconductor wafer having a diameter of 300 mm, such that when the semiconductor wafer is supported by the wafer support, an underside of the semiconductor wafer is coincident with the wafer support plane;
 - a showerhead with one or more sets of gas distribution ports distributed throughout a first region on a first side of the showerhead facing the wafer support plane when the showerhead and wafer support plane are placed in a first configuration; and
 - a first flow conductance tuning surface with a radial cross-section profile spanning between a first location on the showerhead and a second location offset from the first location by a first distance in a direction perpendicular to, and toward, the wafer support plane, wherein the first location, the second location, and the first flow conductance tuning surface are all in an annular zone centered on the first region and having an inner diameter of 290 mm and an outer diameter of 310 mm, and wherein the first distance is between 10% and 20% of a second distance representing a gap through which process gas flows out of a processing region at the first location, and with the second distance being measured in the direction perpendicular to, and toward, the wafer support plane.
2. The apparatus of claim 1, wherein the second location is further from the center axis of the showerhead than the first location.
3. The apparatus of claim 1, wherein the first location and the second location are equal in distance from the center axis of the showerhead.
4. The apparatus of claim 1, wherein the first location and second location are connected by the first flow conductance tuning surface.
5. The apparatus of claim 4, wherein the cross-section profile of the first flow conductance tuning surface is non-linear.
6. The apparatus of claim 5, wherein the cross-section profile of the first flow conductance tuning surface features at least one curved portion.

7. The apparatus of claim 6, wherein the cross-section profile of the first flow conductance tuning surface features:

a first curved portion adjacent to the first region and tangent to the showerhead at the first location; and

a second curved portion tangent to a surface parallel to the wafer support plane at the second location.

8. The apparatus of claim 4, wherein the cross-section profile of the first flow conductance tuning surface features a wall vertical to the first region.

9. The apparatus of claim 4, wherein the cross-section profile of the first flow conductance tuning surface features a wall with a 30-degree slope to the first region.

10. The apparatus of claim 1, wherein the first flow conductance tuning surface is provided by a flow conductance tuning component separate from the showerhead.

11. The apparatus of claim 1, wherein the first flow conductance tuning surface is provided by a ring that extends around all of the first region.

12. The apparatus of claim 1, wherein the first flow conductance tuning surface is provided by a ring segment that extends only partially about the first region.

13. The apparatus of claim 12, further comprising a second flow conductance tuning surface spanning between a third location on the showerhead and a fourth location offset from the third location by a third distance in a direction perpendicular to, and toward, the wafer support plane, wherein the third location, the fourth location, and the second flow conductance tuning surface are all in the annular zone centered on the first region and having an inner diameter of 290 mm and an outer diameter of 310 mm, and wherein the third distance is between 10% and 20% of a fourth distance between the third location of the showerhead and the wafer support plane in the direction perpendicular to, and toward, the wafer support plane.

14. The apparatus of claim 13, wherein the third distance is different from the first distance.

15. The apparatus of claim 1, wherein the first region is non-planar and bulges toward the wafer support plane, and wherein the first flow conductance tuning surface connects to the showerhead at the first location.

16. The apparatus of any one of claims 1 through 15, further comprising a controller configured to cause one or both of the showerhead and the wafer support to be positioned in the first configuration during at least a portion of a semiconductor processing operation in which one or more first process gases are flowed from the gas distribution ports in at least one set of the gas distribution ports, wherein, in the first configuration, the second distance is between 6 mm and 16 mm.

17. The apparatus of any one of claims 1 through 16, further comprising:
a processing chamber; and
a pedestal, wherein:
the first region of the showerhead is positioned within the processing chamber, and
the pedestal is positioned beneath the showerhead and provides the wafer support.

18. An apparatus comprising:
a wafer support defining a wafer support plane and configured to support a semiconductor wafer having a diameter of 300 mm, such that when the semiconductor wafer is supported by the wafer support, an underside of the semiconductor wafer is coincident with the wafer support plane;

a showerhead pedestal with one or more sets of gas distribution ports distributed throughout a first region on a first side of the showerhead pedestal facing the wafer support plane when the showerhead pedestal and wafer support plane are placed in a first configuration; and

a first flow conductance tuning surface spanning between a first location on the showerhead pedestal and a second location offset from the first location by a first distance in a direction perpendicular to, and toward, the wafer support plane, wherein the first location, the second location, and the first flow conductance tuning surface are all in an annular zone centered on the first region and having an inner diameter of 290 mm and an outer diameter of 310 mm, and wherein the first distance is between 10% and 20% of a second distance representing a gap through which process gas flows out of a processing region at the first

location, and with the second distance being measured in the direction perpendicular to, and toward, the wafer support plane.