What is claimed is:

1. A semiconductor package, comprising:

a first semiconductor chip including a first semiconductor substrate, a first semiconductor device layer disposed on a lower surface of the first semiconductor substrate and including a first interconnect structure, and a first through electrode that penetrates through the first semiconductor substrate and is electrically connected to the first interconnect structure;

a second semiconductor chip stacked on an upper surface of the first semiconductor chip;

an underfill material layer interposed between the first semiconductor chip and the second semiconductor chip; and

a first dam structure disposed on the upper surface of the first semiconductor chip, wherein the first dam structure extends along an edge of the second semiconductor chip and includes unit dam structures spaced apart from each other in a first direction with a slit therebetween,

wherein a vertical level of an upper surface of the first dam structure is located between a vertical level of a lower surface of the second semiconductor chip and a vertical level of an upper surface of the second semiconductor chip,

the unit dam structures of the first dam structure each have a rectangular shape in a plan view,

a first sidewall of the first dam structure is in contact with the underfill material layer and includes a flat surface parallel to a sidewall of the second semiconductor chip that faces the first sidewall of the first dam structure,

wherein a width of the slit between the unit dam structures in the first direction is equal to or less than a width of each of the unit dam structures in the first direction,

wherein the width of the slit in the first direction is 60 μm or less, and

wherein the first direction is parallel to the upper surface of the first semiconductor chip.

2. The semiconductor package of claim 1, wherein

the width of the unit dam structures of the first dam structure is between 30 μm and 150 μm.

3. The semiconductor package of claim 1 or claim 2, wherein

the first dam structure includes a metal.

4. The semiconductor package of claim 1 or claim 2, wherein

the first dam structure includes a polymer.

5. The semiconductor package of any one of claims 1 to 4, wherein

the underfill material layer comprises:

a linear sidewall in contact with the first sidewall of the first dam structure, wherein the linear sidewall extends in a direction perpendicular to the upper surface of the first semiconductor chip; and

a curvilinear sidewall connected to the linear sidewall,

wherein the curvilinear sidewall defines an indentation that extends along the edge of the second semiconductor chip.

6. The semiconductor package of claim 5, wherein

the upper surface of the first dam structure is continuously connected to the curvilinear sidewall of the underfill material layer.

7. The semiconductor package of any one of claims 1 to 6, further comprising

a molding layer disposed on the first semiconductor chip, wherein the molding layer surrounds the second semiconductor chip in a plan view.

8. The semiconductor package of claim 7, wherein

the first dam structure is exposed through a sidewall of the molding layer.

9. The semiconductor package of any one of claims 1 to 4, wherein

the first semiconductor chip comprises a trench that is filled with the underfill material layer, and

the trench of the first semiconductor chip is located between the first sidewall of the first dam structure and the edge of the second semiconductor chip.

10. The semiconductor package of any one of claims 1 to 4, wherein

the first dam structure comprises:

a first unit dam structure that has a first horizontal length in a direction parallel to the edge of the second semiconductor chip; and

a second unit dam structure having a second horizontal length greater than the first horizontal length in a direction parallel to the edge of the second semiconductor chip.

11. The semiconductor package of any one of claims 1 to 4, further comprising

a second dam structure disposed on the first semiconductor chip and spaced apart from the edge of the second semiconductor chip with the first dam structure therebetween.

12. The semiconductor package of any one of claims 1 to 11, further comprising

a plurality of semiconductor chips that are vertically stacked on the second semiconductor chip.

13. A semiconductor package, comprising:

a first semiconductor chip including a first semiconductor substrate, a first semiconductor device layer disposed on a lower surface of the first semiconductor substrate and including a first interconnect structure, and a first through electrode that penetrates through the first semiconductor substrate and is electrically connected to the first interconnect structure;

a second semiconductor chip stacked on an upper surface of the first semiconductor chip;

an underfill material layer interposed between the first semiconductor chip and the second semiconductor chip, wherein the underfill material layer covers at least a portion of a sidewall of the second semiconductor chip and includes a lower sidewall that extends linearly in a direction perpendicular to the upper surface of the first semiconductor chip and a curvilinear upper sidewall connected to the lower sidewall, and

a first dam structure disposed on the upper surface of the first semiconductor chip,

wherein the curvilinear upper sidewall of the underfill material layer defines an indentation in an outer region of the underfill material layer,

wherein the first dam structure includes unit dam structures spaced apart from each other in a first direction, and a slit that separates adjacent unit dam structures of the unit dam structures,

wherein a width of the slit between the unit dam structures in the first direction is equal to or less than a width of each of the unit dam structures in the first direction,

wherein the width of the slit in the first direction is 60 μm or less, and

wherein the first direction is parallel to the upper surface of the first semiconductor chip.

14. The semiconductor package of claim 13, wherein

the indentation of the underfill material layer extends linearly in a horizontal direction along an edge of the second semiconductor chip.

15. The semiconductor package of claim 14, wherein the first dam structure contacts the lower sidewall of the underfill material layer.

16. The semiconductor package of claim 13 or claim 14, wherein

an upper surface of the first dam structure is continuously connected to the curvilinear upper sidewall, and

a slope of the upper surface of the first dam structure is equal to a slope of the curvilinear upper sidewall at a boundary between the upper surface of the first dam structure and the curvilinear upper sidewall.

17. The semiconductor package of any one of claims 13 to 16, wherein

the first dam structure includes a plurality of bar-shaped unit dam structures that extend along an edge of the second semiconductor chip, and

a first sidewall of the first dam structure is in contact with the lower sidewall of the underfill material layer and includes a flat surface parallel to the sidewall of the second semiconductor chip that faces the first sidewall of the first dam structure.

18. The semiconductor package of any one of claims 13 to 17, wherein

the first dam structure includes a photoresist material.

19. A semiconductor package, comprising:

a first semiconductor chip that includes a first semiconductor substrate, a first semiconductor device layer disposed on a lower surface of the first semiconductor substrate and that includes a first interconnect structure, and a first through electrode that penetrates through the first semiconductor substrate and is electrically connected to the first interconnect structure;

a second semiconductor chip disposed on an upper surface of the first semiconductor chip, wherein the second semiconductor chip includes a second semiconductor substrate, a second semiconductor device layer disposed on the second semiconductor substrate and that

includes a second interconnect structure, and a second through electrode that penetrates through the second semiconductor substrate and is electrically connected to the second interconnect structure;

a connection bump interposed between the first semiconductor chip and the second semiconductor chip;

an underfill material layer interposed between the first semiconductor chip and the second semiconductor chip, wherein the underfill material layer surrounds a sidewall of the connection bump and covers at least a portion of a sidewall of the second semiconductor chip;

a first dam structure disposed on the upper surface of the first semiconductor chip, wherein the first dam structure contacts the underfill material layer, extends along an edge of the second semiconductor chip and includes a plurality of slits and a plurality of unit dam structures spaced apart from each other in a first direction by the plurality of slits; and

a molding layer disposed on the first semiconductor chip and that covers the underfill material layer and the first dam structure,

wherein the first dam structure further includes:

a first sidewall in contact with the underfill material layer and that includes a flat surface parallel to the sidewall of the second semiconductor chip; and

an upper surface located between a vertical level of a lower surface of the second semiconductor chip and a vertical level of an upper surface of the second semiconductor chip,

wherein an interval between the plurality of first unit dam structures in the first direction parallel to the edge of the second semiconductor chip is 100 % or less of a horizontal length of each of the plurality of unit dam structures in the first direction,

wherein the interval between the plurality of unit dam structures in the first direction is 60 μm or less, and

wherein the first direction is parallel to the upper surface of the first semiconductor chip.