

SOLDER COLUMN GRID ARRAY CAPACITORS

BACKGROUND

[0001] The present disclosure generally relates to electronic interconnect structures. In particular, this disclosure relates to grid array capacitors that can be attached to an integrated circuit (IC) package and to a printed circuit board (PCB).

[0002] A capacitor is a passive electrical component having at least two electrical conductors known as plates, separated by a dielectric or insulator, and which can be used to electrostatically store energy in an electric field. Capacitors can be useful as circuit elements in conjunction with a variety of types of electronic devices such as digital and analog ICs.

[0003] A decoupling capacitor can be used to decouple or electrically isolate one part of an electrical circuit or network from another part of the circuit. Electrical noise generated by certain circuit elements can be shunted through a decoupling capacitor. Decoupling capacitors can be particularly useful for shunting or bypassing high-frequency noise components around noise-sensitive circuitry such as filters, amplifiers and logic elements.

[0004] Solder columns or balls can be used to provide electrical and mechanical interconnection of an IC package to a PCB. Such solder columns can be arranged in an array formation between planar surfaces of the IC package and of the PCB. The IC package can be attached to the PCB by reflowing the solder columns to attachment pads located on the IC package and PCB surfaces.

SUMMARY

[0005] Embodiments can be directed towards a grid array capacitor located between an integrated circuit (IC) package and a printed circuit board (PCB). The grid array capacitor can be configured to be physically and electrically coupled to the IC package and to the PCB. The grid array capacitor can include an inner conductor configured to be electrically connected to the integrated circuit (IC) package and to the PCB and an inner

dielectric in a coaxial orientation to, and at least partially surrounding the inner conductor. The grid array capacitor can also include a secondary conductor in a coaxial orientation to, and at least partially surrounding the inner dielectric. The secondary conductor can be configured to be electrically connected to the IC package and to the PCB.

[0006] Embodiments can also be directed towards an electronic system. The electronic system can include a PCB, an IC package, and a grid array capacitor located between the IC package and the PCB. The grid array capacitor can be physically and electrically coupled to the IC package and to the PCB. The grid array capacitor can include an inner conductor physically and electrically connected to the IC package and to the PCB an inner dielectric in a coaxial orientation to and at least partially surrounding the inner conductor. The grid array capacitor can also include a secondary conductor in a coaxial orientation to and at least partially surrounding the inner dielectric. The secondary conductor can be physically and electrically connected to the IC package and to the PCB.

[0007] Embodiments can also be directed towards a method of manufacturing a grid array capacitor. The grid array capacitor can be located between an IC package and a PCB of an electronic system. The method can include inserting an inner dielectric into an axially-oriented opening of a secondary conductor and forming, in the inner dielectric, an opening suitable to receive an inner conductor. The method can also include inserting the inner conductor into the opening in the inner dielectric and applying solder paste to opposing ends of the secondary conductor and to opposing ends of the inner conductor. The method can also include electrically and mechanically interconnecting the grid array capacitor to an IC package and to a PCB by reflowing the solder paste applied to the opposing ends of the secondary conductor and to the inner conductor.

[0008] The above summary is not intended to describe each illustrated embodiment or every implementation of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The drawings included in the present application are incorporated into, and form part of the specification. They illustrate embodiments of the present disclosure and,

along with the description, serve to explain the principles of the disclosure. The drawings are only illustrative of certain embodiments and do not limit the disclosure.

[0010] FIG. 1 includes views depicting an electronic system and a grid array capacitor, according to embodiments of the present disclosure.

[0011] FIG. 2 depicts a grid array capacitor having a secondary conductor with two sections and a grid array capacitor having three conductors, according to embodiments of the present disclosure.

[0012] FIG. 3 includes schematic views of grid array capacitors and a graph depicting insertion loss characteristics of grid array capacitors, according to embodiments consistent with the figures.

[0013] FIG. 4 includes a flow diagram and corresponding process diagram views depicting a method for manufacturing a grid array capacitor located between an integrated circuit (IC) package and a printed circuit board (PCB), according to embodiments consistent with the figures.

[0014] While the invention is amenable to various modifications and alternative forms, specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention.

[0015] In the drawings and the Detailed Description, like numbers generally refer to like components, parts, steps, and processes.

DETAILED DESCRIPTION

[0016] Certain embodiments of the present disclosure can be appreciated in the context of providing grid array capacitors used to interconnect integrated circuit (IC) packages to printed circuit boards (PCB) within electronic equipment such as servers, which may be used to provide data to clients attached to a server through a network. Such servers may include, but are not limited to web servers, application servers, mail servers, and virtual servers. While not necessarily limited thereto, embodiments discussed in this context can facilitate an understanding of various aspects of the

disclosure. Certain embodiments may also be directed towards other equipment and associated applications, such as providing grid array capacitors used to interconnect IC packages to PCBs within electronic equipment such as computing systems, which may be used in a wide variety of computational and data processing applications. Such computing systems may include, but are not limited to, supercomputers, high-performance computing (HPC) systems, and other types of special-purpose computers. Embodiments may also be directed towards providing grid array capacitors used to interconnect IC packages to PCBs within consumer and small office/home office (SOHO) electronic equipment such as personal computers, laptops, mobile and network server devices.

[0017] The terms “attachment pad,” and “BGA (ball grid array) pad” can be used interchangeably herein in reference to a metallic pad used to form an electrical and mechanical interconnection to an IC package or a PCB. Such pads can include metals such as copper or copper alloys, and can be arranged in arrays that are positionally consistent with solder balls on a BGA electronic package. In the context of the present disclosure, attachment pads can be used as locations on which to place and reflow solder balls to electrically and mechanically interconnect an IC package to a PCB.

[0018] For ease of discussion, the terms “*solder*,” “*solder paste*” and “*solder balls*” are used generally herein in reference to an electrically conductive attachment material used to form a durable mechanical and electrical interconnection between an IC package and a PCB.

[0019] The terms “*secondary conductor*” and “*outer conductor*” are used herein in reference to electrical conductors included within a grid array capacitor. In the context of the present disclosure, it can be understood that the terms “*secondary conductor*” and “*outer conductor*” may each be used interchangeably with the term “*columnar conductive sleeve*.”

[0020] A dielectric constant (Dk), also known as the “*relative permittivity*” of a dielectric or insulating material can be understood to be the ratio of the amount of charge stored in response to an insulating material being placed between two metallic plates to the amount of charge that can be stored when the insulating material is replaced by a vacuum or by air.

[0021] ICs such as processors, graphics processing units (GPUs), memory chips and application-specific integrated circuits (ASICs) can be electrically and mechanically attached to a PCB through the use of reflowed solder columns or solder balls. Such

solder columns or balls can be arranged in an array formation, which can be particularly useful for providing a large number of high-density power and signal interconnections between an IC package and the PCB. Continuing trends of increasing IC operational frequencies and signal slew rates in conjunction with the increased use of high-speed serial (HSS) data interfaces have resulted in the need for increased power supply decoupling and AC (alternating current) coupling capacitance at IC package/PCB interfaces.

[0022] Such increased capacitance can be provided by surface-mount technology (SMT) capacitors placed on the PCB adjacent to the IC package. Placement of these additional SMT capacitors, however, may complicate the routing of wiring within a “breakout” or “escape” area on the PCB. A breakout area generally includes a large number of closely-arranged wires and BGA pads under the IC package. These wires are used to fan out the wiring to wiring regions on the PCB that have more relaxed spacing constraints.

[0023] Area for wiring within breakout regions is generally very limited, and certain signal net types, e.g., differential pairs, can require precise balancing of paired wire lengths in order for the differential signals carried on them to meet electrical design constraints. Disrupting wiring flow, e.g., by including SMT capacitors within the breakout area, can therefore cause significantly increased design complexity, and in some cases, cause critical electrical design requirements, e.g., wiring length and/or length matching, to go unmet.

[0024] According to embodiments, solder column grid array capacitors can provide additional decoupling or AC coupling capacitance at an IC package/PCB interface without disrupting wiring flow of a wiring breakout area on the PCB. The use of such small geometry capacitors can enhance PCB wiring flow, which can allow electrical design constraints to be met without excessive design or PCB wiring layout effort. The use of solder column grid array capacitors can also provide additional capacitance to ICs without additional series inductance (ESL) resulting from PCB surface wiring and/or vias. This additional capacitance can be particularly useful for decoupling IC power supply rails and for AC coupling HSS data signals.

[0025] Various aspects of the present disclosure may be useful for providing HSS and decoupling capacitance solutions within the framework of an existing columnar attach mechanism. Such solutions may not disturb sensitive PCB breakout wiring constraints. Various embodiments can eliminate the need for discrete (SMT) capacitors and the

parasitic inductive losses associated with capacitor wiring breakout. Certain embodiments can be particularly useful in providing improved insertion loss by implementing three-terminal capacitors within the framework of an existing columnar attach mechanism. Such embodiments can also include integrated signal paths.

[0026] Grid array capacitors designed according to certain embodiments may be compatible with existing and proven PCBs and IC packages may be a useful and cost-effective way to provide increased decoupling and AC coupling capacitance.

Embodiments of the present disclosure can be useful in providing a variety of interconnect topologies between a PCB and an IC package that support AC coupling, direct current (DC) connections, and power supply decoupling.

[0027] It can be understood that the elements depicted in the figures are provided for conceptual illustration only, and are not necessarily drawn to scale. For example, structures can be depicted as having rectangular cross-sectional profiles, with surfaces orthogonal to each other. This depiction, however, is not limiting; structures can be of any suitable shape, size and profile, in accordance with specific design criteria, lithographic and manufacturing process limitations and tolerances for a given application. For example, corners shown as having right angles can be rounded, surfaces can have a non-orthogonal relative orientation, and relative dimensional ratios can vary from those depicted in the figures.

[0028] Embodiments of the present disclosure can include a variety of configurations and signal paths/path types. For example, various embodiments can include solder column grid array capacitors having no DC paths, one or more DC paths, an AC path or an AC path with severed inner conductor. Embodiments can generally have a coaxial structure, e.g., including two or three electrical conductors that are electrically insulated from each other by generally cylindrical dielectric layers. This description is not limiting, however, other structures can be included within the spirit and scope of the present disclosure.

[0029] Certain embodiments relate to the use of grid array capacitors in electronic systems to electrically interconnect IC packages to PCBs. FIG. 1 includes views 100, 150 depicting side and top views, respectively, of an electronic system, views 108A, 108B depicting side and top views, respectively, of a grid array capacitor and view 110 depicting an interconnect pad, according to embodiments of the present disclosure. FIG. 1 can be particularly useful in depicting and providing an understanding of the physical structure of a grid array capacitor 108 and the placement and interconnection of an IC

package 106 to a PCB 114 through the use of multiple grid array capacitors 108. It can be understood that the views included in FIG. 1 are provided for the purpose of illustration only, and may not accurately represent dimensions, proportions, quantities or other physical features of elements such as PCBs, IC packages, ICs and grid array capacitors.

[0030] View 100 includes an IC 102 mounted with solder balls 104 onto an IC package 106. IC package 106 is attached to PCB 114 by grid array capacitors 108 located between IC package 106 and PCB 114. IC package 106 and PCB 114 both have a positionally corresponding set of interconnect pads 110 on opposing planer surfaces, consistent with interconnect pads used for solder column and solder ball interconnection of IC packages to PCBs. Such interconnect pads can include a conductive material such as copper or a copper alloy. According to embodiments, grid array capacitor ends, e.g., 116A and 116B, view 108A, are attached to interconnect pads 110 by solder 112. In embodiments, solder 112 is applied to interconnect pads 110 and reflowed to form stable electrical and mechanical connections between IC package 106, grid array capacitor 108 and PCB 114. Grid array capacitor ends 116A and 116B can be solder plated prior to reflow in order to enhance the reflow process.

[0031] In embodiments, IC 102 can be an IC such as a processor or GPU chip, IC package 106 can be a ceramic or organic multi-layer substrate, and PCB 114 can include, for example, a motherboard or daughter card. Solder balls 104 can be formed from a high-temperature solder that is reflowed in conjunction with a lower-temperature solder paste to form a bond between IC 102 and IC package 106.

[0032] View 100 can be particularly useful for depicting desirable electrical and mechanical connections of IC package 106 to PCB 114 using grid array capacitors 108. Such connections/coupling can be electrically and mechanically stable while compensating for differences in planarity of opposing surfaces of IC package 106 and PCB 114. In some applications, such planarity differences may be due to warp caused by coefficient of thermal expansion (CTE) differences between IC package 106 and PCB 114, or due to manufacturing tolerances.

[0033] The assembly depicted in view 100 can thus be understood by one of skill in the art of electrical package and/or electrical system design to be an exemplary IC package and PCB assembly. The structure of grid array capacitors 108, as depicted, is understood to generally yield electrical and mechanical connections that are robust, durable and reliable over an extended time period. Grid array capacitors 108 are

particularly useful in providing capacitance useful for IC power rail decoupling and HSS AC coupling at the IC package 106/PCB 114 interface, while not consuming excess surface area on PCB 114 in addition to area that a solder ball or solder column interconnect structure would occupy.

[0034] Electronic system top view 150, consistent with side view 100, is useful in depicting the relative positioning of PCB 114, IC package 106, IC 102 and interconnect pads 110. Views 108A and 108B depict an expanded view of a grid array capacitor 108 consistent with view 100. Grid array capacitors 108 can provide, at the IC package 106/PCB 114 interface, capacitance that is useful for decoupling IC power supplies and for AC coupling of HSS signals.

[0035] According to embodiments, grid array capacitor 108 includes an inner conductor 118 configured to be electrically connected to the IC package 106 and to the PCB 114. In some embodiments, the inner conductor 118 is a wire, and in some embodiments, the inner conductor 118 can be a helical coil. Inner dielectric 120 is positioned in a coaxial orientation to and at least partially surrounding inner conductor 118. The inner dielectric 120 can be understood to be a dielectric “plug,” and can include, for example, materials such as polyimide and/or barium titanate.

[0036] Secondary conductor 122 is in a coaxial orientation to and at least partially surrounding the inner dielectric 120. The secondary conductor 122 is configured to be electrically connected to the IC package 106 and to the PCB 114. In some embodiments, secondary conductor 122 can be a conductive helical structure or coil, as depicted in view 108A. A secondary conductor 122 that is a conductive helical structure or coil can be useful for compensating for non-uniformities in planarity and/or distance between opposing surfaces of IC package 106 and PCB 114. The use of such helical structures can provide electrical interconnections that are mechanically robust over a wide variety of thermal and dimensional variances of both IC package 106 and PCB 114.

[0037] In some embodiments, secondary conductor 122 can be a hollow, electrically conductive cylindrical structure or sleeve. Secondary conductor 122 may also be referred to as a “*columnar conductive sleeve*.” The inner conductor 118 and secondary conductor 122 can include materials such as copper, tin, nickel, niobium and titanium.

[0038] In some embodiments the inner dielectric 120 can have a Dk value between 100 and 5,000, which, in conjunction with inner conductor 118 and secondary conductor 122 can yield a grid array capacitor 108 capacitance in a range between 1 nF and 8 nF. This capacitance can be particularly useful for decoupling IC 102 power supplies and for

AC coupling of HSS signals electrically interconnected to IC 102. Future technology development may include the use of dielectric materials having Dk values greater than 5,000, which may provide for proportionally greater capacitance values of grid array capacitors.

[0039] Grid array capacitors 108 can be used to establish a variety of types of electrical interconnections between IC 102 and PCB 114. It can be understood that the inner conductor 118 and secondary conductor 122 can each be used for power, ground, or signals, as needed. Capacitances between inner conductors 118 and secondary conductors 122 can be used for power supply decoupling and/or AC coupling.

[0040] For example, a grid array capacitor 108 can form two electrical interconnect paths, e.g., a power supply voltage and ground node, between IC package 106 and PCB 114. In this example, capacitances between an inner conductor 118 and a secondary conductor 122 can be used for IC 102 power supply decoupling. In certain embodiments, at least one of inner conductor 118 and secondary conductor 122 can be left electrically disconnected from either IC package 106 or PCB 114. In some embodiments, grid array capacitor 108A can provide AC coupling between IC package 106 and PCB 114. Such AC coupling can be used in conjunction with HSS interfaces of IC 102.

[0041] View 110 depicts an interconnect pad having interconnect pad 110A positionally corresponding to inner conductor 118 and interconnect pad 110B positionally corresponding to secondary conductor 122. In embodiments, inner conductor 118 can be physically and electrically connected to interconnect pad 110A through a solder reflow operation. Secondary conductor 122 can similarly be physically and electrically connected to interconnect pad 110B.

[0001] FIG. 2 depicts, in views 108C, 108D, a grid array capacitor having a secondary conductor 122 with two sections 228A and 228B. FIG. 2 also depicts, in views 108E, 108F, a grid array capacitor having three conductors 118, 122 and 226, according to embodiments of the present disclosure. Views 108C, 108D, 108E and 108F are generally consistent with FIG. 1.

[0042] Consistent with view 108A, FIG. 1, grid array capacitor 108C includes inner conductor 118 and inner dielectric 120. Grid array capacitor 108C also includes a secondary conductor 122 (see view 108A, FIG. 1) section 228A adjacent to end 116A and section 228B adjacent to end 116B. According to embodiments, section 228A and section 228B are physically separated by gap 229 and are therefore electrically insulated

from each other; no DC connection is therefore possible between sections 228A and 228B.

[0043] According to embodiments, gap 229 can be formed by a severing of secondary conductor 122, FIG. 1, or it can be formed by the placement of two separate sections 228A, 228B. It can be understood that the inner conductor 118 can be used for power, ground, or signals, as needed. In embodiments, capacitive coupling between sections 228A and 228B of grid array capacitor 108C can be useful in providing AC coupling or power supply decoupling between IC package 106 and PCB 114.

[0044] Grid array capacitor 108D (top view), consistent with view 108B, FIG. 1, depicts secondary conductor 122, inner dielectric 120 and inner conductor 118. Consistent with view 108A, FIG. 1, grid array capacitor 108E includes inner conductor 118, inner dielectric 120 and secondary conductor 122. Grid array capacitor 108C also includes outer dielectric 224 and outer conductor 226. According to embodiments, outer dielectric 224 is located in a coaxial orientation to and at least partially surrounding the secondary conductor 122. Outer conductor 226 is in a coaxial orientation to and at least partially surrounding the outer dielectric 224. Outer conductor 226 is configured to be electrically connected to the IC package 106 and to the PCB 114, FIG. 1.

[0045] It can be understood that the inner conductor 118, secondary conductor 122 and outer conductor 226 can each be used for power, ground, or signals, as needed. In embodiments, capacitive coupling between the inner conductor 118, secondary conductor 122 and outer conductor 226 of grid array capacitor 108C can be useful in providing AC coupling or power supply decoupling between IC package 106 and PCB 114.

[0046] A grid array capacitor 108 configured as a three-terminal capacitor structure can have certain advantageous electrical properties, namely decreased ESL and improved insertion loss relative to a two-terminal capacitor structure. It is understood that ESL in, for example, a decoupling capacitor effectively reduces the capacitance available to act as a filter of power supply noise/transients. The electrical properties and benefits of such three-terminal capacitor structures are further discussed in reference to FIG. 3.

[0047] In the practice of the present disclosure, outer dielectric 224 and outer conductor 226 can be formed together, and subsequently positioned so as to surround inner conductor 118, inner dielectric 120 and secondary conductor 122. For example, outer conductor 226 can be formed as a hollow cylindrical conductive tube, and the inner surface subsequently coated with outer dielectric 224 with a process such as spraying, or dipping. Alternatively, a sheet of conductive material, e.g., copper, can be coated on one

surface with outer dielectric 224, and subsequently rolled or stamped to form a cylindrical shape. Following the fabrication of the outer dielectric 224/outer conductor 226 assembly, this assembly can be positioned so as to surround the secondary conductor 122. The outer dielectric 224 can include, for example, polyimide and/or barium titanate. Outer conductor 226 can include materials such as copper, tin, nickel, silver and gold. Grid array capacitor 108F (top view), consistent with view 108E, depicts inner conductor 118, inner dielectric 120, secondary conductor 122, outer dielectric 224 and outer conductor 226.

[0048] FIG. 3 includes schematic views 302 and 304 of grid array capacitors and a graph 350 depicting insertion loss characteristics of various grid array capacitors, according to embodiments consistent with the figures. Two-terminal circuit 302 includes capacitor C1 and parasitic inductors L1 and L2, series connected between terminal T1 and GND. Three-terminal circuit 304 includes capacitor C2 and parasitic inductors L3, L4 and L5, interconnected between terminals T2, T3 and GND.

[0049] In general, two-terminal capacitor structures have an ESL greater than that of comparable three-terminal capacitors, which can make a two-terminal capacitor less effective in decoupling and AC coupling applications. Three-terminal capacitor structures, e.g., views 108E, 108F, FIG. 2, can therefore have lower ESL and higher electrical performance than comparable two-terminal capacitor structures, e.g., 108A, 108B, FIG. 1.

[0050] Capacitor insertion loss characteristics graph 350 depicts, insertion loss (dB) 352, versus frequency (MHz) 362 plotted against the x-axis for four types of capacitors. Plots include a two-terminal capacitor 354, three-terminal capacitors 356 and 358, and an ideal capacitor 360. It can be noted that across the frequency range 362, when compared to ideal capacitor 360, two-terminal capacitor 354 has the smallest frequency range where insertion loss is lower than the ideal capacitor 360, whereas three-terminal capacitors 356 and 358 have significantly enhanced frequency ranges where insertion loss is lower than the ideal capacitor 360. These enhanced frequency ranges can be viewed as indicating enhanced electrical performance of three-terminal capacitors over two-terminal capacitors in decoupling and AC coupling applications, as described herein.

[0051] FIG. 4 includes a flow diagram 400 and a corresponding sequential set of six side and top process diagram views 434-444 depicting a method for manufacturing a grid array capacitor 108 that is located between an IC package 106 and a PCB 114, according to embodiments consistent with the figures. These process diagram views illustrate an

example process; other views and operations can be possible. An electronic system formed by these process operations can be consistent with 100, FIG. 1, and can have grid array capacitors 108 that provide enhanced capacitance characteristics and increased interconnection reliability. Each grid array capacitor 108 is configured to electrically and mechanically interconnect an IC package 106 to a PCB 114, according to embodiments. Example ICs can include processors, GPUs, memory devices, ASICs, and the like. Example PCBs can include daughter cards motherboards, and standalone PCBs.

[0052] The execution of method 400 can result in an electronic system, e.g., electronic system 100, FIG. 1, having enhanced capacitance characteristics and increased interconnection reliability. An electronic system fabricated according to embodiments can also have improved compensation for non-planarity of PCBs and/or IC packages and grid array capacitor 108 size inconsistencies. Embodiments of the present disclosure are generally consistent with existing ICs, electronic packages, PCBs, as well as existing design methodologies and electronic system fabrication technologies and methods.

[0053] The progression depicted in views 434-444 begins with a secondary conductor 122, and ends with a completed electronic assembly of view 444. Process operations can be completed using processes and materials presently used for electronic system fabrication, such as drilling, alignment, placement, insertion, and solder processes, and solder paste 430.

[0054] For ease of illustration, only 2 grid array capacitors 108 are shown in FIG. 4, however, in the practice of the present disclosure, many grid array capacitors 108 can be used, in an array arrangement, to provide mechanical and electrical interconnections between an IC package 106 and a PCB 114. It can be understood that the operations depicted in FIG. 4 can be performed in conjunction with one or more fixtures used to hold various elements, e.g., secondary conductor 122 and inner dielectric 120 in place during an assembly operation. Such a fixture could include openings or holes arranged to hold such elements in a stationary position during an assembly process.

[0055] For ease of discussion a single label, e.g., view 434, can be used for both a top view and a side view in FIG. 4, in order to identify various entities and elements depicted in the Figures and discussed in the Specification. It can be understood that within the following discussion, elements referred to may be included in one or both of the associated side and top view(s).

[0056] For ease of illustration, secondary conductors 122 are included within the views 434-444 as generic representations of helical structures/springs. It can be

understood that these representations depicted herein in FIG. 4 can represent secondary conductors 122 of any size or proportion useful for particular applications. In some embodiments not depicted, secondary conductors 122 can also represent conductive columnar sleeves or conductive cylinders.

[0057] The results of one or more process operations can be depicted in each view. For example, a view can depict the results a positioning operation and a solder reflow operation which can include alignment and positioning of grid array capacitors 108 adjacent to an IC package 106 and a PCB 114, and subsequently reflowing of solder to attach grid array capacitors 108 to the IC package 106 and to the PCB 114. Processing operations associated with views 434-444 can include, but are not limited to: insertion of an inner dielectric 120 within an opening of a secondary conductor 122, forming an opening in the inner dielectric 120, inserting an inner conductor 118 within the opening, applying solder paste to ends of the grid array capacitor 108, positioning/aligning an IC package 106 and a PCB 114 with the grid array capacitors 108 and a solder reflow operation used to form an assembly of the IC package 106, PCB 114 and grid array capacitors 108.

[0058] Completed structures can be generally shown in views 434-444 as having rectangular cross-sectional profiles, with surfaces orthogonal to each other. This depiction, however, is not limiting; structures can be of any suitable shape, size and profile, in accordance with specific design criteria, lithographic and manufacturing process limitations and tolerances for a given application. For example, corners shown as having right angles can be rounded, surfaces can have a non-orthogonal relative orientation, and relative dimensional ratios can vary from those depicted in the figures.

[0059] Unless explicitly directed towards another figure or view, it can be understood that textual references to figure elements contained within a discussion of an operation of method 400 generally refer to a corresponding view immediately to the right of the discussed operation box of flow diagram 400.

[0060] View 434 depicts a secondary conductor 122 as a conductive helical structure or spring, having an opening 432A. In some embodiments, secondary conductor 122 can be a hollow conductive cylindrical structure such as a metal tube or “sleeve.” According to embodiments, secondary conductor 122 can be fabricated from electrically conductive materials such as copper, tin, nickel, silver or gold. In some embodiments, secondary conductor 122 can be tinned with various solder types in order to facilitate a solder reflow operation. Secondary conductor 122 includes an axially-oriented opening 432A.

[0061] Method 400 moves from start 402 to operation 406. Operation 406 generally refers to inserting an inner dielectric 120 into the axially-oriented opening 432A of a secondary conductor 122. According to embodiments, automated electronic equipment can be used to align and insert an inner dielectric 120 or “*plug*” into the axially-oriented opening 432A of a secondary conductor 122. Such a plug can include high Dk materials such as polyimide and/or barium titanate. Once the inner dielectric is inserted into an axially-oriented opening, the method 400 moves to operation 408.

[0062] Operation 408 generally refers to forming, in the inner dielectric 120, an opening 432B that is suitable to receive an inner conductor 118. According to embodiments, opening 432B is approximately the size, within manufacturing tolerances, of an inner conductor 118, view 440, to be inserted into opening 432B. Opening 432B can be formed using classical mechanical drilling, laser drilling, or other suitable manufacturing methods or processes. Once the opening is formed in the inner dielectric, the method 400 moves to operation 410.

[0063] Operation 410 generally refers to inserting the inner conductor 118 into the opening 432B in the inner dielectric 120. According to embodiments, an inner conductor 118 is approximately the size of opening 432B, within manufacturing tolerances. In embodiments, automated electronic equipment can be used to align and insert inner conductor 118 into the axially-oriented opening 432B of a secondary conductor 122. In some embodiments, the inner conductor 118 is a wire that can include materials such as copper, tin, nickel, niobium and titanium. Once the inner conductor is inserted into the opening in the inner dielectric, the method 400 moves to operation 412.

[0064] Operation 412 generally refers to applying solder paste 430 to opposing ends 116A, 116B of the secondary conductor 122 and to opposing ends 116A and 116B of the inner conductor 118. Solder masks, pastes, and solder spreading equipment consistent with equipment used to apply solder paste to BGA pads of PCBs can be used for this operation. Alternately, solder paste can be applied to IC package 106 and PCB 114, view 444. Once the solder paste 430 is applied to ends of the secondary conductor and the inner conductor, the method 400 moves to operation 414.

[0065] Operation 414 generally refers to electrically and mechanically interconnecting the grid array capacitor 108 to IC package 106 and to PCB 114 by reflowing the solder paste 430. Operation 414 includes positioning and aligning IC package 106, grid array capacitor 108 and PCB 114 in a suitable orientation that includes the ends 116A, 116B (FIG. 1), of grid array capacitors 108, solder paste 430, and

interconnect pads 110 of IC package 106 and PCB 114 being in physical contact. Once this contact is established, a thermal profile is applied by a device such as a specialized reflow oven, using a specified temperature profile, consistent with reflow operations used to attach solder balls to PCBs. The solder paste 430 is brought to at least a melting point and then cooled, joining grid array capacitors 108, solder paste 430, IC package 106 and PCB 114 into an assembly. Once the grid array capacitor is electrically and mechanically interconnected to IC package 106 and to PCB 114, the method 400 may end at block 416.

[0066] In the practice of the present disclosure, additional optional operations can be performed in order to add an outer dielectric 224 and an outer conductor 226, consistent with views 108E and 108F, FIG. 2, to the completed assembly, as described above.

[0067] For example, outer dielectric 224 and outer conductor 226 can be formed together, and subsequently positioned so as to surround inner conductor 118, inner dielectric 120 and secondary conductor 122. Following this example, outer conductor 226 can be formed as a hollow cylindrical conductive tube, and the inner surface subsequently coated with outer dielectric 224 with a process such as spraying, or dipping. Alternatively, a sheet of conductive material, e.g., copper, can be coated on one surface with outer dielectric 224, and subsequently rolled or stamped to form a cylindrical shape. Following the fabrication of the outer dielectric 224/outer conductor 226 assembly, this assembly can be positioned so as to surround the secondary conductor 122.

[0068] The descriptions of the various embodiments of the present disclosure have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiments. The terminology used herein was chosen to explain the principles of the embodiments, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

CLAIMS

1. A grid array capacitor located between an integrated circuit (IC) package and a printed circuit board (PCB), the grid array capacitor configured to be physically and electrically coupled to the IC package and to the PCB, the grid array capacitor comprising:
 - an inner conductor configured to be electrically connected to the IC package and to the PCB;
 - an inner dielectric in a coaxial orientation to and at least partially surrounding the inner conductor; and
 - a secondary conductor in a coaxial orientation to and at least partially surrounding the inner dielectric, the secondary conductor configured to be electrically connected to the IC package and to the PCB.
2. The grid array capacitor of claim 1 further comprising:
 - an outer dielectric in a coaxial orientation to and at least partially surrounding the secondary conductor; and
 - an outer conductor in a coaxial orientation to and at least partially surrounding the outer dielectric, the outer conductor configured to be electrically connected to the IC package and to the PCB.
3. The grid array capacitor of claim 1, wherein the inner conductor is a wire.
4. The grid array capacitor of claim 1, wherein the inner conductor is a helical coil
5. The grid array capacitor of claim 1, wherein the secondary conductor includes a first section adjacent to a first end and a second section adjacent to a second end, wherein the first section and the second section are electrically insulated from each other.
6. The grid array capacitor of claim 1, wherein the secondary conductor includes materials selected from the group consisting of: copper, tin, nickel, niobium and titanium.

7. The grid array capacitor of claim 1, wherein a capacitance of the grid array capacitor is in a range between 1 nF and 8 nF.
8. The grid array capacitor of claim 1, wherein the secondary conductor is a helical coil.
9. The grid array capacitor of claim 1, wherein the secondary conductor is a hollow cylindrical sleeve.
10. An electronic system comprising:
 - a printed circuit board (PCB);
 - an integrated circuit (IC) package;
 - a grid array capacitor located between the IC package and the PCB, the grid array capacitor physically and electrically coupled to the IC package and to the PCB, the grid array capacitor comprising:
 - an inner conductor physically and electrically connected to the IC package and to the PCB;
 - an inner dielectric in a coaxial orientation to and at least partially surrounding the inner conductor; and
 - a secondary conductor in a coaxial orientation to and at least partially surrounding the inner dielectric, the secondary conductor physically and electrically connected to the IC package and to the PCB.
11. The electronic system of claim 10, wherein the secondary conductor is a helical coil.
12. The electronic system of claim 10, wherein the secondary conductor is a hollow cylindrical sleeve.
13. The electronic system of claim 10, wherein the inner dielectric is selected from the group consisting of: polyimide and barium titanate.

14. The electronic system of claim 10, wherein the outer dielectric is selected from the group consisting of: polyimide and barium titanate.
15. A method of manufacturing a grid array capacitor located between an integrated circuit (IC) package and a printed circuit board (PCB) of an electronic system, the method comprising:
- inserting an inner dielectric into an axially-oriented opening of a secondary conductor;
 - forming, in the inner dielectric, an opening suitable to receive an inner conductor;
 - inserting the inner conductor into the opening in the inner dielectric;
 - applying solder paste to opposing ends of the secondary conductor and to opposing ends of the inner conductor;
 - electrically and mechanically interconnecting the grid array capacitor to an IC package and to a PCB by reflowing the solder paste applied to the opposing ends of the secondary conductor and to the inner conductor.
16. The method of claim 15 further comprising:
- forming an outer dielectric that at least partially surrounds the secondary conductor; and
 - forming an outer conductor that at least partially surrounds the outer dielectric.
17. The method of claim 15, wherein the inner conductor includes materials selected from the group consisting of: copper, tin, nickel, niobium and titanium.
18. The method of claim 15, wherein the secondary conductor includes solder at a first end and at a second end.
19. The method of claim 15, wherein the inner dielectric has a relative permittivity (Dk) value between 100 and 5,000.
20. The method of claim 15, wherein the outer dielectric has a relative permittivity (Dk) value between 100 and 5,000.