ABSTRACT

PROCESSING ARCHITECTURES WITH TYPED INSTRUCTION SETS

An architecture fear microprocessors and the like in which instructions include a type identifier, which selects one of several inteipretation registers. The mterpretation registers hold Moπnatiøn for interpreting the opcode of each instruction, so that a stream of compressed instructions (with type identifiers) can be translated into a stream of expanded instructions. Preferably the type identifiers also distinguish sequencer instructions from processing-element instructions, and can even distinguish among different types of sequencer instructions (as well as among different types of processing-element instructions).

FIG. 1

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