

PATENT SPECIFICATION

(11)

1 569 385

1 569 385

- (21) Application No 30714/77 (22) Filed 21 July 1977
(31) Convention Application No. 719550
(32) Filed 1 Sept. 1976 in
(33) United States of America (US)
(44) Complete Specification published 11 June 1980
(51) INT CL³ H03K 13/02
(52) Index at acceptance

H3H 13D 14A 14B 14D 6A 6D 7B 7F 7G 8B 8D BC

- (72) Inventors JAMES EVERETT COOPER, Jr. and
ROBERT CHARLES HUNTINGTON



(54) DIGITAL TO ANALOG CONVERTER

(71) We, MOTOROLA, INC., a corporation organised and existing under the laws of the State of Delaware, United States of America, of 1303 E. Algonquin Road, Schaumburg, Illinois 60196, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to digital to analog (D/A) converters and more particularly to ladderless D/A converters suitable to be fabricated in monolithic form on a single chip utilizing CMOS technology.

The electronic field is replete with applications for D/A converter systems. For example, D/A converters may be used as peripheral units interfacing between microprocessors (MPU's), computers and other systems requiring real time analog voltage inputs. D/A converters are also required in applications where any type of digital number (BCD, binary, etc.) must be converted to a corresponding analog output.

Most contemporary D/A converter systems available today are of the discrete type and comprises resistive ladder termination networks and operational amplifiers. These components result in a D/A converter of relatively large size and high cost. The resistive ladder network typically is fabricated in a matrix using diffused resistors or thin film resistors. Because the accuracy of these converters is directly proportional to the precision of the relative values of the resistors, much care is required in the fabrication thereof. Typically, however, the resistors must be trimmed in value, for instance, by laser trimming or other methods to meet the tolerance established for the system. The process is expensive and undesirous. Moreover, the ladder network makes it virtually impossible to fabricate such converters on a single monolithic chip.

Therefore, a need exists for a D/A converter system which requires no such precision components as a resistive ladder termination network. Such a system could be fabricated on a single chip and requires no trimming. Hence, size and cost could be reduced while maintaining system accuracy.

Another critical problem of the prior art is related to the inherent inaccuracies of operational amplifiers. The offset voltages associated with the operational amplifier produce errors in these systems which must be compensated therefor. Typically, the prior art includes precision adjusting components to provide zeroing of the system and to eliminate the variations caused by the offsets of the amplifiers. These components further increase not only the size but the cost of the prior art systems. Moreover, these converters require constant adjustment to maintain system accuracy. Thus, it is desirous to eliminate the need for such precision components by providing a D/A converter having self zeroing and offset compensation. Where such self-correction is accomplished for each conversion cycle, sensitivity to temperature changes is minimized. Such a system would reduce cost, inaccuracies, eliminate any need for operator attention, and lend itself to being fabricated on a single chip to further reduce the size thereof, all of which are very desirous goals. Moreover, such a D/A converter could be fabricated using CMOS technology which would also reduce power drain to reduce power requirements.

In an attempt to overcome the deficiencies of the prior art discrete converters, one contemporary converter system eliminates the need for the ladder network, and is capable of being fabricated using MOS technology. However, this system suffers from several deficiencies. Most significantly, this system does not compensate for the offset voltages of the included operational amplifiers. These errors arise between the input digital signal

50

55

60

65

70

75

80

85

90

95

and the generation of the output analog signal. In an attempt to overcome these errors, several successive conversion cycles are required by the system which, therefore, time limits the system. Additionally, both positive and negative reference voltages are required to provide conversion of binary numbers of both polarities. To insure accuracy, the system requires that these voltages be equal in absolute magnitude. This requires complex and precision power supplies which increase the cost of the system. Moreover, this system, to provide outputs of both polarities, requires the use of an internal up-down counter which further increases the system complexity and hence cost. Therefore, a need exists for a single chip, CMOS D/A converter which requires only a single reference voltage and which can provide analog outputs of both polarities therefrom, and which is self-correcting for each conversion cycle.

Furthermore, the above prior art converter is capable of only receiving digital input numbers in binary form and is limited to a six-bit input. Thus, there is a requirement for an improved converter which is adaptable to receive any type of binary coded number, i.e., BCD, binary or any other desired code. In conjunction therewith, the input of such a converter should not be limited to the number of input bits—except for practical realities.

According to one aspect of the invention there is provided apparatus for converting both positive and negative digital signals to analog signals, comprising logic input circuitry adapted to receive and store an applied digital input signal during a first portion of the conversion cycle including a circuit for generating monotonically increasing and progressive digital signals and for comparing said generated signals to said stored input signal during a second portion of the conversion cycle to provide a control pulse upon coincidence therebetween; and analog output circuitry adapted to receive a single polarity reference voltage V_R for integrating the same during the time that said circuit is generating said digital signals until coincidence of said digital signals with said stored digital signals to produce an analog signal which is representative of the stored digital signal, integration of said reference signal being terminated in response to said control pulse being provided, said analog output circuitry including circuitry for sampling said analog signal during a third portion of each conversion cycle and holding the value of the same and for providing self compensation to operational offset errors during said first and said second portion of each conversion cycle.

According to another aspect of the

present invention there is provided a digital to analog converter for producing a representative analog output signal in response to receiving either positive or negative digital input signal, characterized by; a control circuit for generating sequence control signals in response to the initiation of a conversion cycle; a latch storage circuit adapted to receive digital signals for storage therein in response to an inhibiting signal applied thereto from said control circuit during a first portion of the conversion cycle; a coincidence circuit selectively enabled by said control circuit for generating increasing and progressive digital signals and for comparing said signals to said digital signal stored in said latch circuit to provide a coincidence output pulse therefrom when coincidence is obtained between said stored digital signal and said generated digital signal during a second portion of said conversion cycle; and analog output circuitry responsive to said control circuit and being adapted to receive a single polarity reference voltage V_R for integrating said reference voltage during the time interval said generated progressive digital signals are being compared to said stored digital signal and coincidence therebetween to produce an analog output signal which is representative of said stored digital signal and including a dual channel sampling circuit for sampling and holding the value of said analog signal during a third portion of said conversion cycle, said analog output circuit providing compensation for analog error signals generated during each conversion cycle.

In accordance with an embodiment of the present invention, there is provided a D/A converter for converting a digital input signal to an analog output signal. The D/A converter of the invention includes input circuitry adapted to receive the digital input number for storing the same and for generating internal digital numbers which are compared to the stored input number. In response to coincidence being obtained therebetween, the input circuit produces a control signal. The D/A converter further includes analog circuitry adapted to receive a single reference voltage for integrating the same while the digital signals are being internally generated and compared to the stored digital number until, in response to the control signal being produced, integration is terminated. In addition, the output circuit includes dual channel sample/hold circuitry for sampling and holding the final voltage value obtained during integration of the conversion cycle. The analog output circuitry provides self zeroing and offset voltage compensation during each

conversion cycle to eliminate errors which otherwise might occur and to which prior art converter systems suffer therefrom.

5 The invention will now be described by way of example only with particular reference to the accompanying drawings wherein:

10 Figure 1 is a functional block diagram of the D/A converter of the present invention;

Figure 2 is a circuit diagram of the linear subsystem of the D/A converter of Fig. 1;

15 Figure 3 is a truth table indicating switch closures of the buffer-integrator section of the linear subsystem of Figure 2 during each timing cycle of a conversion step.

Figure 4 is a truth table indicating switch closures of a sample/hold section of the linear subsystem of Figure 2;

20 Figure 5 is a circuit diagram of an exemplary logic control circuit for providing switch driving signals to the switches of the sample/hold section of Fig. 2;

25 Figure 6 is a sequence timing diagram illustrating the operation of the sample/hold section of the present invention;

Figure 7 is a voltage diagram useful for explaining the operation of the linear subsystem of Figure 2;

30 Figure 8 is another voltage waveform useful for explaining the operation of the linear subsystem; and

35 Figure 9 illustrates particular configurations of the buffer-integrator and sample/hold sections for each of the operational cycles of the D/A converter of the present invention.

Referring to Figure 1, there is illustrated D/A converter 10 of the present invention which is suitable to be fabricated on a single monolithic integrated chip using CMOS technology. D/A converter 10 comprises storage latch bank 12 which is adapted to receive, at input terminal 14, input digital signals and for storing the same. It is to be understood that the digital signals may be applied in parallel or serially to the individual storage latches comprising latch bank 12. The digital signals may be in the form, for example, of binary coded decimal (BCD), binary numbers or any other desired digital code. The output of latch 12 is coupled to coincidence circuit or comparator 16 which is also coupled to the output of counter 18, for instance a synchronous counter. A clock generator 20 is coupled to counter 16 for causing counting thereof. Counter 18 produces digital signals which are in the same code as the storage input digital signal and monotonically progresses from a "zero" count to a full count (the count corresponding to the largest input number applied at terminal 14). An output from clock 20 is also coupled to sequence control

13
circuit 22 which is adapted to receive a strobe or start signal at the input thereof. Sequence control circuit 22 comprises the logic control circuits for controlling the logic functions of D/A converter 10. As will be explained, in response to applied control signals a control signal is provided at the output of sequence control circuit 22, via lead 30, to selectively render selected analog switches either open or closed through switch driver circuit 23. A sign bit, either a logic "1" or "0" is provided to the input of switch driver circuit 23 to control the particular configurations of buffer-integrator circuit 26 of linear subsystem 24. All of the foregoing circuits except for linear subsystem 24 may be considered as the input of D/A converter 10 with the latter comprising the analog output thereof. Besides buffer-integrator section 26, linear subsystem 24 is illustrated as including sample/hold section 28 comprising dual channels. Buffer-integrator section 26 is adapted to receive a single polarity and constant reference voltage which is provided "off-chip". As will be explained, one advantage of the present invention over the prior art is that the reference voltage, V_R , need not be a precise value. It is merely an external voltage which can be adjusted to any desired value.

Briefly, as will be explained in greater detail later, the conversion cycle from the digital input to an analog output comprises three distinctive cycles. Further, only the single reference voltage is required even though the desired analog output voltage may be of either polarity, i.e., negative or positive. The sign bit, either a logic "0" or "1" sets the logic circuits to control the configuration of buffer-integrator section 26 such that the reference voltage is integrated either positive or negative to provide the derived output polarity. Digital input numbers are continually read into latch circuit 12 and the conversion step begins with cycle 1, when the strobe pulse is provided to sequence control circuit 22. The conversion cycle is then initiated and latch 12 inhibited by an inhibiting pulse, via lead 32, from sequence control circuit 22 such that the digital input number appearing coincidentally to the input of the bank of latches is stored and cannot be altered. Simultaneously, synchronous counter 18 is reset to zero, via a command pulse over lead 34, and is allowed to clock through, for example, a full count during the first cycle. The time interval is a function of the period of the clocking signal provided by clock generator 20. During this time interval, linear subsystem 24 is preset to a quiescent operating condition which, as will be explained, eliminates analog errors during the following integration period (cycle 2).

Upon termination of cycle 1, a full count having been obtained, an output pulse from counter 18 to sequence control circuit 22 is generated which resets and again enables counter 18 to begin cycle 2 of the conversion cycle. Simultaneously to the counter being enabled, buffer-integrator section 26 is placed in a configuration to integrate the externally provided reference voltage V_R . This action continues until the number contained in the counter coincides with the stored number at which time coincident circuit 16 produces a coincidence pulse which causes the integrator to stop integrating and to hold the final voltage acquired until this voltage is transferred into sample/hold circuit 28 to provide the output analog output voltage at output terminal 34. This output voltage is held constant until it is altered by the next conversion cycle.

As previously mentioned V_R need not be a precise value. An operator may adjust the reference voltage to any full scale value (within the range of the system) desired. For instance, D/A converter 10 may be put in a set mode which allows counter 18 to count to full count simultaneously with the integrator integrating the reference voltage. The result is that the analog output voltage so produced represents a full scale voltage. By adjusting V_R in the set mode, the magnitude of full scale voltage is varied. When the system is then returned to the operate mode, the analog output voltage appearing at terminal 34 becomes the full scale voltage value times the ratio of the input digital number to the full scale count.

Turning to Fig. 2, there is illustrated linear subsystem 24 in greater detail. Linear subsystem 24, including buffer-integrator section 26 and sample/hold section 28, consists of a plurality of transmission gates or switches $S_1, S_2, S_3, \dots, S_{32}$. The transmission gates are selectively rendered closed or open by logic control signals from sequence control circuit 22 to place buffer-integrator section 26 and sample/hold section 28 in particular configurations during the three distinct cycles of each conversion step.

The buffer portion of buffer-integrator section 26 consists of operational amplifier 38 and compensating capacitor 40 (C_c). The integrator portion of buffer integrator section 26 consists of operational amplifier 42, integrator capacitor 44 (C_i) and integrator resistor 46 (R_i). Sample/hold section 28 is illustrated as including identical dual channels 48 and 50. These channels include, respectively, operational amplifier 52, holding capacitor C_1 , operational amplifier 54 and holding capacitor C_2 . In both buffer-integrator section 26 and sample/hold section 28 the

offsets of the operational amplifiers are compensated to eliminate errors which would otherwise be produced thereby.

Figures 3 and 4 are truth tables indicating the status of transmission gates or switches $S_1, S_2, \dots, S_{32}$ of linear subsystem 24 for the timing cycles, 1, 2 and 3 of the conversion step. As an example, during cycle 2, switches S_4, S_6, S_8, S_{10} and S_{32} of buffer integrator section 26 are closed. Simultaneously, depending on which of the dual channels is in the hold mode only while the other channel is in a hold plus display mode, selected switches of sample/hold circuit 28 are also closed.

Figure 5 illustrates a sample of a logic driver which may be provided to control the states of the transmission gates of sample/hold section 28. As shown, logic driver 56 includes input terminals 58 and 60. Terminal 58 is adapted to receive an input pulse which may be, for example, derived when the coincidence pulse is initiated from comparator 16 to initiate cycle 3 of the conversion step. Simultaneously, the complement of this pulse is applied at terminal 60. These two signals are shown as $CY3$ and $\overline{CY3}$ respectively. Logic drive 56 comprises two D-type flip-flops 62 and 64. Outputs of flip-flop 62 are selectively coupled to NOR gates 66 and 68 and to flip-flop 64. Logic drive signals are provided from the outputs of the circuit as well as inverters 70 and 72 to drive the transmission gates as shown. Similarly, logic control circuits generate switch driving signals to buffer-integrator section 26.

Figures 6-8 represent timing sequence diagrams and waveforms for the three distinct cycles of the conversion step. Additionally, Figure 9 illustrates the effective configurations of linear subsystem 24 during each of the three cycles as determined by the switch closures listed in the truth tables of Figs. 3 and 4. Observing Figures 9A and 9B, note that different configurations are used for cycle 1 depending upon whether the output analog voltage is to negative or positive as determined by a logic "0" or "1" sign bit, respectively.

Referring to the Figures, a first digital to analog conversion cycle illustrating the operation of sample-hold circuit 28 will be explained and then the same for buffer-integrator section 26. The assumption is made that D/A converter 10 has been in operation such that prior to time T_0 , the system is in a third cycle of the conversion step. Thus, coincidence has been obtained between the stored input number and the output of counter 18 which initiates cycle 3 and terminates integration by buffer-integrator section 26. Concurrently, sequence control circuit 22 produces an

output pulse, CY3 and its complement, CY3, which are applied to respective input terminals 58 and 60 of switch logic control circuit 56 (Figure 5). It is to be understood that the time duration of cycle 3 is maintained substantially constant in the preferred embodiment. This may be accomplished by utilizing an auxiliary counter which is enabled to count to a full count which then causes termination of the CY3 control signal from sequence control circuit 22. In response to the cycle 3 control signals, the transmission gates S11, S12, . . . , S26 of sample/hold section 28 are selectively closed as indicated in the truth table of Figure 4 such that the configuration of channel 48 and 50, for example, are as shown in Figure 9E. In this condition, as indicated in Figure 6, channel 50 is in the sample mode and channel 48 is in a hold mode and is connected to output terminal 34. Integrator amplifier 42 is disconnected from buffer amplifier 38 by the selective closures of the switches of buffer integrator section 26 as illustrated by truth table of Figure 3 and the final value of the previous cycle 2 is held constant at the output of the integrator and is sampled by channel 50 of sample/hold circuit 28.

At time T_0 , cycle 1 is initiated by strobing the input of sequence control circuit 22. The CY3 control signal is then inhibited which causes both channels 48 and 50 to be placed in a hold configuration. However, as illustrated by either Figure 9A or 9B, and Figure 6, channel 48 remains connected to the output of D/A converter 10 while channel 50 is placed in a hold configuration but not connected to the output.

Sample/hold section 28 remains in this particular configuration during cycle 2, times T_0 — T_2 . As an aside, because both channels are disconnected from buffer-integrator section 26, the output from D/A converter 10 remains constant and will not vary during conversion cycles 1 and 2. At time T_2 , another cycle 3 is initiated which causes channel 48 to be placed in a sample mode to sample the final value held by integrator amplifier circuit 42 and is simultaneously disconnected from output terminal 34. However, channel 50 remains in the hold mode but is simultaneously connected to output terminal 34 to produce thereat the analog voltage sample thereby during cycle 3 of the previous cycle which occurred prior to time T_0 (Fig. 9D). At T_3 , another cycle 1 is initiated and both channels 48 and 50 are disconnected from integrator amplifier 42 and put in a hold mode. Channel 50 remains connected to output terminal 34. This state remains until time, T_4 , at which a third cycle is again initiated and the previous conversion states are produced.

In brief summary of the above, it is seen that each channel of sample/hold circuit 28 samples during a predescribed cycle 3, holds during the following cycles 1 and 2 and is connected to the output of the D/A converter during the next three cycles. This sequence of states alternates for the two channels such that one channel is always in an output state while the other samples and holds the integrated analog voltage generated during the conversion process. The insertion of a hold state between the sample and output state allows the system to settle to its final value before providing an output voltage. It should be noted that an obvious alternative configuration for some applications would be to eliminate the hold state between sample and output states. This can be accomplished with a simple change in logic control circuit 56. For example, by eliminating flip-flop 64 and providing direct connections from the Q and $\bar{Q}$ outputs of flip-flop 62 to respective switches 526 and 516, the hold state between sampling and output display would be eliminated.

Turning now to buffer-integrator section 26, the effective configurations thereof are different in each of the three cycles as determined by the selection of particular transmission gates or switches as illustrated in the truth table of Figure 3. Considering first the case of a negative input digital signal (sign bit=0) during cycle 1 (when counter 18 is counting through a full count) both buffer amplifier 38 and integrator amplifier 42 are placed in a voltage follower configuration as illustrated in Figure 9A. The noninverting input of buffer amplifier 38 is connected to the reference voltage V_R . Compensating capacitor C_c is serially coupled between buffer amplifier 38 and integrator amplifier 42. Integrator capacitor C_i is coupled between the inverting and noninverting terminals of integrator amplifier 42 and, as will be explained, is charged to an initial quiescent value during the cycle 1 conversion step. The purpose of buffer amplifier 38 is to provide integrator current and charging current for compensating capacitor C_c .

If the digital input number is positive (sign bit=1), as illustrated in Fig. 9B, the roles of buffer amplifier 38 and integrator amplifier 42 are reversed and V_R is applied to the noninverting terminal of integrator amplifier 42. However, both amplifiers are placed in a voltage follower configuration. Furthermore, as observed, the reference voltage V_R component charges capacitor C_c in a reverse polarity to that of the Fig. 9A configuration which causes integration in a negative sense during cycle 2. Note that cycle 2 and cycle 3 configurations for the

buffer and integrators do not change with polarity.

Referring to Figures 7 and 9A for the case of sign bit=0, during cycle 1, the output voltage V_o from integrator amplifier 42 is equal to the offset voltage of amplifier 42 (E_2). Between T_0 and T_1 , capacitor C_c is charged to a voltage V_{AB} which is a function of the reference voltage V_R and the offset voltages of amplifiers 38 and 42. During cycle 2, buffer-integrator section 26 is configured as illustrated in Figure 9C, and the voltage V_{AB} constitutes the input to buffer amplifier 38 which in turn provides the integrating current to integrator 42. As will be explained, the offset voltage E_2 is compensated therefore, such that V_o becomes equal to zero at time T_1 . Integration proceeds in a positive sense between T_1 — T_2 , portion 78 of waveform 76, until coincidence is obtained and integration is terminated by initiation of cycle 3. Integrator amplifier 42 is then separated from buffer amplifier 38 and placed in a hold configuration such that the final voltage value of V_o is held, waveform portion 30. During cycle 3, between times T_2 and T_3 , the final voltage value obtained during cycle 2 is sampled by the selected one of either channel 48 or 50 of sample/hold circuit 28. At the start of the next conversion cycle, if the input number remains negative the input (non-inverting terminal) of the integrator is returned to ground which causes the voltage V_o to be at the same potential so that the initial quiescent operating condition is the same for the start of each conversion. As illustrated by waveform 82, if the input digital number remains constant through succeeding conversion steps, and if the number is negative, the analog output voltage, V_{out} , remains constant and negative and is representative of the digital number.

The operation of buffer-integrator section 26 is the same as the foregoing discussion when the digital number is positive except that the non-inverting input terminal of integrator amplifier 42 is returned to the reference voltage at the beginning of each cycle 1 which establishes the initial output voltage V_o equal to V_R plus the offset voltage E_2 of amplifier 42 (waveform 84, Fig. 8). At time T_1 , the voltage established across capacitor C_1 during cycle 1 compensates for the offset voltage of amplifier 42 such that with the non-inverting input of the integrator returned to ground, portion 86, V_o becomes equal to zero and integration proceeds negatively, portion 88 of waveform 84. The voltage V_o reaches a final negative value at time T_2 and is held constant as before. Because the output of the sample/hold circuit is the inverse of the input thereto,

V_{out} is positive and corresponds to the input number, waveform 90.

As previously mentioned, in both the buffer-integrator section 26 and sample/hold section 28, the offset voltages of the operational amplifiers are compensated. Referring to the particular configurations of these sections as illustrated in Fig. 9, the foregoing self-compensating provision can be discussed.

It is known that for an op amp in a voltage follower configuration that:

$$E = \left(\frac{A}{A-1} \right) E_{os}$$

where E is the resulting voltage from the non-inverting terminal to the output, E_{os} is the input offset voltage and A the open loop gain. With A very large, which is the normal case for an op amp, the output voltage E becomes equal to the offset voltage.

Now, considering the case of a negative input number (sign bit=0), the configuration of buffer integrator section 26 is as illustrated in Figure 9A. In this configuration it can be shown that the voltage V_{AB} produced across capacitor C_c is:

$$V_{AB} = V_R + E_1 - E_2 \quad (1)$$

Also, in this configuration, capacitor C_1 is charged to an initial voltage equal to E_2 which is the offset voltage of amplifier 42. At the beginning of cycle 2, the buffer-integrator section is configured as illustrated in Fig. 9C and the voltage V_{AB} becomes the input voltage to buffer amplifier 38. It can be shown that if the initial voltage on C_1 were zero, the integrator output voltage V_o would be:

$$V_o = E_2 + \frac{1}{R_1 C_1} \int_0^T V_R dt \quad (2)$$

and

$$V_o = E_2 + \frac{V_R T}{R_1 C_1} \quad (3)$$

However, as capacitor C_1 is initially charged during cycle 1 to the value E_2 and is of opposite polarity to the E_2 term of equation 3, these two terms cancel each other such that the final value of the voltage V_o is proportional to the full scale reference voltage $V_R \times T$, where T is the time interval required for obtaining coincidence. In a similar manner, the offset voltages are cancelled when the input digital number is positive.

Turning to sample/hold circuit 28, as illustrated in Fig. 9D, channel 48 is in a

sample mode and channel 50 in hold mode. In a sample mode, the voltage V across capacitor C_1 equals:

$$V = V_{in} + E_{os} \quad (4)$$

5 where V_{in} is the input voltage from integrator 42 and E_{os} equals the offset voltage of the amplifier. In the hold mode, the output voltage v_{out} (Figure 9A) is

$$V_{out} = E_{os} - V \quad (5)$$

10 or, from equation 4

$$V_{out} = E_{os} - V_{in} - E_{os} = -V_{in} \quad (6)$$

Hence, from equation 6 it is observed that the output voltage from the sample/hold channel is the inverse of the input voltage and the offset voltage is cancelled.

15 In summary, the D/A converter of the present invention converts either positive or negative digital input signals to analog output signals of respective polarities. The conversion process functions in three distinct cycles:

Cycle 1:

- A. Digital input is read in and stored.
- 25 B. C_2 is charged with V_{REF} and the op amp offset compensating voltages.
- C. C_1 is charged to the integrator offset voltage.

Cycle 2:

- 30 A. Voltage stored on C_2 is integrated until contents of the counter, which is counting concurrently with the integration, coincides with the stored input digital number. This stops integration.

35 Cycle 3:

- A. Final voltage on the integrator is held while the sample/hold circuit samples.

40 The converter of the present invention provides several significant advantages over the prior art. Good conversion accuracy is obtained with self zeroing and self compensating for operational amplifiers provided; there is no requirement for manual adjustment or precision components. The converter system is equally adaptable to BCD, binary or any other desired input digital code and uses a single polarity off-chip reference voltage which can be adjusted to scale the analog output voltage range to any desired value. 50 As the converter is suitable to be fabricated using CMOS techniques, the converter requires low power consumption.

WHAT WE CLAIM IS:—

- 55 1. Apparatus for converting both positive

and negative digital signals to analog signals, comprising logic input circuitry adapted to receive and store an applied digital input signal during a first portion of the conversion cycle, including a circuit for generating monotonically increasing and progressive digital signals and for comparing said generated signals to said stored input signal during a second portion of the conversion cycle to provide a control pulse upon coincidence therebetween; and analog output circuitry adapted to receive a single polarity reference voltage V_n for integrating the same during the time that said circuit is generating said digital signals until coincidence of said digital signals with said stored digital signals to produce an analog signal which is representative of the stored digital signal, integration of said reference signal being terminated in response to said control pulse being provided, said analog output circuitry including circuitry for sampling said analog signal during a third portion of each conversion cycle and holding the value of the same and for providing self compensation to operational offset errors during said first and said second portion of each conversion cycle.

2. Apparatus as claimed in Claim 1 wherein said logic input circuitry includes a logic control circuit for generating sequence control signals, said logic control circuit being responsive to a start signal to cause said input digital signal to be stored and said circuit for generating progressive digital signals to produce said generated digital signals, said logic control circuit causing said analog output circuitry to be coupled in a plurality of configurations during distinct time intervals of said conversion cycle, said configurations including a compensating mode for providing self compensation to internally generated error signals, an integrating mode, and sample and hold modes.

3. Apparatus as claimed in claim 2 wherein said logic input circuitry further includes; a storage latch circuit for storing said digital input means; a coincidence circuit coupled to said storage latch circuit and said circuit for generating progressive digital signals for producing said control pulse upon coincidence of said stored digital signal with said generated progressive digital signals; and said circuit for generating progressive digital signals including a counter circuit for generating said digital signals and a clocking circuit for driving said counter circuit.

4. Apparatus as claimed in Claim 3 wherein said analog output circuit includes; buffer-integrator circuitry adapted to receive said reference voltage and being responsive to said logic control circuit for



17

sample mode and channel 50 in hold mode. In a sample mode, the voltage V across capacitor C_1 equals:

$$V = V_{in} + E_{os} \quad (4)$$

where V_{in} is the input voltage from integrator 42 and E_{os} equals the offset voltage of the amplifier. In the hold mode, the output voltage v_{out} (Figure 9A) is

$$V_{out} = E_{os} - V \quad (5)$$

or, from equation 4

$$V_{out} = E_{os} - V_{in} - E_{os} = -V_{in} \quad (6)$$

Hence, from equation 6 it is observed that the output voltage from the sample/hold channel is the inverse of the input voltage and the offset voltage is cancelled.

In summary, the D/A converter of the present invention converts either positive or negative digital input signals to analog output signals of respective polarities. The conversion process functions in three distinct cycles:

Cycle 1:

- A. Digital input is read in and stored.
- B. C_2 is charged with V_{REF} and the op amp offset compensating voltages.
- C. C_1 is charged to the integrator offset voltage.

Cycle 2:

- A. Voltage stored on C_2 is integrated until contents of the counter, which is counting concurrently with the integration, coincides with the stored input digital number. This stops integration.

Cycle 3:

- A. Final voltage on the integrator is held while the sample/hold circuit samples.

The converter of the present invention provides several significant advantages over the prior art. Good conversion accuracy is obtained with self zeroing and self compensating for operational amplifiers provided; there is no requirement for manual adjustment or precision components. The converter system is equally adaptable to BCD, binary or any other desired input digital code and uses a single polarity off-chip reference voltage which can be adjusted to scale the analog output voltage range to any desired value. As the converter is suitable to be fabricated using CMOS techniques, the converter requires low power consumption.

WHAT WE CLAIM IS:—

- 1. Apparatus for converting both positive

and negative digital signals to analog signals, comprising logic input circuitry adapted to receive and store an applied digital input signal during a first portion of the conversion cycle, including a circuit for generating monotonically increasing and progressive digital signals and for comparing said generated signals to said stored input signal during a second portion of the conversion cycle to provide a control pulse upon coincidence therebetween; and analog output circuitry adapted to receive a single polarity reference voltage V_R for integrating the same during the time that said circuit is generating said digital signals until coincidence of said digital signals with said stored digital signals to produce an analog signal which is representative of the stored digital signal, integration of said reference signal being terminated in response to said control pulse being provided, said analog output circuitry including circuitry for sampling said analog signal during a third portion of each conversion cycle and holding the value of the same and for providing self compensation to operational offset errors during said first and said second portion of each conversion cycle.

2. Apparatus as claimed in Claim 1 wherein said logic input circuitry includes a logic control circuit for generating sequence control signals, said logic control circuit being responsive to a start signal to cause said input digital signal to be stored and said circuit for generating progressive digital signals to produce said generated digital signals, said logic control circuit causing said analog output circuitry to be coupled in a plurality of configurations during distinct time intervals of said conversion cycle, said configurations including a compensating mode for providing self compensation to internally generated error signals, an integrating mode, and sample and hold modes.

3. Apparatus as claimed in claim 2 wherein said logic input circuitry further includes; a storage latch circuit for storing said digital input means; a coincidence circuit coupled to said storage latch circuit and said circuit for generating progressive digital signals for producing said control pulse upon coincidence of said stored digital signal with said generated progressive digital signals; and said circuit for generating progressive digital signals including a counter circuit for generating said digital signals and a clocking circuit for driving said counter circuit.

4. Apparatus as claimed in Claim 3 wherein said analog output circuit includes; buffer-integrator circuitry adapted to receive said reference voltage and being responsive to said logic control circuit for

integrating said reference voltage during said integrating mode; and dual channel sample and hold circuitry coupled to said buffer-integrator circuitry and being responsive to said logic control circuitry for sampling and holding the final value of the analog output signal during said sampling and holding modes.

5
10
15
20
25
30
35
40

5. A digital to analog converter for producing a representative analog output signal in response to receiving either positive or negative digital input signal, characterized by; a control circuit for generating sequence control signals in response to the initiation of a conversion cycle; a latch storage circuit adapted to receive digital signals for storage therein in response to an inhibiting signal applied thereto from said control circuit during a first portion of the conversion cycle; a coincidence circuit selectively enabled by said control circuit for generating increasing and progressive digital signals and for comparing said signals to said digital signal stored in said latch circuit to provide a coincidence output pulse therefrom when coincidence is obtained between said stored digital signal and said generated digital signal during a second portion of said conversion cycle; and analog output circuitry responsive to said control circuit and being adapted to receive a single polarity reference voltage V_R for integrating said reference voltage during the time interval said generated progressive digital signals are being compared to said stored digital signal and coincidence therebetween to produce an analog output signal which is representative of said stored digital signal and including a dual channel sampling circuit for sampling and holding the value of said analog signal during a third portion of said conversion cycle, said analog output circuit providing compensation for analog

error signals generated during each conversion cycle. 45

6. A converter as claimed in Claim 5 wherein said analog output circuitry includes a buffer amplifier, an integrator amplifier, a compensating capacitor, a 50
integrator circuit (R, C_1) and a plurality of switches interposed between said buffer amplifier, said integrator amplifier, said compensating capacitor, and said integrator circuit means and being 55
responsive to said control circuit for operating said analog output circuitry in a plurality of analog modes.

7. A converter as claimed in Claim 5 wherein each sample and hold channel of said dual channel sample and hold circuit includes an amplifier, a holding capacitor (C, C_2) and additional switches interposed 60
between said holding capacitor, the input and output terminals of said amplifier and said integrator amplifier for operating said sample and hold circuit in a sample and hold 65
mode and for selectively coupling said sample and hold circuits to said integrator amplifier during successive conversion 70
cycles.

8. A converter as claimed in Claim 5 wherein said coincidence circuit includes counter means selectively enabled and reset by said control circuit and comparator 75
means coupled between said latch storage circuit and said counter means and having an output coupled to said control circuit.

9. A digital-to-analog converter substantially as hereinbefore described with 80
reference to the accompanying drawings.

For the Applicants,
F. J. CLEVELAND & COMPANY,
Chartered Patent Agents,
40-43 Chancery Lane,
London, WC2A 1JQ.

