

## INTEGRATED SUBSTRATES AND RELATED METHODS

### CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This document claims the benefit of the filing date of U.S. Provisional Patent Application 63/378,628, entitled “Module Structure Using an Integrated Substrate” to Kang et al. which was filed on 10/6/2022, the disclosure of which is hereby incorporated entirely herein by reference. This document also claims the benefit of the filing date of U.S. Provisional Patent Application 63/378,391, entitled “Transfer Molded Direct Cooling Module” to Kang et al. which was filed on 10/5/2022, the disclosure of which is hereby incorporated entirely herein by reference.

### BACKGROUND

#### 1. Technical Field

[0002] Aspects of this document relate generally to substrates, such as substrates for semiconductor packages.

#### 2. Background

[0003] Semiconductor packages work to provide mechanical support for semiconductor die and to allow them to be coupled with sockets, motherboards, or other components. Semiconductor packages also have been devised that allow for protection of the semiconductor die from humidity and electrostatic discharge effects.

### SUMMARY

[0004] An integrated substrate may include a conductor layer; a heat sink including a plurality of fins extending therefrom; and a dielectric layer including boron nitride chemically bonded to the conductor layer and to the heat sink with an epoxy.

[0005] Implementations of an integrated substrate may include one, all, or any of the following:

[0006] The thermal resistance of the integrated substrate may be lower than a direct bonded copper substrate including silicon nitride.

[0007] The integrated substrate may include a spacer coupled to the conductor layer.

[0008] The integrated substrate may include a semiconductor die coupled to the conductor layer.

[0009] The integrated substrate may include a mold compound coupled to the conductor layer, the heat sink, and the dielectric layer.

[0010] The integrated substrate may include one or more electrical connectors electrically coupled with the conductor layer.

[0011] The integrated substrate may include a second conductor layer, a second heat sink, and a second dielectric layer including boron nitride coupled with a semiconductor die coupled with the conductor layer.

[0012] The boron nitride of the dielectric layer may be a filler in a sheet of epoxy resin.

[0013] The dielectric layer may be sufficiently flexible to be folded in half.

[0014] Implementations of a method of forming an integrated substrate may include providing a conductor layer and a heat sink including a plurality of fins extending therefrom; and chemically bonding a dielectric layer including boron nitride to the conductor layer and to the heat sink with an epoxy.

[0015] Implementations of a method of forming an integrated substrate may include one, all, or any of the following:

[0016] The method may include patterning the conductor layer to form a plurality of traces therein.

[0017] The method may include a coupling a spacer to the conductor layer.

[0018] The method may include coupling a semiconductor die to the conductor layer.

[0019] The method may include applying a mold compound to the conductor layer, the heat sink, and the dielectric layer and electrically coupling one or more electrical connectors with the conductor layer.

[0020] Implementations of a method of forming an integrated substrate may include providing a conductor layer; machining a pattern corresponding with one or more traces into the conductor layer; and coupling the conductor layer and a heat sink to a dielectric substrate. The method may include, after coupling the conductor layer to the dielectric substrate, etching the conductor layer to form the one or more traces.

[0021] Implementations of a method of forming an integrated substrate may include one, all, or any of the following:

[0022] Coupling the conductor layer and the heat sink further may include active metal brazing.

[0023] The method may include coupling one or more spacers with the conductor layer using active metal brazing. Coupling the conductor layer and the heat sink further may include active metal brazing.

[0024] Coupling the conductor layer and the heat sink to the dielectric substrate further may include where the dielectric substrate includes boron nitride.

[0025] The method may include transfer molding a mold compound over the one or more traces, the dielectric substrate, and the heat sink.

[0026] Machining the pattern further may include removing between 90 percent and 95 percent of a thickness of the conductor layer to form the pattern.

[0027] The foregoing and other aspects, features, and advantages will be apparent to those artisans of ordinary skill in the art from the DESCRIPTION and DRAWINGS, and from the CLAIMS.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0028] Implementations will hereinafter be described in conjunction with the appended drawings, where like designations denote like elements, and:

[0029] FIG. 1 is a series of drawings showing side cross sectional views of an integrated substrate at four points during an implementation of a method of forming an integrated substrate;

[0030] FIG. 2 is a cross sectional view of an implementation of an integrated substrate showing two spacers coupled thereto;

[0031] FIG. 3 is a cross sectional view of an implementation of semiconductor package that includes an integrated substrate and mold compound coupled thereto;

[0032] FIG. 4 is a cross sectional view of another implementation of a semiconductor package that includes two integrated substrates and mold compound coupled thereto;

[0033] FIG. 5 is a cross sectional detail view of an implementation of an etched trace;

[0034] FIG. 6 is a cross sectional view of an implementation of an integrated substrate formed using active metal brazing to a ceramic dielectric layer;

[0035] FIG. 7 is a cross sectional view of another implementation of an integrated substrate that includes a dielectric layer that includes boron nitride;

[0036] FIG. 8 is a cross sectional view of an implementation of an integrated substrate at a first point in an implementation of a method of forming an integrated substrate;

[0037] FIG. 9 is a cross sectional view of the implementation of the integrated substrate of FIG. 8 following milling, etching, and plating processes;

[0038] FIG. 10 is a cross sectional view of an implementation of a semiconductor package that includes an integrated substrate and mold compound coupled thereto; and

[0039] FIG. 11 is a cross sectional view of another implementation of a semiconductor package that includes two integrated substrates and mold compound coupled thereto.

#### DESCRIPTION

[0040] This disclosure, its aspects and implementations, are not limited to the specific components, assembly procedures or method elements disclosed herein. Many additional components, assembly procedures and/or method elements known in the art consistent with the intended integrated substrates and related methods will become apparent for use with particular implementations from this disclosure. Accordingly, for example, although particular implementations are disclosed, such implementations and implementing components may comprise any shape, size, style, type, model, version, measurement, concentration, material, quantity, method element, step, and/or the like as is known in the art for such integrated substrates, and implementing components and methods, consistent with the intended operation and methods.

[0041] Direct bond copper (DBC) substrates are used to electrically couple and mechanically hold semiconductor die in place in a semiconductor package and facilitate the connection of various electrical connectors with semiconductor die. In various package implementations, the DBC substrate also has a heat sink bonded to the copper layer on the

side of the substrate that does not have semiconductor coupled thereto. The bonding methods used to attach the heatsink to the copper layer include soldering or sintering. Because soldering involves adding an additional metal layer between the heat sink and the DBC substrate, it adds significantly to the cost of the package and large voids in the solder layer have been observed to consistently be present in the layer post-soldering, increasing thermal resistance in these areas. Sintering the heat sink to the DBC substrate has been observed to regularly result in cracking of the ceramic dielectric portion of the DBC substrate due to the high temperatures and pressures used in sintering processes, where the ceramic dielectric portion includes aluminum oxide or zirconia toughened oxide. Sintering is also a process that can add significant cost to the package formation process. Furthermore, because of the differences in thickness between the first copper layer in the DBC on the opposite side of the dielectric layer from the second copper layer soldered/sintered to the heatsink, warpage of the DBC substrate has been observed to occur unless the first copper layer is thicker than 0.8 mm. Also, when traces are formed in the first copper layer, the spacing between the traces to avoid warping beyond a manufacturable level has been observed to be 2 mm where 1 mm thick copper is used for the first copper layer. This requirement of 2 mm spaced traces limits the ability to include semiconductor die of larger sizes on form the same size of DBC substrate.

**[0042]** Two integrated substrate implementations and related methods are disclosed in this document that structurally differ from DBC substrates in two different ways. In a first implementation, the heat sink is directly coupled to the dielectric layer and not to a second copper layer as when a DBC substrate is used, while a conductor layer is coupled to the opposing side of the dielectric layer, forming an integrated substrate. In a second implementation, a dielectric layer that includes boron nitride is used instead of a ceramic substrate that includes, by non-limiting example, aluminum oxide, aluminum oxide,

zirconia oxide, or beryllium oxide. In implementations of methods of making both integrated substrates, other methods of bonding/coupling the dielectric layer with the conductor layer and heat sink that do not include soldering or sintering are disclosed.

[0043] Referring to FIG. 1, a series of drawings is illustrated showing side cross sectional views of an integrated substrate at four points during an implementation of a method of forming an integrated substrate is illustrated. As illustrated, conductor layer 2 is illustrated which may, in various implementations have a thickness between about 0.8 mm to about 1.2 mm in various implementations. As illustrated in FIG. 1 (and with reference to FIG. 2), the thickness of the conductor layer 2 (distance A) can be matched to the thickness of the largest planar portion of a heat sink 6 coupled to dielectric layer 8 (also distance A). Because of this, the thickness of the conductor layer 2 could also be greater than about 1.2 mm to match a correspondingly greater thickness of the largest planar portion of the heat sink 6. The conductor layer 2 is then illustrated following machining of channels 4 into the material of the conductor layer. In various implementations, about 90 percent to about 95 percent of the thickness of the conductor layer 2 may be removed during the machining process. In various implementations, the machining may take place using a computer numerical control (CNC) machining process. Because of the integration of the substrate structure, a minimum spacing B between adjacent channels can be about 1 mm (rather than the 2 mm observed for DBC substrates). This closer spacing can allow for larger/more die to be coupled to the integrated substrate for the same sized substrate.

[0044] FIG. 1 shows the machined conductor layer 2 coupled to dielectric layer 8 and heat sink 6 forming an integrated substrate where the heat sink is fully integrated by forming the second metal coupled to the dielectric layer 8. In particular method implementations, the conductor layer 2 and heat sink 6 are coupled using an active metal brazing process. Because active metal brazing does not generally involve the use of solder

or other metallization to form the bond between the material of the machined conductor layer 2 and the heat sink, the costs and the observed voiding of the solder process are avoided. Furthermore, the cost and dielectric layer fracturing issues associated with sintering caused by the high temperature and pressure can also be avoided.

[0045] The flow illustrated in FIG. 1 finishes with integrated substrate 10 following an etching process that removes the remaining about 5% to about 10% of the material in the channels forming one or more traces 12 in the conductor layer 2 and exposing the material of the dielectric layer 8. The etching process used in various implementations may be any of a wide variety of processes, including, by non-limiting example, wet etching, dry etching, chemical etching, laser etching, any combination thereof, or any other removal process capable of selectively removing the material of the conductor layer 2. As illustrated in FIG. 1, the heat sink 6 includes a plurality of fins 14 extending therefrom substantially perpendicular to the largest planar surface of the heat sink 6. However, in various implementations, heat sinks of a wide variety of types may be employed that include, by non-limiting example, folded fins, fins, pins, skived fins, or any other heat sink projection type. In various implementations, the projections of the heat sink 6 may be formed prior to coupling to the dielectric layer 8; in other implementations the projections of the heat sink 6 may be formed after coupling to the dielectric layer 8. A wide variety of methods may be employed to form the projections of the heat sinks disclosed herein including by non-limiting example, casting, machining, skiving, molding, or any other method used to form a thermally conductive material.

[0046] Referring to FIG. 2, an implementation of an integrated substrate 16 formed using the method of FIG. 1 is illustrated following coupling of two spacers 18 to the surface of the conductor layer 20. In various method implementations, the spacers 18 can be coupled to the conductor layer 20 using active metal brazing either at the same time the

conductor layer 20 is coupled to the dielectric layer 22 or in a separate active metal brazing step. The use of spacers may be used where the semiconductor package is intended to include double sided cooling via the use of two heat sinks. The spacers may be formed of various materials, including, by non-limiting example, copper, aluminum, copper alloys, aluminum alloys, metals, ceramics, or any other mechanically stiff material capable of electrically/thermally coupling with a semiconductor die and supporting it.

[0047] FIG. 3 illustrates a cross sectional view of an implementation of a semiconductor package 24 following additional packaging steps, including die mounting/bonding of semiconductor die 26 using die bonding material 28 to spacers 30. In various method implementations, the placement of clips and/or wirebonding (not shown in FIG. 3) may also be employed to form additional connections to the semiconductor die 26, the integrated substrate 32, and/or to electrical connectors 34 that are illustrated as extending out from mold compound 36 that covers/contacts the integrated substrate components (conductor layer 38, dielectric layer 40, and heat sink 42). In the various method implementations, a molding process and post-mold-cure (PMC) process are used to apply the mold compound. In various implementations, transfer molding may be used to apply the mold compound. In various package formation methods additional operations may be employed, including laser marking, electroplating of the leads (with tin and with nickel in a particular implementation), and testing of the electrical function of the package.

[0048] Any of a wide variety of semiconductor die may be used in combination with the various integrated substrates disclosed herein, including, by non-limiting example, a silicon die, a silicon-on-insulator die, a silicon carbide die, a gallium arsenide die, a power semiconductor die, a metal oxide field effect transistor (MOSFET) die, an insulated gate bipolar transistor (IGBT), a diode, a rectifier, a thyristor, or any other semiconductor device type formed on any other semiconductor material type. A wide variety of

combinations of semiconductor die and semiconductor packages may be constructed with the integrated substrate implementations disclosed herein using the principles disclosed.

[0049] Referring to FIG. 4, an implementation of a semiconductor package 44 that includes a first integrated substrate 46 and a second integrated substrate 48 is illustrated. The structure of the first integrated substrate 46 and the second integrated substrate 48 are similar to those previously discussed in this document. The first and second integrated substrates 46, 48 are joined through the illustrated arrangement of first spacer 50 and die bonding layers 52, 54 which bond semiconductor die 56 between the substrates. Similarly, second spacer 58, die bonding layers 60, 62 coupled semiconductor die 64 to the first and second integrated substrates 46, 48. Similar to the semiconductor package implementation in FIG. 3, mold compound 66 has been applied over the various components of the first integrated substrate 46 and second integrated substrate 48. As with the implementation illustrated in FIG. 3, additional clips/wirebonds or other structures (not shown in FIG. 4) may be used to electrically connect connectors 68 to the semiconductor die 56, 64; the first integrated substrate 46; and/or the second integrated substrate 48.

[0050] Referring to FIG. 5, a detail cross sectional view of an implementation of a space between traces/etched traces 68, 70 is illustrated. As illustrated, the space includes a head measure 72 and a bottom measure 74. The curved edges of the traces 68, 70 indicates that the space illustrated in FIG. 6 is currently under etched as the head measure 72 is wider/larger than the bottom measure 74. Table 1 shows a non-limiting example of minimum head measures and minimum bottom measures after the machining process and after the subsequent etching processes are completed. Note that the general trend is that the bottom measure is larger/wider than the head measure, indicating an over etch condition exists at the end of the etching process. All of the values in the table are in millimeters and the header row of the table is the thickness of the conductor layer in millimeters.

|                       | 0.5 Cu |        | 0.8 Cu |        | 1.0 Cu  |         | 1.2 Cu  |         |
|-----------------------|--------|--------|--------|--------|---------|---------|---------|---------|
|                       | Head   | Bottom | Head   | Bottom | Head    | Bottom  | Head    | Bottom  |
| <b>Post-Machining</b> | 0.6    | 0.6    | 1.0    | 1.0    | 1.0     | 1.0     | 1.0     | 1.0     |
| <b>Post-Etching</b>   | 1.0    | 1.5    | 1.2    | 2.0    | No data | No data | No data | No data |

**Table 1**

[0051] While Table 1 illustrates a set of post-machining and post-etching head measure and bottom measure values for an integrated substrate implementation that includes copper, other values may exist for other copper-containing implementations and for other conductor types, such as, by non-limiting example, copper alloys, aluminum, aluminum alloys, or any other electrical conductor type. A wide variety of machining and etching head and bottom measures may be constructed using the principles disclosed herein.

[0052] Referring to FIG. 6, an implementation of an integrated substrate 76 formed using the method implementations previous discussed that involve active metal brazing is illustrated. The integrated substrate 76 includes dielectric layer 78, conductor layer 80, and heat sink 82 and FIG. 6 illustrates brazed regions 84, 86 in the material of each of the layers. The brazed regions 84, 86 are formed during the active metal brazing process and are the portions of the various layers that serve to bond the layers together. One of the challenges of the brazed regions 84, 86 is that in various implementations, the coefficient of thermal expansion (CTE) and/or the heat transfer coefficient of the material in the brazed regions is different from the CTE and heat transfer coefficients of the dielectric layer 78, conductor layer 80, and/or the heat sink 82. Because of this, the brazed regions 84, 86 may negatively impact either or both of the CTE and heat transfer performance of the integrated substrate itself.

[0053] FIG. 7 illustrates an implementation of a second type of an integrated substrate 88 that employs a dielectric layer 90 that includes boron nitride. As illustrated,

the integrated substrate 88 also includes a conductor layer 92 and heat sink 94. In various substrate implementations, the conductor layer 92 may be patterned using any of the previously discussed methods of machining and etching. However, in other implementations, other patterning methods may be employed to form the pattern, such as, by non-limiting example, photolithographic patterning and etching or lasering. Similar to the integrated substrate implementations previously disclosed, one or more spacers 96 may be coupled to the conductor 92.

[0054] In a particular implementation, the dielectric layer 90 may be a sheet of epoxy resin that include boron nitride particles as filler. The coefficient of thermal expansion of this implementation of dielectric layer may be about 17-19 ppm and thermal conductivity may be about 16.5 W/K which may enable comparable or better thermal resistance performance to the ceramic dielectric layer materials disclosed previously in this document. In various implementations, because the dielectric layer 90 is made of a sheet of epoxy resin, the layer is flexible enough to allow it to be folded in half/folded back onto itself. Such a dielectric layer 90 material is quite different from the rigid ceramic dielectric layer materials previously discussed in this document and thus has significant mechanical flexibility advantages. For example, the use of the boron nitride-containing dielectric layer may enable the use of common mold compounds with CTEs of about 14-17 ppm for the molding process which may lower the overall package cost. Also, the boron nitride-containing dielectric layer may demonstrate higher thermal conductivity and breakdown voltage than a ceramic dielectric material containing aluminum oxide or aluminum nitride in an insulated metal substrate (IMS) design. This result may be observed particularly when the dielectric layer is formed as an integrated substrate where the heat sink is integrated with the dielectric layer as in the implementation in FIG. 7.

[0055] Referring to FIG. 8, an implementation of an integrated substrate 96 is illustrated in an exploded view during an implementation of a method of forming an integrated substrate. As illustrated, a conductor layer 98 (which may be any conductor layer type disclosed herein) is provided along with heat sink 100 (which may be any heat sink type disclosed herein). Dielectric layer 102 is also provided which contains boron nitride (which may be any boron nitride-containing dielectric layer disclosed herein). The dielectric layer 102 then has an epoxy resin applied to each of its largest planar surfaces and the conductor layer 98 and heat sink 100 are placed in contact with the dielectric layer 102 until the epoxy resin has cured/adhered/bonded the layers and heat sink together. Referring to FIG. 9, the integrated substrate 96 is illustrated following patterning via an etching process and electroplating of layers 104 over portions of conductor layer 98. The method implementation illustrated in FIGS. 8-9, an etch patterning process is utilized that may involve photolithographic patterning, stencil patterning, screen printing, or other methods of protecting the material of the conductor layer 98 during etching. However, in other method implementations, the process of machining the conductor layer 98 previously disclosed herein may be first performed prior to the bonding of the dielectric layer 102 to the conductor layer 98. Then the etching process previously disclosed may be employed to form the one or more traces 106 in the material of the conductor layer 98, which may involve protective patterning or may not include protective patterning in various method implementations.

[0056] With the integrated substrate formed, the substrate can now be used in any of the previously disclosed method implementations that involve semiconductor die attach, wire bonding, clip attach, molding, transfer molding, post-mold-cure, laser marking, electroplating, and/or testing operations to form a semiconductor package. FIG. 10 illustrates a semiconductor package 108 that includes an integrated substrate with a

dielectric layer 110 that includes boron nitride that includes semiconductor die 112, 114 and which includes mold compound 116 that contacts the various components of the integrated substrate. This package includes similar die bonding layers and electrical connections to the electrical connectors 118 included in the package that electrically couple the semiconductor die 112, 114 and/or the integrated substrate to the electrical connectors 118. FIG. 11 illustrates a semiconductor package 120 that includes two integrated substrates with boron nitride containing dielectric layers 122, 124. Like the implementation illustrated in FIG. 4, this package includes spacers 126, 128, but these spacers are attached to just one of the integrated substrates while the semiconductor die 130, 132 are attached to the other integrated substrate. This package also contains electrical connectors 134 which are electrically connected to the semiconductor die 130, 132 and/or the integrated substrates through wirebonds/clips, etc. similar to the implementations previously disclosed herein.

[0057] In places where the description above refers to particular implementations of integrated substrates and implementing components, sub-components, methods and sub-methods, it should be readily apparent that a number of modifications may be made without departing from the spirit thereof and that these implementations, implementing components, sub-components, methods and sub-methods may be applied to other integrated substrates.

## CLAIMS

What is claimed is:

1. An integrated substrate (88) comprising:  
a conductor layer (92);  
a heat sink (94) comprising a plurality of fins extending therefrom; and  
a dielectric layer (90) comprising boron nitride chemically bonded to the conductor layer (92) and to the heat sink (94) with an epoxy.
2. The integrated substrate of claim 1, wherein a thermal resistance of the integrated substrate (88) is lower than a direct bonded copper substrate comprising silicon nitride.
3. The integrated substrate of claim 1, further comprising a spacer (126) coupled to the conductor layer (92).
4. The integrated substrate of claim 1, further comprising a semiconductor die (112) coupled to the conductor layer (92).
5. The integrated substrate of claim 1, further comprising a mold compound (116) coupled to the conductor layer (92), the heat sink (94), and the dielectric layer (90).
6. The integrated substrate of claim 1, further comprising one or more electrical connectors (118) electrically coupled with the conductor layer (92).

7. The integrated substrate of claim 1, further comprising a second conductor layer, a second heat sink, and a second dielectric layer (124) comprising boron nitride coupled with a semiconductor die (114) coupled with the conductor layer.
8. The integrated substrate of claim 1, wherein the boron nitride of the dielectric layer (90) is a filler in a sheet of epoxy resin.
9. The integrated substrate of claim 8, wherein the dielectric layer (90) is sufficiently flexible to be folded in half.

10. A method of forming an integrated substrate (88) comprising:  
providing a conductor layer (92) and a heat sink (94) comprising a plurality of fins extending therefrom;  
chemically bonding a dielectric layer (90) comprising boron nitride to the conductor layer (92) and to the heat sink (94) with an epoxy.
11. The method of claim 10, further comprising patterning the conductor layer (92) to form a plurality of traces (106) therein.
12. The method of claim 10, further comprising coupling a spacer (126) to the conductor layer (92).
13. The method of claim 10, further comprising coupling a semiconductor die (112) to the conductor layer (92).
14. The method of claim 10, further comprising applying a mold compound (116) to the conductor layer (92), the heat sink (94), and the dielectric layer (90) and electrically coupling one or more electrical connectors (118) with the conductor layer (92).

15. A method of forming an integrated substrate (16) comprising:
- providing a conductor layer (2);
  - machining a pattern corresponding with one or more traces (12) into the conductor layer (2);
  - coupling the conductor layer (2) and a heat sink (6) to a dielectric substrate (8);
  - after coupling the conductor layer (2) to the dielectric substrate (8), etching the conductor layer (2) to form the one or more traces (12).
16. The method of claim 15, wherein coupling the conductor layer (2) and the heat sink (6) further comprises active metal brazing.
17. The method of claim 15, further comprising coupling one or more spacers (18) with the conductor layer (2) using active metal brazing and wherein coupling the conductor layer (2) and the heat sink (6) further comprises active metal brazing.
18. The method of claim 16, wherein coupling the conductor layer (2) and the heat sink (6) to the dielectric substrate (8) further comprises wherein the dielectric substrate (8) comprises boron nitride.
19. The method of claim 16, further comprising transfer molding a mold compound (36) over the one or more traces (12), the dielectric substrate (8), and the heat sink (6).
20. The method of claim 15, wherein machining the pattern further comprises removing between 90 percent and 95 percent of a thickness of the conductor layer (2) to form the pattern.