WHAT IS CLAIMED IS:

1. A method for forming a semiconductor device, the method comprising:

forming a stacked structure having a plurality of stacked layers;

forming a plurality of stepped trenches having a first depth in the stacked structure by etching the stacked structure, each of the stepped trenches having first and second opposing stepped sidewalls that each have a plurality of steps;

forming an etch stop pattern having a hard mask material over a top surface of the stacked structure, the etch stop pattern including a plurality of openings exposing portions of the plurality of stepped trenches;

forming a first photoresist pattern over the etch stop pattern, the first photoresist pattern filling a first portion of the openings and exposing a second portion of the openings; and

etching the second portion of the openings using the etch stop pattern as an etch mask to extend a bottom of the stepped trenches exposed by the second portion of the openings to a second depth lower than the first depth.

2. The method of claim 1, wherein the semiconductor device includes a cell region and a contact region, and

wherein etching the second portion of the openings forms a first

groove, and a first stepped trench of the plurality of stepped trenches is disposed between the first groove and the cell region of the semiconductor device.

3. The method of claim 2, further comprising:

removing the first photoresist pattern from the first portion of the openings;

forming a second photoresist pattern that covers the first groove; and

etching a third portion of the openings using the etch stop pattern and the second photoresist pattern as etch masks.

4. The method of claim 3, wherein etching the third portion of the openings includes forming a second groove adjacent to the first groove, the second groove having a depth greater than that of the first groove.

5. The method of claim 4, wherein etching the third portion of the openings includes forming a third groove adjacent to the second groove, the third groove having a depth greater than that of the second groove.

6. The method of claim 1, wherein the plurality of openings of the etch stop pattern extends in a first direction, and the plurality of stepped trenches extends in a second direction perpendicular to the first direction.

7. The method of claim 1, wherein the stacked structure comprises a plurality of first layers alternating with a plurality of second layers, the second layers comprising a different material from the first layers, and each of the steps has at least one of the first layers and at least one of the second layers.

8. The method of claim 7, wherein the stacked structure comprises at least 32 first layers and at least 32 second layers.

9. The method of claim 8, wherein etching the second portion of the openings includes etching at least 8 first layers and at least 8 second layers.

10. The method of claim 7, wherein the stacked structure comprises at least 96 first layers and at least 96 second layers.

11. The method of claim 10, wherein etching the second portion of the openings includes etching at least 16 first layers and at least 16 second layers.

12. The method of claim 1, wherein edges of openings in the first photoresist pattern are set back from edges of openings in the etch stop pattern.

13. The method of claim 1, wherein the first stepped sidewalls are asymmetric to the second stepped sidewalls.

14. The method of claim 1, wherein the second stepped sidewalls are dummy structures.

15. The method of claim 1, wherein the semiconductor device includes a cell region and a contact region and steps of the first stepped sidewalls are contact pads for the contact region, the method further comprising:

respectively forming vertical contacts on the contact pads.

16. The method of claim 1, wherein the openings in the etch stop pattern are used to form a plurality of grooves having different depths, the method further comprising filling the plurality of grooves with an insulating material.

17. The method of claim 16, further comprising:

removing a portion of the insulating material using the etch stop pattern as a stop layer.

18. The method of claim 1, wherein the openings are substantially rectangular openings that are used to define sidewalls of a plurality of grooves through a plurality of etching processes.

19. The method of claim 18, wherein the substantially rectangular openings define four sidewalls of each of the plurality of grooves.

20. The method of claim 1, wherein the semiconductor device is a memory device that includes at least 192 layers in the stacked layers.