# METHODS FOR PACKAGING MICROELECTRONIC DEVICES AND MICROELECTRONIC DEVICES FORMED USING SUCH METHODS

## TECHNICAL FIELD

**[0001]** The present invention is related to methods for packaging microelectronic devices and microelectronic devices formed using such methods.

## BACKGROUND

**[0002]** Packaged microelectronic devices are used in cellular phones, pagers, personal digital assistants, computers, and many other electronic products. Conventional packaged microelectronic devices can include a singulated microelectronic die, an interposer substrate or lead frame attached to the die, and a molded casing around the die. The die generally includes an integrated circuit and an active side with a plurality of bond-pads coupled to the integrated circuit. The bond-pads are typically coupled to terminals on the interposer substrate or lead frame, and supply voltage, signals, etc., are transmitted to and from the integrated circuit via the bond-pads. In addition to the terminals, the interposer substrate can also include ball-pads coupled to the terminals by conductive traces supported in a dielectric material. Solder balls can be attached to the ball-pads in one-to-one correspondence to define a "ball-grid array." Packaged microelectronic devices with ball-grid arrays are generally higher grade packages having lower profiles and higher pin counts than conventional packages using lead frames.

**[0003]** One such conventional packaged microelectronic device is a build up package ("BUP") microelectronic device. BUP devices are formed by placing multiple singulated microelectronic dies active side down on a temporary carrier. A fill material is used to cover the dies and the carrier. Once the fill material sets up, the temporary carrier is removed. The active sides of the dies are cleaned and then a redistribution layer is applied to the active sides of the dies. Often solder balls are connected to the

redistribution layer and a dielectric layer is placed over portions of the redistribution layer so that the solder balls extend through the dielectric layer. The fill material between the dies is then cut to separate the dies from one another and form multiple BUP devices. The solder balls and redistribution layer can then be used to connect the BUP device to a printed circuit board. In certain cases, the redistribution layer can extend beyond the edge of the die onto the fill material to increase the area available for the array of solder balls.

**[0004]** BUP microelectronic devices can also be formed by placing multiple singulated dies active side up on a temporary carrier and placing a fill material between the dies. Once the fill material hardens, the temporary carrier is removed and the BUP devices are separated by cutting the fill material between the dies. However, with this process it can be difficult to place a redistribution layer on the active sides because the active sides and the fill material between the dies may not form a sufficiently planar surface for effective and efficient application of a redistribution layer.

**[0005]** The foregoing processes have a large number of steps, and thus fabricating BUP devices can be time consuming and expensive. Additionally, BUP devices may not be well suited for use in stacked die arrangements because BUP devices generally only have contacts on the active side of each device. Accordingly, a significant amount of space on a circuit board must be reserved for BUP devices in products that require several such devices. This can be problematic because the sizes of electronic products that use BUP devices are decreasing in response to consumer demand. Therefore, it would be desirable to produce BUP devices that are well suited for stacked die arrangements.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0006]** Figures 1-8 schematically illustrate stages in a method for packaging microelectronic devices in accordance with certain embodiments of the invention.

**[0007]** Figure 9 is a schematic illustration of stacked microelectronic devices in accordance with selected embodiments of the invention.

**[0008]** Figures 10-11 schematically illustrate the formation of microelectronic devices in accordance with other embodiments of the invention.

**[0009]** Figure 12 is a schematic illustration of stacked microelectronic devices in accordance with still other embodiments of the invention.

## DETAILED DESCRIPTION

### A. Overview/Summary

**[0010]** The following disclosure describes methods for packaging microelectronic devices and microelectronic devices formed using such methods. One aspect of the invention is directed toward a method for packaging microelectronic devices that includes coupling multiple microelectronic dies to a surface of a support member. Individual microelectronic dies can have an active side, a backside, and a through-wafer interconnect extending from the active side toward the backside. The individual dies generally have a plurality of through-wafer interconnects having a first end at the active side and a second end at the backside or at an intermediate level within the die toward the backside. The active side of each microelectronic die can be coupled to the surface of the support member. The method can further include applying an encapsulant to cover at least a portion of the surface of the support member so that a portion of the encapsulant is laterally adjacent to the microelectronic dies. The method can still further include removing material from the backside of the microelectronic dies to expose a portion of the through-wafer interconnects, and applying a redistribution structure to the backside of the microelectronic dies. The redistribution structure can be electrically coupled to the through-wafer interconnects.

**[0011]** Other aspects of the invention are directed toward a method for packaging a microelectronic device that includes coupling an active side of a microelectronic die to a surface of a support member. The microelectronic die can have a backside opposite the active side, a peripheral side extending at least part way between the active side and the backside, and at least one through-wafer interconnect. The method can further include applying an encapsulant to cover at least a portion of the surface of the support member so that a portion of the encapsulant is laterally adjacent to the peripheral side. The method can still further include removing material from a backside of the microelectronic die to

expose a portion of at least one through-wafer interconnect, and applying a redistribution structure to the backside of the microelectronic die. The redistribution structure can be electrically coupled to the at least one through-wafer interconnect.

**[0012]** Still other aspects of the invention are directed toward a method for packaging microelectronic devices that includes attaching multiple microelectronic dies to a surface of a support member. Individual microelectronic dies can have an active side, a backside, and at least one through-wafer interconnect. The active side of each microelectronic die can be attached to the surface of the support member. The method can further include applying an encapsulant to cover the multiple microelectronic dies and at least a portion of the surface of the support member so that a portion of the encapsulant is laterally adjacent to the microelectronic dies. The method can still further include removing material from the backside of the microelectronic dies to expose a portion of the through-wafer interconnects and applying a redistribution structure to the backside of the microelectronic dies. The redistribution structure can be electrically coupled to the through-wafer interconnects. The method can yet further include connecting at least one of solder balls and solder bumps to the at least one redistribution structure and singulating the microelectronic dies.

**[0013]** Yet other aspects of the invention are directed toward a method for packaging a microelectronic device that includes coupling an active side of a microelectronic die to a surface of a support member and applying an encapsulant to cover at least a portion of the microelectronic die and at least a portion of the surface of the support member so that a portion of the encapsulant is laterally adjacent to the microelectronic die. The method can further include removing material from a backside of the microelectronic die to expose a portion of at least one through-wafer interconnect and applying a redistribution structure to the backside of the microelectronic die. The redistribution structure can be electrically coupled to the at least one through-wafer interconnect. The method can still further include connecting at least one of solder balls and solder bumps to the redistribution structure.

**[0014]** Still other aspects of the invention are directed toward a microelectronic device that includes a microelectronic die having an active side, a backside opposite the active side, a peripheral side extending at least part way between the active side and the

backside, and at least one through-wafer interconnect. The through-wafer interconnect can have an active side portion electrically coupled to the active side of the microelectronic die and a backside portion. The device can further include a redistribution structure electrically coupled to the backside portion of the at least one through-wafer interconnect and an encapsulant laterally adjacent to the peripheral side of the microelectronic die.

**[0015]** Yet other aspects of the invention are directed toward microelectronic devices that include a support member having a surface and multiple microelectronic dies. Each microelectronic die can have an active side, a backside, and at least one through-wafer interconnect. The at least one through-wafer interconnect can have a first portion electrically coupled to the active side of the microelectronic die and a second portion. The multiple microelectronic dies can be coupled to the surface of the support member so that the active side of the microelectronic die is adjacent to the surface of the support member. The device can further include at least one redistribution structure. The at least one redistribution structure can be electrically coupled to the second portions of the through-wafer interconnects. The device can further include an encapsulant covering at least a portion of the support member so that a portion of the encapsulant is laterally adjacent to the microelectronic dies.

**[0016]** Still other aspects of the invention are directed toward stacked microelectronic devices that include a first microelectronic device and at least one second microelectronic device stacked with the first microelectronic device. The first microelectronic device can include a microelectronic die having an active side, a backside, at least one peripheral side, and at least one through-wafer interconnect. The through-wafer interconnect can have a first portion electrically coupled to the active side of the microelectronic die and a second portion. The first microelectronic device can further include a redistribution structure electrically coupled to the second portion of the at least one through-wafer interconnect and an encapsulant adjacent to the at least one peripheral side.

**[0017]** Many specific details of certain embodiments of the invention are set forth in the following description and in Figures 1-12 to provide a thorough understanding of these embodiments. A person skilled in the art, however, will understand that the invention may be practiced without several of these details or additional details can be added to the

invention. Well-known structures and functions have not been shown or described in detail to avoid unnecessarily obscuring the description of the embodiments of the invention. Where the context permits, singular or plural terms may also include plural or singular terms, respectively. Moreover, unless the word "or" is expressly limited to mean only a single item exclusive from the other items in reference to a list of two or more items, then the use of "or" in such a list is to be interpreted as including (a) any single item in the list, (b) all of the items in the list, or (c) any combination of the items in the list. Additionally, the term "comprising" is used throughout to mean including at least the recited feature(s) such that any greater number of the same feature and/or additional types of features or components are not precluded.

B. Methods for Packaging Microelectronic Devices and Microelectronic Devices Formed Using Such Methods

**[0018]** Figures 1-8 illustrate various stages in a method for packaging microelectronic devices build up package microelectronic devices and microelectronic devices formed using such a method, in accordance with certain embodiments of the invention. The examples of the method shown in Figures 1-8 are particularly useful for fabricating build up package devices for use in single and/or stacked die arrangements. Figure 1 is a partially schematic cross-sectional illustration of multiple microelectronic dies 110, shown as a first microelectronic die 110a and a second microelectronic die 110b. The first die 110a can include an active side 111a, a backside 113a (e.g., opposite the active side), one or more peripheral sides 118a between the active side 111a and the backside 113a, and integrated circuitry IC (shown schematically). The active side 111a can include one or more die contacts 112a (e.g., bond-pads) electrically coupled to the integrated circuitry IC. The first die 110a can also include one or more through-wafer interconnects 114a that are electrically coupled to the integrated circuitry IC and that extend through at least a portion of the first die 110a. The through-wafer interconnects 114a can include first portions 115a proximate to the active side of the first die 110a and second portions 116a positioned opposite the first portions 115a. The first portions 115a of the through-wafer interconnects 114a of the first die 110a can be electrically coupled to the integrated circuitry IC (e.g., via the die contacts 112a).

**[0019]** Similarly, the second die 110b includes an active side 111b with one or more die contacts 112b, a backside 113b, one or more peripheral sides 118b, integrated circuitry IC (shown schematically), and one or more through-wafer interconnects 114b with first portions 115b and second portions 116b. Although in the illustrated embodiment the dies 110 have the same configuration, in other embodiments the dies 110 may have different features to perform different functions. For example, various dies 110 can include memory devices, processors, or other types of devices that include integrated circuitry (e.g., DRAM, SRAM, Flash, Imagers, PCRAM, MRAM, and CAM).

**[0020]** Figure 2 is a partially schematic cross-sectional illustration of the first and second dies 110a and 110b coupled to a support member 120 that has a first side 121 and a second side 123. In certain embodiments the support member 120 can include various contacts and connectors. For example, in Figure 2 the support member 120 includes first support contacts 122 at the first side 121 and second support contacts 124 at the second side 123 that are electrically coupled to corresponding first support contacts 122. The first and second dies 110a and 110b can be temporarily or permanently coupled (e.g., mechanically and/or electrically) to the support member 120 with their respective active sides 111a and 111b facing the first surface 121 of the support member 120.

**[0021]** For example, in the illustrated embodiment the active sides 111a and 111b of the first and second dies 110a and 110b are mechanically attached to the support member 120. The active sides 111a and 111b of the dies 110a and 110b can be coupled to the support member 120 using various techniques well known to those skilled in the art. For example, the dies 110 can be mechanically or physically coupled or attached to the support member 120 using various types of adhesive films, epoxy, tape, paste, or other suitable material. In certain embodiments were the dies 110 are temporarily attached to the support member 120, a releasable attachment method can be used, such as tapes or adhesives that have suitable thermal release characteristics (e.g., where the bond is released at a certain temperature).

**[0022]** Additionally, the die contacts 112a and 112b of the first and second dies 110a and 110b contact the first support contacts 122 to electrically couple the integrated circuitry IC of the first and second dies 110a and 110b with the support member 120. Because the

first support contacts 122 are electrically coupled to the second support contacts 124 in the illustrated embodiment, the integrated circuitries IC of the first and second dies are also electrically coupled to the second support contacts 124. In selected embodiments, the dies 110 can be electrically coupled to the support 120 via various techniques. For example, in certain embodiments contacts on the dies 110 can be positioned to physically touch contacts on the support 120. In other embodiments, other techniques can be used to electrically couple the dies 110 to the support 120, for example, flip chip and direct die attach methods can also be used. In certain embodiments, the technique used to electrically couple the dies 110 to the support 120 can also mechanically couple the dies 110 to the support 120 (e.g., using various flip chip attach techniques). In other embodiments, the support has no electrical contacts and the dies 100 are only mechanically attached to the support.

**[0023]** Although in the illustrated embodiment the first and second dies 110a and 110b are shown laterally disposed from each other in one direction, it is understood that multiple dies can be positioned relative to the support member in other arrangements. For example, Figure 3 is a partially schematic top plan view of multiple dies 310 coupled to a support member 320 so that the dies are laterally disposed from one another in multiple directions (e.g., two directions) in accordance with certain embodiments of the invention. In Figure 3 the dies 310 are coupled to the support 320 with the active sides of the dies 310 adjacent to a surface 321 of the support 320 and the backsides 313 of the dies 310 opposite the active sides. Additionally, as shown in Figure 3, there is space 335 between and around (e.g., laterally adjacent to) the dies 310. The space 335 is positioned above the surface 321 of the support 320 Accordingly, portions of the space 335 are laterally disposed from the one or more peripheral sides 318 of the dies 310 and from the dies 310 themselves.

**[0024]** Figure 4 is a partially schematic cross-sectional view of the dies 110 and support member 120 shown in Figure 3 after an encapsulant 135 has been applied to cover at least a portion of the first surface 121 of the support member 120. In the illustrated embodiment, the encapsulant has been applied to the extent that it covers the backsides 113a and 113b of the dies 110. In Figure 4, a portion of the encapsulant is

laterally disposed from, and attached to, the peripheral sides 118a and 118b of the dies 110. Accordingly, a portion of the encapsulant has filled at least a portion of the space 135 between the first and second dies 110a and 110b. In other embodiments, the encapsulant 130 is only placed between the dies and does not cover the backsides 113a and 113b of the dies 110. The encapsulant 130 can be applied via various methods including an over mold method, a liquid dispense method, a film-assisted molding process, and a glob-type dispensing process, all of which are well-known to those skilled in the art. The encapsulant 130 can include various types of materials, including a dielectric material or an epoxy.

**[0025]** Figure 5 is a partially schematic cross-sectional view of the dies 110 and support member 120 shown in Figure 4 after removing at least a portion of the backsides of 113a and 113b of the dies 110 and a portion of the encapsulant 130 (e.g., by a planarization or back grinding process). In the illustrated embodiment, sufficient material has been removed from the backsides 113a and 113b to expose the second portions 116a and 116b of the through-wafer interconnects 114a and 114b. Also, in selected embodiments, the backsides 113a in 113b of the dies 110 and the encapsulant 134 can form a generally planar surface after removing the material, as shown in Figure 5.

**[0026]** Figure 6 is a partially schematic cross-sectional view of the dies 110 and support member 120 shown in Figure 5 after a redistribution structure 140 has been applied to the backsides 113a and 113b of the dies 110. In the illustrated embodiment, the redistribution structure 140 has contacts electrically coupled to the second portions 116a and 116b of the through-wafer interconnects 114a and 114b. In Figure 6, portions of the redistribution structure 140 extend over, or are carried by, at least part of the portion of the encapsulant 130 that is laterally adjacent to the dies 110. The redistribution structure 140, however, can be applied so that a portion of the redistribution structure 140 does not extend onto the encapsulant 130.

**[0027]** Figure 7 is a partially schematic cross-sectional view of the dies 110 and support member 120, shown in Figure 6, where connector elements 150 have been coupled to the redistribution structure 140. The connector elements 150 can include various types of connectors including solder balls, solder bumps, and/or reflowable

contacts that can act as a connecting mechanism between multiple components during a reflow process (e.g., when multiple components that are being connected are placed in a reflow oven). The dies can then be separated to form multiple separate microelectronic devices. For example, in the illustrated embodiment the first and second dies 110 can be singulated by cutting along line S-S through the encapsulant 130 and the support member 122 to form two microelectronic devices 105, shown in Figure 8 as a first microelectronic device 105a and a second microelectronic device 105b. In various embodiments, the microelectronic devices 105 can be operably coupled to one or more other electronic devices (e.g., a circuit board) via the second support contacts 124 and/or the connector elements 150.

**[0028]** A feature of some of the embodiments described above is that a build up package microelectronic device can be formed using fewer steps than is required with current processes. Accordingly, build up package microelectronic devices can be formed in less time allowing a higher throughput in the production process than with current methods. An advantage of this feature is that fewer steps in the formation process and/or higher production throughput can result in a cost savings per microelectronic device produced.

C. Additional Embodiments of Microelectronic Devices and Methods for Packaging Microelectronic Devices

**[0029]** In other embodiments, the microelectronic devices 105 discussed above with reference to Figures 1-8 can have other arrangements, including more, fewer, and/or different components. For example, in certain embodiments the microelectronic devices 105 do not include connector elements 150 and/or a redistribution structure 140. In still other embodiments, at least a portion of the support member 120 is removed from at least one of the microelectronic devices 105. For example, in certain embodiments the support member 120, shown in Figure 7, is removed from the dies 110 before the dies are separated. In still other embodiments, the microelectronic devices 105 are singulated before the one or more connector elements 150 are coupled to the microelectronic devices 105. In still other embodiments, the microelectronic devices 105 can be stacked with each other or with other types of microelectronic devices.

**[0030]** For example, Figure 9 is a partially schematic cross-sectional view of the first and second microelectronic devices 105a and 105b, shown in Figure 8, stacked on one another to form a stacked unit 107. In Figure 9, the first microelectronic device 105a has been positioned relative to the second microelectronic device 105b so that the connector elements 150 of the second microelectronic device 105b are in contact with the second support contacts 124 (discussed above with reference to Figure 2) of the first microelectronic device 105a. Accordingly, in the illustrated embodiment the integrated circuits IC of the first microelectronic device 105a are connected to the integrated circuits IC of the second microelectronic device 105b. For example, in the illustrated embodiment, the integrated circuits IC of the second microelectronic device 105b are electrically connected to the connector elements 150 via the die contacts 112b, the through-wafer interconnects 114b, and the redistribution structure 140. The connector elements 150 are electrically connected to the integrated circuits IC of the first microelectronic device 105a via the second support contacts 124, the first support contacts 122, and the die contacts 112a.

**[0031]** In the illustrated embodiment, the connector elements 150 of the first microelectronic device can be used to operably couple the stacked unit 107 to another device (e.g., a circuit board). In still other embodiments, the second contact pads of the second microelectronic device 105b can be used to operably couple the stacked unit 107 to another device. Although only two microelectronic devices 105a and 105b are shown stacked in Figure 9, in other embodiments three or more microelectronic devices can be stacked together. Additionally, in certain embodiments a coating or covering 160 can be applied to at least one surface of at least one microelectronic device to provide protection and/or insulation. For example, the covering 160 shown in Figure 9 can include various types of material, including dielectric materials and/or encapsulants.

**[0032]** A feature of some of the embodiments discussed above with reference to Figures 1-9 is that build up package microelectronic devices can be formed so that they can be stacked with one another and/or with other microelectronic devices. Stacked microelectronic devices can take up less space on a circuit board and/or allow designers to use space more efficiently by distributing microelectronic devices in multiple dimensions

when placing microelectronic devices in electronic products. An advantage of this feature is that electronic products using build up package microelectronic devices can be made smaller in response to consumer demand.

**[0033]** In other embodiments, the microelectronic devices can have still other arrangements. For example, Figure 10 is a partially schematic cross-sectional view of a two microelectronic dies 810, shown as a first microelectronic die 810a and a second microelectronic die 810b, coupled to a temporary support member 820. In Figure 10, individual dies include an active side 811, a backside 813, integrated circuitry IC, one or more die contacts 812, and one or more through-wafer interconnects 814. The dies 810 are attached to the support member 820, but the support member 820 does not include any electrical contacts.

**[0034]** In Figure 10, an encapsulant 830 has been applied to the dies 810 and to portions of the support member 820 so that a portion of the encapsulant 830 is in the spaces between the dies 810. Some of the encapsulant 830 and a portion of the backsides 813 of the dies 810 have been removed to form a generally planar surface and expose portions of the through-wafer interconnects 814. A redistribution structure 840 has been applied to the backsides 813 of the dies 810 and is electrically coupled to the exposed portions of the through-wafer interconnects 814 (e.g., the redistribution structure 840 can be attached to or in contact with the through-wafer interconnects 814).

**[0035]** Additionally, in the illustrated embodiment connector elements 850 have been coupled to portions of the redistribution structure 840 and at least one dielectric material 844 has been applied or placed over at least a portion of the redistribution structure 840 so that the connector elements extend through or above the dielectric material 844. The dielectric material 844 can provide insulation and/or protection for the redistribution structure 840. In certain embodiments, the dielectric material 844 can be applied to the redistribution structure 840 before the connector elements 850 are coupled to the redistribution structure 840. In other embodiments, the dielectric material 844 can be applied to the redistribution structure 840 after the connector elements 850 have been coupled to the redistribution structure 840.

**[0036]** Figure 11 is a partially schematic cross-sectional view of two microelectronic devices 805, shown as a first microelectronic device 805a and a second microelectronic device 805b, in accordance with embodiments of the invention. In the illustrated embodiment, the microelectronic devices 805 were formed by cutting the arrangement shown in Figure 10 along line S-S to form the separate microelectronic device 805. As shown in Figure 11, the support member 820 has been removed from the microelectronic devices 805 (e.g., before or after singulating the microelectronic devices 805). In other embodiments, the dielectric material 844, the one or more redistribution structure 840, and/or of the connector elements 850 can be positioned on the respective microelectronic devices 805 after the microelectronic devices 805 have been separated from one another. As discussed above with reference to Figure 9, in certain embodiments a protective and/or insulative coating or covering 860 can be positioned on portions of one or more of the microelectronic devices 805.

**[0037]** As discussed above, in certain embodiments the microelectronic devices can be stacked or stackable. For example, in Figure 12 the second microelectronic device 805b, shown in Figure 11, is shown stacked with the first microelectronic device 105a, shown in Figure 8, to form a stacked unit 1107. In Figure 12, an encapsulating material 1132 has been applied to the stacked unit 1107 (e.g., on, around, and/or between the microelectronic devices 105a and 805b) to provide structural support, insulation, and/or protection for the stacked unit 1107. As discussed above, the encapsulating material 1132 can include various types of material, including dielectric materials and/or epoxies. Features and advantages of embodiments discussed above with reference to Figures 10-12 are similar to those discussed above with reference to Figures 1-9.

**[0038]** From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that various modifications may be made without deviating from the invention. For example, aspects of the invention described in the context of particular embodiments may be combined or eliminated in other embodiments. Furthermore, while advantages associated with certain embodiments of the invention have been described in the context of those embodiments, other embodiments may also exhibit such advantages, and not all embodiments need

necessarily exhibit such advantages to fall within the scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

I/We claim:

1. A method for packaging microelectronic devices, the method comprising:

coupling multiple microelectronic dies to a surface of a support member, the support member having at least one contact substantially co-planar with the surface of the support member, individual microelectronic dies each having an active side including at least one contact substantially co-planar with the active side, a backside, and at least one through-wafer interconnect, wherein the active side and the contact of the microelectronic dies abut the surface of the support member such that the substantially co-planar contact of the support member contacts the substantially co-planar contact of the active side;

applying an encapsulant to cover at least a portion of the surface of the support member so that a portion of the encapsulant is laterally adjacent to the microelectronic dies;

removing material from the backside of the microelectronic dies to expose a portion of the through-wafer interconnects; and

constructing a redistribution structure on the backside of the microelectronic dies, wherein the redistribution structure has pads electrically coupled to the through-wafer interconnects.

2. The method of claim 1, further comprising singulating the microelectronic dies to form multiple separate microelectronic devices.

3. The method of claim 1 wherein applying the encapsulant comprises filling at least a portion of space in between the microelectronic dies with the encapsulant, and wherein the method further comprises singulating the microelectronic dies by cutting the

encapsulant between the microelectronic dies to form multiple separate microelectronic devices.

4. The method of claim 1, further comprising applying a dielectric material over at least a portion of the redistribution structure.

5. The method of claim 1 wherein applying an encapsulant includes covering at least a portion of the surface of the backside of at least one of the microelectronic dies.

6. The method of claim 1 wherein applying encapsulant includes applying encapsulant to fill at least a portion of space in between the microelectronic dies.

7. The method of claim 1 wherein applying an encapsulant includes depositing an encapsulant via at least one of an over-mold method, a liquid dispense method, a film-assisted molding process, and a glob-type dispensing process.

8. The method of claim 1 wherein coupling multiple microelectronic dies to a surface of a support member includes mounting multiple microelectronic dies to a surface of a temporary support member, and wherein the method further includes removing the temporary support member from at least one of the microelectronic dies.

9. The method of claim 1, further comprising removing at least a portion of the support member from at least one of the multiple microelectronic dies.

10. The method of claim 1, further comprising:

singulating the microelectronic dies to form multiple separate microelectronic devices, the microelectronic devices including first microelectronic devices; and

stacking one of the first microelectronic device with (a) at least one other first microelectronic device, (b) at least one second microelectronic device, or (c) both (a) and (b).

11. The method of claim 1, wherein applying an encapsulant includes applying a first encapsulant, and where in the method further comprises:

singulating the microelectronic dies to form multiple separate microelectronic devices, the microelectronic devices including first microelectronic devices;

forming a stacked unit by stacking one of the first microelectronic device with (a) at least one other first microelectronic device, (b) at least one second microelectronic device, or (c) both (a) and (b); and

applying a second encapsulating material to at least a portion of the stacked unit.

12. A method for packaging a microelectronic device, the method comprising:

positioning an active side of a microelectronic die against an electrical contact substantially co-planar with a surface of a support member with a contact of the active side of the microelectronic die substantially co-planar with the active side, the microelectronic die having a backside opposite the active side, a peripheral side extending at least part way between the active side and the backside, and at least one through-wafer interconnect;

applying an encapsulant to cover at least a portion of the surface of the support member so that a portion of the encapsulant is laterally adjacent to the peripheral side and substantially no encapsulant is between the active side and the support member;

removing material from a backside of the microelectronic die to expose a portion of the through-wafer interconnect; and

constructing a redistribution structure on the backside of the microelectronic die, wherein the redistribution structure has pads electrically coupled to the through-wafer interconnect.

13. The method of claim 12 wherein applying the encapsulant includes applying the encapsulant so that the encapsulant is attached to the peripheral side of the microelectronic die.

14. The method of claim 12 wherein coupling an active side of a microelectronic die to a surface of a support member includes coupling an active side of a microelectronic die to a surface of a temporary support member, and wherein the method further includes removing at least a portion of the temporary support member from the microelectronic die.

15. The method of claim 12, further comprising removing at least a portion of the support member from the microelectronic die.

16. The method of claim 12, further comprising:

attaching connector elements to the redistribution structure; and

stacking the microelectronic device with at least one other microelectronic device.

17. The method of claim 12, further comprising:

forming a stacked unit by stacking the microelectronic device with at least one other microelectronic device; and

applying an encapsulating material to at least a portion of the stacked unit.

18. A method for packaging microelectronic devices, the method comprising:

attaching multiple microelectronic dies to a surface of a support member, the support member having at least one support contact substantially co-planar with the surface of the support member, individual microelectronic dies having an active side including at least one contact substantially co-planar with the active side, a backside, and at least one through-wafer interconnect connected to the contact, wherein the active side of the microelectronic dies contacts and is attached to the surface of the support member, and wherein the contact is electrically connected to the support contact;

applying an encapsulant to cover at least a portion of the multiple microelectronic dies and at least a portion of the surface of the support member so that a portion of the encapsulant is laterally adjacent to the microelectronic dies;

removing material from the backside of the microelectronic dies to expose a portion of the through-wafer interconnects;

constructing a redistribution structure on the backside of the microelectronic dies, wherein the redistribution structure has pads electrically coupled to the through-wafer interconnects; and

singulating the microelectronic dies.

19. The method of claim 18 wherein constructing a redistribution structure includes constructing a redistribution structure that extends over at least a part of the portion of the encapsulant laterally adjacent to the microelectronic dies.

20. The method of claim 18 wherein attaching multiple microelectronic dies to a surface of a support member includes attaching multiple microelectronic dies to a surface of a temporary support member.

21. The method of claim 18, further comprising removing at least a portion of the support member from at least one of the multiple microelectronic dies.

22. The method of claim 18 wherein attaching multiple microelectronic dies includes attaching multiple first microelectronic dies, and wherein the method further comprises stacking one of the first microelectronic device with (a) at least one other first microelectronic device, (b) at least one second microelectronic device, or (c) both (a) and (b).

23. The method of claim 18 wherein attaching multiple microelectronic dies includes attaching multiple first microelectronic dies, and wherein the method further comprises:

forming a stacked unit by stacking one of the first microelectronic device with (a) at least one other first microelectronic device, (b) at least one second microelectronic device, or (c) both (a) and (b); and

applying a second encapsulating material to at least a portion of the stacked unit.

24. A method for packaging a microelectronic device, the method comprising:

coupling an active side of a microelectronic die to a contact substantially co-planar with a surface of a support member, wherein the active side extends over substantially the lateral width of the microelectronic die and contains at least one contact at the active side, connected to integrated circuitry within the microelectronic die, and substantially co-planar with the active side;

applying an encapsulant to cover at least a portion of the microelectronic die and at least a portion of the surface of the support member so that a portion of the encapsulant is laterally adjacent to the microelectronic die and no encapsulant is between the active side and the support member;

removing material from a backside of the microelectronic die to expose a portion of at least one through-wafer interconnect; and

constructing a redistribution structure on the backside of the microelectronic die, the redistribution structure has pads electrically coupled to the through-wafer interconnect.

25. The method of claim 24, further comprising removing at least a portion of the support member from the microelectronic die.

26. The method of claim 24, further comprising stacking the microelectronic device with at least one other microelectronic device.

27. The method of claim 24 wherein applying an encapsulant includes applying a first encapsulant, and wherein the method further comprises:

forming a stacked unit by stacking the microelectronic device with at least one other microelectronic device; and

applying a second encapsulating material to at least a portion of the stacked unit.

28. The method of claim 24 wherein removing material from a backside of the microelectronic die includes removing part of the encapsulant.