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Switched-Mode Power Converter
with Triple Protection
in a Single Latch

Background and Summary of the Invention

5 This invention is related to overvoltage, overcurrent, and overtemperature protection in switching power supplies.

 The prior art techniques for overvoltage, overcurrent, and overtemperature protection are implemented using separate circuits. Each method is discussed below.

10 **Background: Switched-Mode Power Converters**

 Switched-mode power converters have many applications in industry including television and monitor power supplies. The basic application is a power supply (DC output) which achieves its output regulation by means of one or more active power handling devices
15 which are switched ON or OFF. Because the switching device, for example a switching transistor, is fully OFF or fully ON at any one time, it dissipates very little energy, and so runs coolly and efficiently. The ratio of the on-time to the off-time of the switch (duty-cycle) is varied to suit the load demand. When little energy
20 is required, the switch dwells in the ON position for only a short time during each cycle of operation. This short on-time is used to briefly "top off" an inductive and/or capacitive reservoir which supplies the load during the switch's off period. When the load's energy demand increases, a feedback/monitoring circuit automatical-
25 ly increases the duty-cycle of the switch so that it remains ON for a longer period of time in each operating cycle, and increases the energy fed to the reservoir. In this way, the energy drawn from the primary power source (usually AC mains) almost exactly matches the energy demanded by the load from instant to instant, with

minimal energy waste within the power supply itself.

This type of supply is distinguished from a "linear" or "dissipative" power supply, in which regulation is achieved by power handling devices whose conduction is varied continuously over a wide range, and whose state is seldom (if ever) in a full OFF or full ON condition.

Background: Overvoltage Protection Techniques

Overvoltage ("OV") protection is normally accomplished using a large Zener diode connected across the output (VOUT and GND, in Figure 1). During an OV fault, the Zener clamps the output to a safe voltage level and in the process draws excessive current which eventually fails to a short circuit. Correct sizing of the Zener in terms of clamping level and power dissipation is critical, because there is the danger of the Zener failing (open circuit) due to an excessive power surge. A condition may also occur where the Zener sustains its clamped mode longer than necessary and dissipates enough heat to affect operation of nearby components. Additionally, the Zener may even exceed the maximum allowable temperature rating of the printed circuit board itself.

Background: Overtemperature Protection Techniques

Overtemperature ("OT") protection is obtained using a temperature-sensitive resistor which changes in value proportional to temperature, and is connected in a voltage divider circuit. The circuit is biased by a fixed reference voltage. Changes in resistance value are translated to a change in voltage output. The output is then used to drive a comparator/driver circuit which feeds a secondary-side control loop configured to turn off the supply when an overtemperature fault occurs. The additional comparator/driver circuit adds to the complexity and cost of the circuit.

Background: Overcurrent Protection Techniques

Overcurrent ("OC") protection can be implemented in either the secondary or primary circuit. In the case of flyback topology design using current-mode pulse-width modulation ("PWM"),
5 overload protection is performed in the primary by forcing the auxiliary supply (VAUX, in Figure 1) to the PWM control circuit (U1) to decay to its Under Voltage Lock-Out ("UVLO") voltage level by closely coupling its auxiliary winding to the main secondary output voltage (VOUT). This low cost scheme does not offer fast
10 response during an output short circuit condition, and allows higher power dissipation to the switching devices (Q3 and CR3). Although the standard 384X series of current-mode PWM ICs have an inherent pulse-by-pulse current limit feature, this is insufficient to provide complete overcurrent protection because it does not
15 completely shutdown converter operation.

Alternatively, OC protection can be accomplished using a current-sense resistor or current-sense transformer connected along the secondary output current path, and as part of a complex trigger circuit. Either of these circuits offer accuracy and better response
20 than the aforementioned but are rather costly and complex.

Switched-Mode Power Converter with Triple Protection in a Single Latch

This application discloses a single circuit comprising protection against overvoltage, overcurrent, and overtemperature in an off-
25 line switched-mode power converter. The unified protection circuit meets the need for a simple and low-cost multiple protection circuit for an off-line Switched-Mode Power Supply ("SMPS") design which uses PWM control (preferably current-mode PWM control). A single latch element (preferably a bistable device structure, such
30 as a thyristor-connected PNP+NPN pair) provides PWM control for all three protection circuit functions. Any of the three abnormal

conditions can set the latch element, and the latch element will shut down the PWM controller when it is set. Preferably the latch is reset, once set, by timing elements which combine with one of the PWM outputs.

- 5 An advantage is that the circuit is ideally suited to work with the industry standard 384X-series of current-mode PWM controllers typically used in a flyback converter. Another advantage is that the circuit is easily implemented because it allows independent triggering of the latch driver from all three abnormal conditions. Another
10 advantage is that it uses the minimum number of low cost components while providing full protection from overvoltage, overcurrent, and overtemperature conditions. Another advantage is that the circuit reacts much faster to a short circuit condition, thereby significantly reducing the power dissipation of the switching device.
15 Another advantage is that the reduction in thermal load translates into improved device reliability.

- To implement the three basic circuit protection functions of overvoltage, overcurrent, and overtemperature in a unified circuit by conventional methods would require a minimum dual comparator
20 IC, dual-level reference voltages, an optoisolator to couple the fault signal to the primary circuit, and a number of resistors and capacitors. The set of components adds cost, occupies more space, and decreases circuit reliability. However, in a flyback design, reduced cost can be achieved by using individual protection circuits
25 for each protection function, and may be implemented in both the primary and secondary sides of the circuit. The problem when using such scheme is performance degradation.

Brief Description of the Drawings

The disclosed inventions will be described with reference to the accompanying drawings, which show important sample embodiments of the invention and which are incorporated in the specification hereof by reference, wherein:

Figure 1 shows a circuit diagram of a power converter according to the presently preferred embodiment.

Figure 2 shows a block diagram of a portable computer system according to the presently preferred embodiment.

Figure 3 shows overcurrent circuit waveforms during normal operation and when a fault occurs.

Figure 4 shows overvoltage circuit waveforms during normal operation and when a fault occurs.

Detailed Description of the Preferred Embodiments

The numerous innovative teachings of the present application will be described with particular reference to the presently preferred embodiment. However, it should be understood that this class of
5 embodiments provides only a few examples of the many advantageous uses of the innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not
10 to others.

Flyback Power Converter Overview

"Flyback" converters are a class of power converter topology which are common in off-line adapters (*e.g.* in battery chargers). During the power transistor on time, energy is stored in a power
15 transformer while load current is supplied from an output filter capacitor. When the power transistor turns off, the energy stored in the power transformer is transferred to the output as load current, and to the filter capacitor to replenish the charge lost when it alone was delivering load current.

20 In this configuration, as shown in **Figure 1**, a switching transistor **Q3** switches the primary L_p of a transformer **T1**. Each of the secondary windings L_s of the transformer **T1** is connected through flyback diodes **CR3** to an output capacitor **C122**. Thus, while the switching transistor **Q3** is ON, the current through the
25 primary increases (storing energy in the transformer), and when the switch **Q3** is opened, the stored energy is discharged at the transformer secondary through the flyback diodes **CR3**. Feedback is provided through the optoisolator **U102** to the PWM chip **U1**.

The Unified Protection Circuit

The heart of the all-in-one protection circuit **101** is the sense and latch circuit combination using resistive-divider circuits and two general-purpose bipolar transistors (in a monolithic package) configured to allow regenerative feedback. Figure 1 shows a circuit diagram of a power circuit according to the presently preferred embodiment (a typical off-line flyback topology SMPS design using current-mode PWM control). Chip U1 is the PWM control IC (which among its functions) has a primary current-sense input pin (**Is**, pin 3) used to control the primary peak current. Additionally, together with its internal PWM comparator and latch circuits, chip U1 indirectly controls the output voltage constant. Resistors **R1**, **R2**, **R3**, **R4**, and transistors **Q1** and **Q2** form a discrete implementation of a latch circuit biased by a +5-volt reference **+5VREF** from chip U1. Adding thermistor **RT1** at the junction of **R1**, **R2**, and base pin of **Q1**, forms the OT sense circuit.

During an OT condition, the power supply is cycled ON and OFF until the power supply temperature decreases to an acceptable level. However, if the condition persists, driving the temperature back up, the cycling will continue. Thermistor **RT1** resistance decreases to a value sufficient to cause the voltage at node **R** (junction of **R1**, **R2**, and base of **Q1**) to decrease to approximately 4.3V. This drops approximately 0.7 volt across the base-emitter of **Q1**, effectively turning it ON. During this time, voltage reference **+5VREF** is applied to the base of transistor **Q2** through resistors **R3** and **R4**, turning **Q2** ON as well. Transistor **Q2** then pulls the base voltage of **Q1** (through **R2**) even lower, ensuring its ON state (latched mode), and at the same time pulling voltage at the cathode of diode **CR2** to the voltage level of **PRI RTN**, forward biasing diode **CR2**. This brings the **COMP** pin (pin 1) of U1 low, effectively stopping the operation of U1 and the converter. This condition will persist until reference **+5VREF** decays to zero, when

UVLO level of U1 is reached, and the latch circuit is reset. The power supply then cycles ON and OFF until the OT condition is removed.

During an OV condition, the power supply will cycle ON and
5 OFF until the AC mains power is removed. However, during the
cycling, the converter is protected from catastrophic failure (the
main switching components blowing up) due to the reduced power
dissipation. The OV condition is sensed by Zener CR1 which is
sized according to the desired OV level. For flyback topology
10 designs, the output voltages track one another through the coupled
windings, such that it allows the use of the primary referenced
VAUX to provide secondary OV protection. The threshold level for
OV detect is the sum of the Vbe of Q2, the small voltage drop
across R5, and the CR1 Zener voltage. The threshold level voltage,
15 when multiplied by the transformer (T1) turns ratio, provides the
desired main output OV level. When diode CR1 conducts sufficient
current to make transistor Q2 Vbe reach approximately 0.7 volt, Q2
turns ON and pulls the base of transistor Q1 low to turn it ON.
Transistor Q1 then provides the latching current. Diode CR2 is
20 again forward biased pulling chip U1 COMP pin low, thereby
shutting down PWM operation and the converter.

During an OC condition, the power supply will cycle ON and
OFF until the fault is removed. Again, the converter is protected
from catastrophic failure due to the reduced power dissipation. For
25 current-mode PWM control, the primary peak current is sensed and
converted to voltage through R7 in the circuit diagram. The low
level voltage across R7 is used by U1 (pin 3) through R116 as an
input to its internal PWM comparator. By connecting R6 between
the base of Q2 and the output of R7, the overcurrent-sense circuit
30 is created. For the standard 384X series of PWM ICs, the maxi-
mum voltage input at the current sense input (Is) pin 3 to indicate
maximum peak current, is approximately 1.0 volt. At this level, the

converter will be in a worst case maximum output power condition. Chip U1 will be at the verge of pulse-by-pulse current limiting. To provide adequate noise margin for Q2 and prevent false triggering of the latch circuit at full load, resistor R7 is sized such that at the
5 peak output load condition, the voltage across it is less than the minimum V_{beON} of transistor Q2 at the maximum operating temperature. Additionally, capacitor C1 filters noise. Resistor R9 along with R10 and R11, provide voltage compensation to pin 3 of U1 and restores the 1.0 V limit. Thus during the OC (or short
10 circuit) condition, the resulting voltage across R7 will turn transistor Q2 ON (through R6) and activate the latch circuit. The circuit reacts much faster to a short circuit condition, and thereby significantly reduces the power dissipation of the switching device. This reduction in thermal load translates into improved reliability.

15 Computer Embodiment

Figure 2 shows a portable computer utilizing the innovative protection architecture. The system includes a power converter 205 which is used to charge a battery 215. Optionally, a battery interface 210 is interposed between the battery and the rest of the
20 circuitry. The power converter 205 is connected, through a full-wave bridge rectifier, 200, to draw power from AC mains, and is connected to provide a DC voltage to the battery 215. The battery 215 (or the converter 205), connected through a voltage regulator 220, is able to power the complete portable computer system, which
25 includes in this example:

user input devices (*e.g.* keyboard 235 and mouse 240);
at least one microprocessor 225 which is operatively connected to
 receive inputs from said input device, through an interface
 manager chip 230 (which also provides an interface to the
30 various ports);
a memory (*e.g.* flash or non-volatile memory 255 and RAM 260),

- which is accessible by the microprocessor;
a data output device (*e.g.* display 250 and video display adapter card 245) which is connected to output data generated by the microprocessor 225; and
5 a magnetic disk drive 270 which is read-write accessible, through an interface unit 265, by the microprocessor 225.

Optionally, of course, many other components can be included, and this configuration is not definitive by any means. For example, the portable computer may also include a CD-ROM drive
10 280 and floppy disk drive ("FDD") 275 which may interface to the disk interface controller 265. Additionally, L2 cache 285 may be added to speed data access from the disk drives to the microprocessor, and a PCMCIA 290 slot accommodates peripheral enhancements.

15 Normal Operation and Fault Condition Waveforms

Figure 3 shows overcurrent circuit waveforms during normal operation and when a fault occurs. Reference channel 300 shows the normal drain-source switching voltage waveform of transistor Q3 with a duty cycle of approximately 18.3%. Channel 301 shows a
20 waveform obtained at the same node during an overcurrent fault condition. The duty cycle has changed to 3.6%, the result of which is a negligible heat dissipation of both the switching devices, transistor Q3 and diode CR3.

Figure 4 shows overvoltage circuit waveforms during normal
25 operation and when a fault occurs. Reference channel 400 shows the normal level of VOUT at approximately 18.8 volts. Channel 401 shows the output waveform during an overvoltage fault where the output voltage VOUT is limited to approximately 21.8 volts, and the converter cycles ON (402) and OFF (403).

According to a disclosed class of innovative embodiments, there is provided: a power supply circuit, comprising: a switched-mode power conversion circuit; a pulse-width modulator circuit operatively connected to apply drive pulses to operate said conversion circuit, and connected to be controlled by feedback signals received at a modulator voltage input and a modulator current input; and a latching circuit which is operatively connected to detect overvoltage, overtemperature, and overcurrent conditions in said power conversion circuit, and which is connected to shut down said modulator circuit by driving said modulator voltage input during an overvoltage or overtemperature condition, and connected to shut down said modulator circuit by driving said modulator current input during an overcurrent condition.

According to a another disclosed class of innovative embodiments, there is provided: a power supply protection circuit, comprising: a switched-mode power conversion circuit; a pulse-width modulator circuit operatively connected to apply drive pulses to operate said conversion circuit; a latch which is operatively connected to disable said modulator circuit whenever said latch is in a set condition; an overvoltage protection circuit connected to set said latch when an overvoltage condition occurs; an overtemperature protection circuit connected to set said latch when an overtemperature condition occurs; and an overcurrent protection circuit connected to set said latch when an overcurrent condition occurs.

According to a another disclosed class of innovative embodiments, there is provided: a method for overcurrent, overvoltage, and overtemperature protection in a power supply, comprising the steps of: (a.) providing a switched-mode power conversion circuit for (b.) operating said switched-mode power conversion circuit with a pulse-width modulator circuit; and (c.) disabling said modulator circuit with a latching circuit when said overvoltage, overtemperature, or

overcurrent condition occurs.

According to a another disclosed class of innovative embodiments, there is provided: a computer system, comprising: a user input device, a microprocessor which is operatively connected to
5 detect inputs from said input device, random-access memory which is connected to be read/write accessible by said microprocessor, and an output device operatively connected to receive outputs from said microprocessor; and a power supply connected to provide power to said computer system, said power supply comprising a
10 switched-mode power conversion circuit; a pulse-width modulator circuit operatively connected to apply drive pulses to operate said conversion circuit, and connected to be controlled by feedback signals received at a modulator voltage input and a modulator current input; and a latching circuit which is operatively connected
15 to detect overvoltage, overtemperature, and overcurrent conditions in said power conversion circuit, and which is connected to shut down said modulator circuit by driving said modulator voltage input during an overvoltage or overtemperature condition, and connected to shut down said modulator circuit by driving said modulator
20 current input during an overcurrent condition.

Modifications and Variations

As will be recognized by those skilled in the art, the innovative concepts described in the present application can be modified and varied over a tremendous range of applications, and
25 accordingly the scope of patented subject matter is not limited by any of the specific exemplary teachings given.

For example, the disclosed protection circuitry can be combined with many other PWM controller chips.

For example, the disclosed protection circuitry can also be
30 used with converter topologies other than flyback, such as Forward Mode topologies and all derivatives thereof.

Of course, in implementing power supply circuits and systems, safety is a very high priority. Those of ordinary skill in the art will therefore recognize the necessity to review safety issues carefully, and to make any changes in components or in circuit
5 configuration which may be necessary to improve safety or to meet safety standards in various countries.



CLAIMS

What is claimed is:

- 1 1. A power supply circuit, comprising:
 - 2 a switched-mode power conversion circuit;
 - 3 a pulse-width modulator circuit operatively connected to apply
 - 4 drive pulses to operate said conversion circuit, and
 - 5 connected to be controlled by feedback signals received at
 - 6 a modulator voltage input and a modulator current input;
 - 7 and
 - 8 a latching circuit which is operatively connected to detect
 - 9 overvoltage, overtemperature, and overcurrent conditions
 - 10 in said power conversion circuit, and which is
 - 11 connected to shut down said modulator circuit by driving said
 - 12 modulator voltage input during an overvoltage or
 - 13 overtemperature condition, and
 - 14 connected to shut down said modulator circuit by driving said
 - 15 modulator current input during an overcurrent condi-
 - 16 tion.
- 1 2. The circuit of Claim 1, wherein said power supply circuit embod-
2 ies flyback topology.
- 1 3. The circuit of Claim 1, wherein said latch comprises a bistable
2 semiconductor device structure.
- 1 4. The circuit of Claim 1, wherein said latching circuit cycles power
2 on and off when in an overtemperature condition.



- 1 5. The circuit of Claim 1, wherein said latching circuit cycles power
2 on and off when in an overvoltage or overcurrent condition.
- 1 6. The circuit of Claim 1, wherein said pulse-width modulator resets
2 said latching circuit.
- 1 7. The circuit of Claim 1, wherein said modulator, in response to
2 said latch, cycles on and off when an overtemperature
3 condition occurs.
- 1 8. A power supply protection circuit, comprising:
2 a switched-mode power conversion circuit;
3 a pulse-width modulator circuit operatively connected to apply
4 drive pulses to operate said conversion circuit;
5 a latch which is operatively connected to disable said modulator
6 circuit whenever said latch is in a set condition;
7 an overvoltage protection circuit connected to set said latch when
8 an overvoltage condition occurs;
9 an overtemperature protection circuit connected to set said latch
10 when an overtemperature condition occurs; and
11 an overcurrent protection circuit connected to set said latch when
12 an overcurrent condition occurs.
- 1 9. The circuit of Claim 8, wherein said power supply circuit embod-
2 ies flyback topology.
- 1 10. The circuit of Claim 8, wherein said latch comprises a bistable
2 semiconductor device structure.
- 1 11. The circuit of Claim 8, wherein said latch cycles power on and
2 off when in an overtemperature condition.



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1 12. The circuit of Claim 8, wherein said latching circuit cycles
2 power on and off when in an overvoltage or overcurrent
3 condition.

1 13. The circuit of Claim 8, wherein said pulse-width modulator
2 resets said latch.

1 14. The circuit of Claim 8, wherein said modulator, in response to
2 said latch, cycles on and off when an overtemperature
3 condition occurs.

1 15. A method for overcurrent, overvoltage, and overtemperature
2 protection in a power supply, comprising the steps of:
3 (a.) providing a switched-mode power conversion circuit for
4 (b.) operating said switched-mode power conversion circuit with
5 a pulse-width modulator circuit; and
6 (c.) disabling said modulator circuit with a latching circuit when
7 said overvoltage, overtemperature, or overcurrent condi-
8 tion occurs.

1 16. The method of Claim 15, wherein said power supply circuit
2 embodies flyback topology.

1 17. The method of Claim 15, wherein said latch comprises a
2 bistable semiconductor device structure.

1 18. The method of Claim 15, wherein said latching circuit cycles
2 power on and off when in an overtemperature condition.



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- 1 19. The method of Claim 15, wherein said latching circuit cycles
2 power on and off when in an overvoltage or overcurrent
3 condition.
- 1 20. The method of Claim 15, wherein said pulse-width modulator
2 resets said latching circuit.
- 1 21. The method of Claim 15, wherein said modulator, in response
2 to said latching circuit, cycles on and off when an
3 overtemperature condition occurs.



- 1 22. A computer system, comprising:
2 a user input device, a microprocessor which is operatively con-
3 nected to detect inputs from said input device, random-
4 access memory which is connected to be read/write acces-
5 sible by said microprocessor, and an output device
6 operatively connected to receive outputs from said
7 microprocessor; and
8 a power supply connected to provide power to said computer
9 system, said power supply comprising
10 a switched-mode power conversion circuit;
11 a pulse-width modulator circuit operatively connected to apply
12 drive pulses to operate said conversion circuit, and
13 connected to be controlled by feedback signals received
14 at a modulator voltage input and a modulator current
15 input; and
16 a latching circuit which is operatively connected to detect
17 overvoltage, overtemperature, and overcurrent condi-
18 tions in said power conversion circuit, and which is
19 connected to shut down said modulator circuit by driving said
20 modulator voltage input during an overvoltage or
21 overtemperature condition, and
22 connected to shut down said modulator circuit by driving said
23 modulator current input during an overcurrent condi-
24 tion.
- 1 23. The system of Claim 22, wherein said power supply circuit
2 embodies flyback topology.
- 1 24. The system of Claim 22, wherein said latching circuit comprises
2 a bistable semiconductor device structure.



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- 1 25. The system of Claim 22, wherein said latching circuit cycles
2 power on and off when in an overtemperature condition.
- 1 26. The system of Claim 22, wherein said latching circuit cycles
2 power on and off when in an overvoltage or overcurrent
3 condition.
- 1 27. The system of Claim 22, wherein said pulse-width modulator
2 resets said latching circuit.
- 1 28. The system of Claim 22, wherein said modulator, in response
2 to said latching circuit, cycles on and off when an
3 overtemperature condition occurs.