METHOD FOR MAKING SELF-ALIGNED CONTACTS TO SOURCE/DRAIN WITHOUT HARD MASK LAYER

ABSTRACT

An improved and new process for fabricating self-aligned contacts (SAC) to source/drain areas of complimentary (CMOS) FET's has been developed using a non-conformal layer of silicon nitride, eliminating the need for a hard mask. This process allows for "zero" spacing from contact structure to polysilicon gate structure, for closely spaced design rule gates. Some key process features of this invention are as follows: no hard mask is needed and the gate process is exactly the same as "standard" logic process. The process differences are that between the S/D implant, salicidation and the normal contact process, there is inserted a non-conformal CVD silicon nitride deposition with a SAC pattern and etch process. The process is fully compatible with both state of-the-art salicide and polycide processes. The self-aligned contact process simplifies processing, while yielding improvements in electrical device performance and reliability. The process is very useful for the "standard" logic device salicided processes.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)