FIG. 1

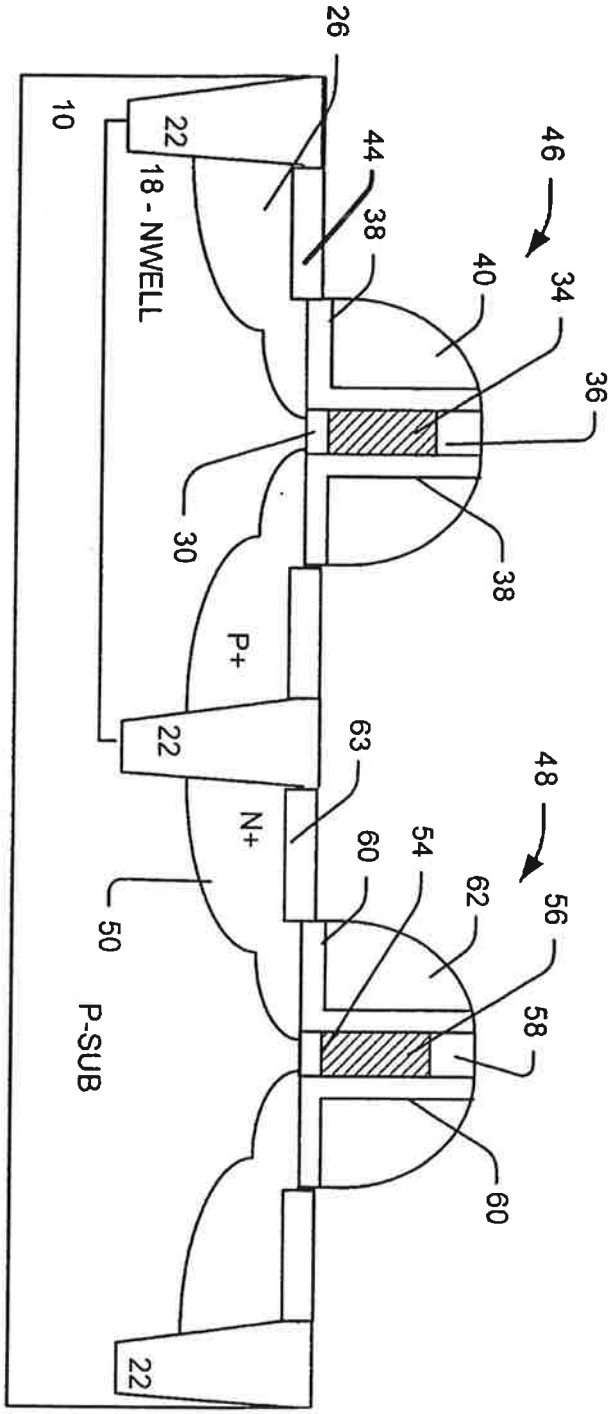

26
22
18 - NWELL
10
44
38
46
40
34
36
30
38
P+
22
63
48
N+
60
54
62
56
58
50
P-SUB
60
22
PFET 14
NFET 12

FIG. 2

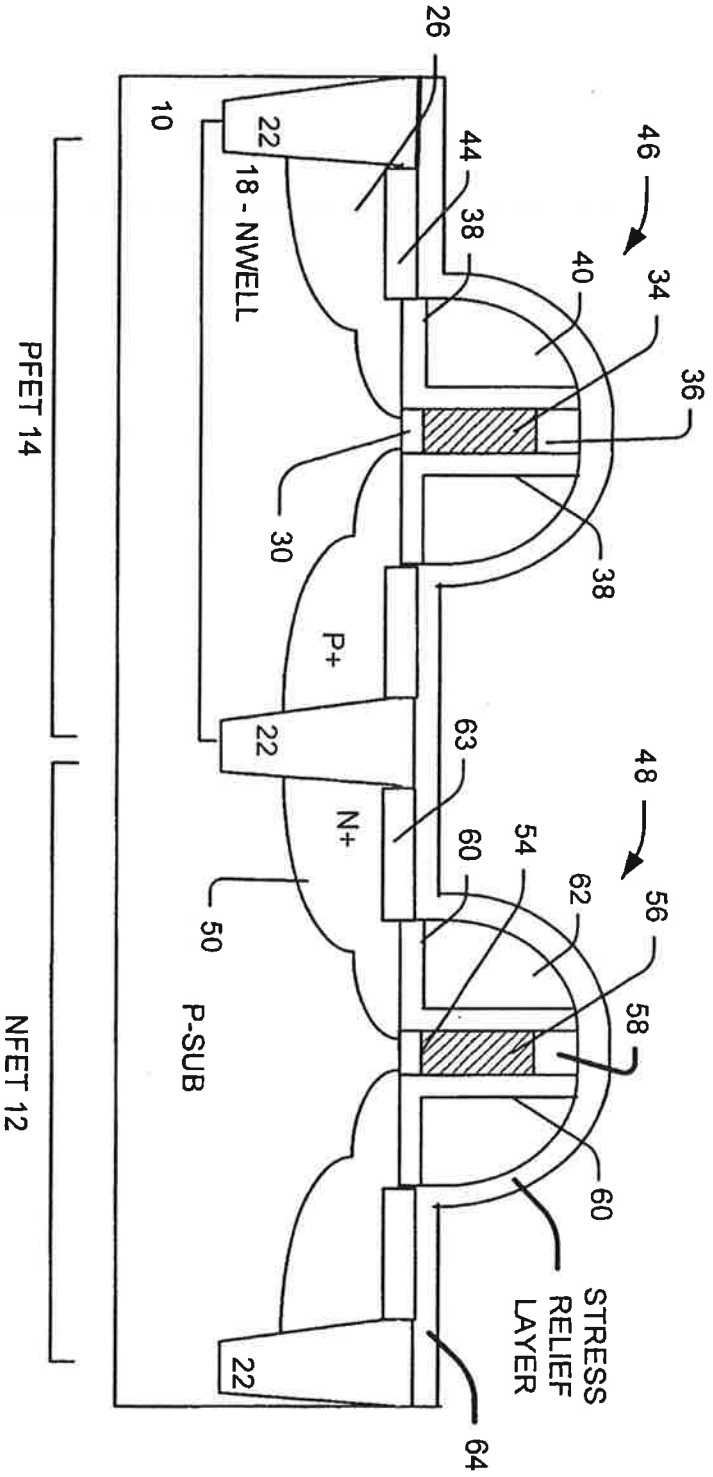

26
10
22
18 - NWELL
44
38
46
40
34
36
30
38
P+
22
63
48
N+
60
54
62
56
50
58
P-SUB
60
STRESS
RELIEF
LAYER
22
64
PFET 14
NFET 12

FIG. 3

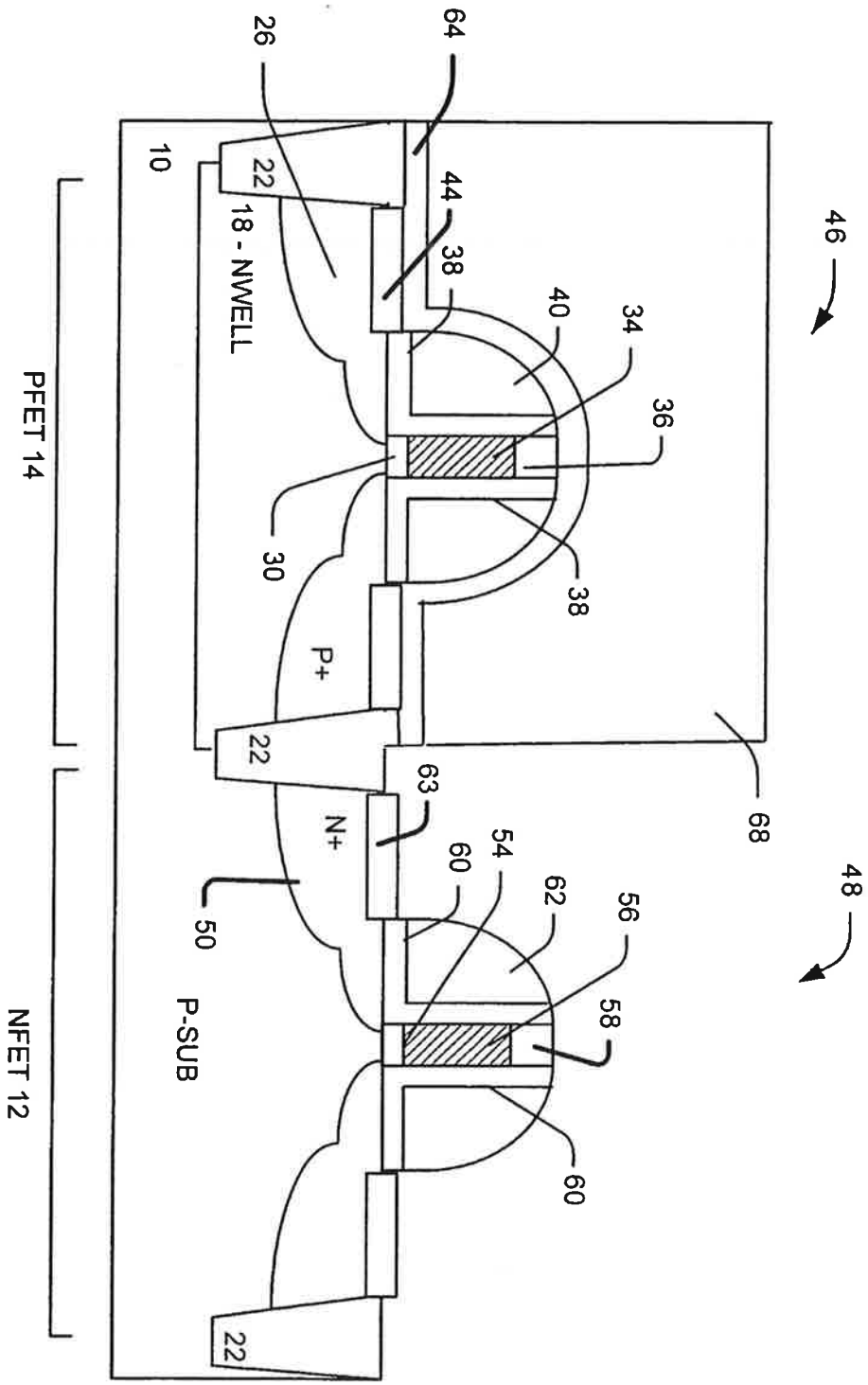

64
26
22
10
18 - NVELL
44
38
40
34
36
30
38
P+
22
63
N+
50
P-SUB
60
54
62
56
58
60
22
68
46
48
PFET 14
NFET 12

FIG. 4

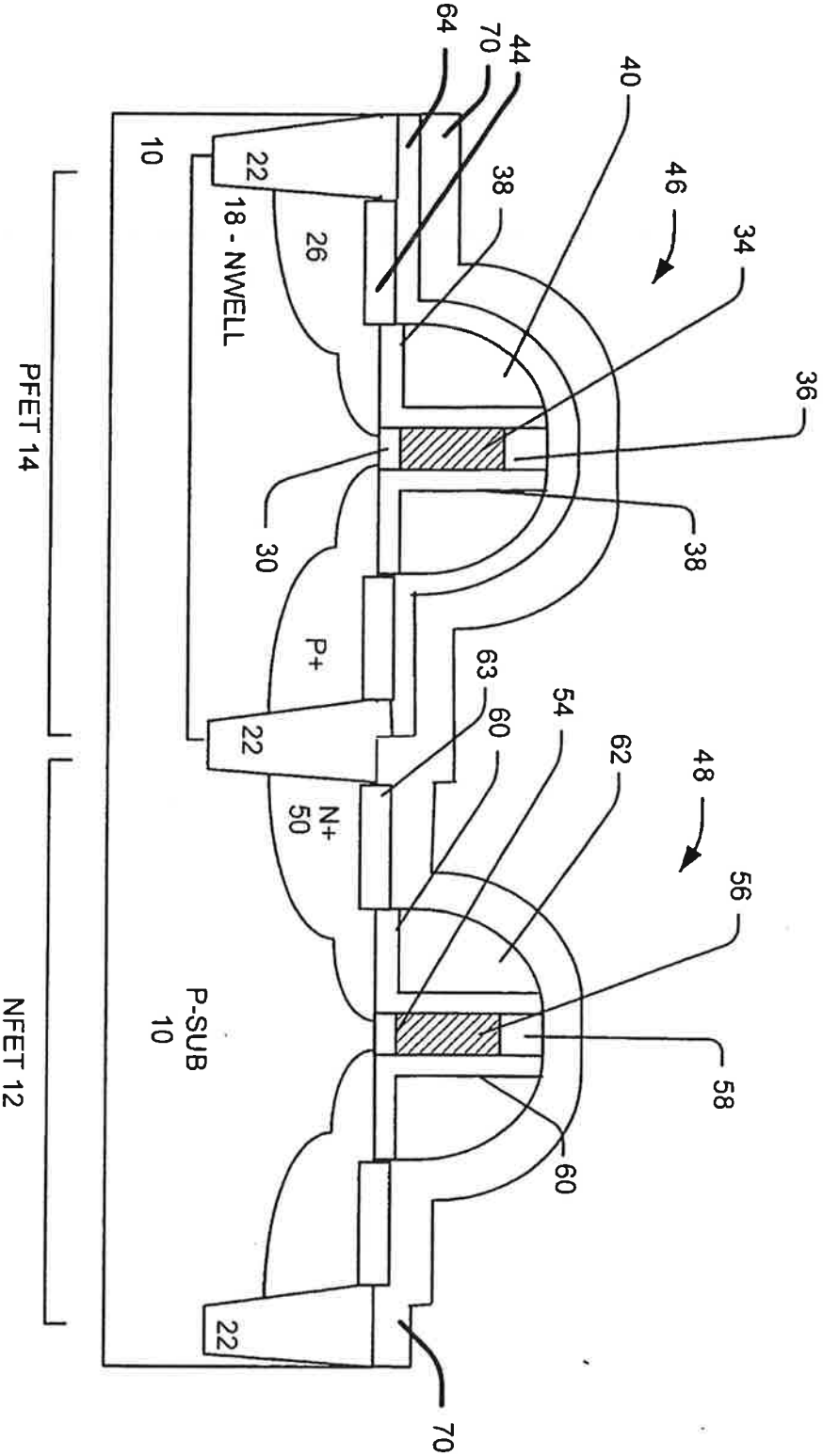
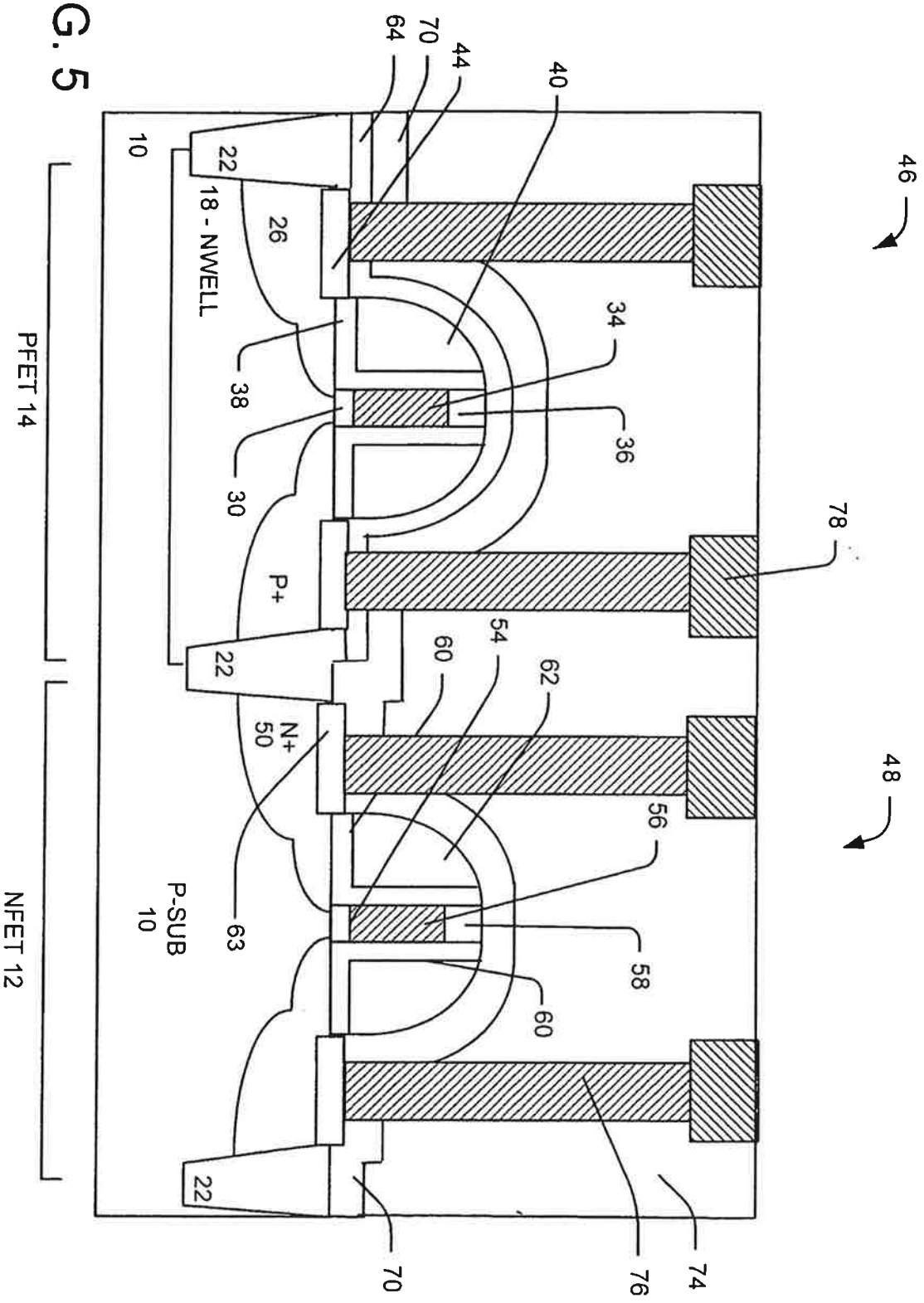

64
70
44
40
46
34
36
38
22
18 - NWELL
26
10
30
38
P+
63
60
54
62
48
22
N+
50
56
58
P-SUB
10
60
22
70
PFET 14
NFET 12

FIG. 5


PFET 14
NFET 12
10
22
18 - NVELL
26
38
30
P+
22
N+
50
63
P-SUB
10
22
64
70
44
40
34
36
78
54
60
62
56
58
60
70
76
74
46
48

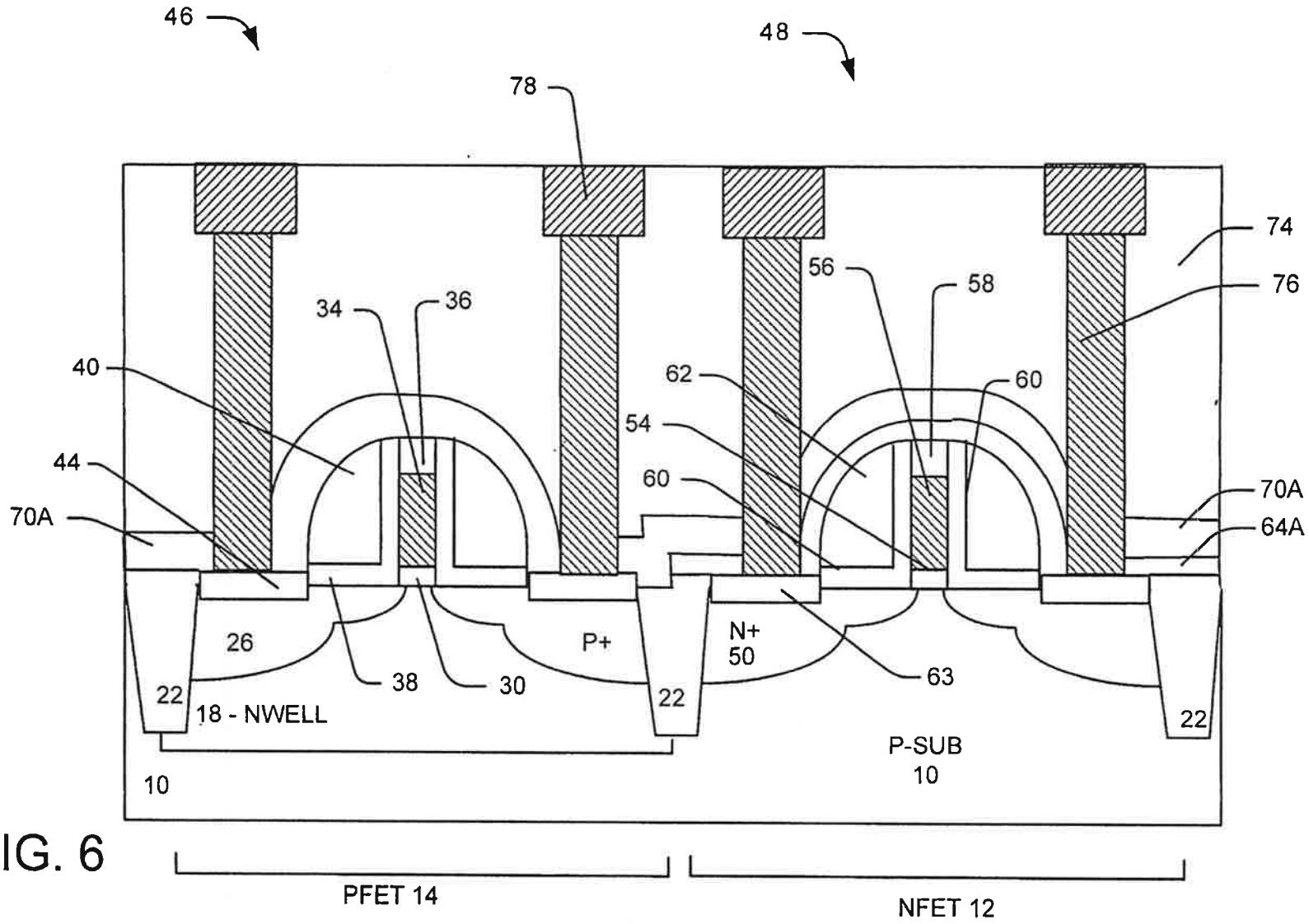

46
48
78
74
56
58
76
34
36
40
62
60
54
44
60
70A
70A
64A
26
P+
N+
50
38
30
63
22
18 - NWELL
22
22
P-SUB
10
10
PFET 14
NFET 12

FIG. 6