

SEMICONDUCTOR MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of
5 priority from the prior Japanese Patent Application No.
2010-061153, filed on March 17, 2010; No. 2010-143666, filed
on June 24, 2010; the entire contents of all of which are
incorporated herein by reference.

10 FIELD

Embodiments described herein relate generally to a
semiconductor memory device.

BACKGROUND

15 Methods for high integration of semiconductor memory
devices (memory) include a method of using sidewall patterning
technology to form a data transfer line connected to a memory
cell such that the width of the data transfer line is half the
minimum dimension of the lithography. However, in such a
20 method, the fluctuation of the width of the mask pattern of the
lithography may cause, for example, a wide interconnect width
and a narrow interconnect width to occur alternately in adjacent
interconnects. Therefore, the interconnect resistance
undesirably fluctuates between the interconnects.

25 Particularly for interconnects having narrow interconnect
widths, the read-out speed decreases and the read-out margin
decreases as the interconnect delay of the electrical signal
increases. As the interconnect resistance increases,
electromigration and stress induced migration occur easily; and
30 the reliability of the semiconductor memory device deteriorates.

Furthermore, in the case where the voltage applied to
the data transfer line is constant, the current flowing through
the memory cell farthest from a sense amplifier circuit
decreases to reduce the read-out speed because the series
35 resistance of the data transfer line is added one upon another in
the memory cell.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic view illustrating the configuration of a semiconductor memory device according to a first embodiment;

FIG. 2 is a block diagram illustrating the configuration of the semiconductor memory device of a first example;

FIG. 3 is a schematic circuit diagram illustrating the configuration of the semiconductor memory device of the first example;

FIGS. 4A and 4B are schematic views illustrating the configuration of the semiconductor memory device of the first example;

FIGS. 5A and 5B are schematic cross-sectional views illustrating the configuration of the semiconductor memory device of the first example;

FIG. 6 is a schematic plan view illustrating the configuration of the semiconductor memory device of the first example;

FIGS. 7A and 7B are schematic cross-sectional views illustrating the configuration of the semiconductor memory device of the first example;

FIGS. 8A to 8C are schematic cross-sectional views in order of the processes, illustrating a method for constructing the data transfer lines of the semiconductor memory device of the first example;

FIGS. 9A to 9C are schematic cross-sectional views in order of the processes, illustrating the method for constructing the data transfer lines of the semiconductor memory device of the first example;

FIG. 10 is a schematic circuit diagram illustrating the configuration of a semiconductor memory device of a comparative example;

FIG. 11 is a schematic plan view illustrating the configuration of a semiconductor memory device of a second example;

FIG. 12 is a schematic plan view illustrating the configuration of a semiconductor memory device of a third example;

5 FIG. 13 is a schematic view illustrating the configuration of a semiconductor memory device according to a second embodiment;

FIG. 14 is a schematic circuit diagram illustrating the configuration of a semiconductor memory device of a fourth example;

10 FIG. 15 is a schematic plan view illustrating the configuration of the semiconductor memory device of the fourth example;

FIG. 16 is a block diagram illustrating the configuration of a semiconductor memory device according to a third embodiment;

FIG. 17 is a schematic circuit diagram illustrating the configuration of the semiconductor memory device according to the third embodiment;

20 FIGS. 18A and 18B are schematic views illustrating the read timing in the case where read-out is performed when there is a difference in interconnect resistance;

FIG. 19 is a flowchart illustrating the reading of data;

FIGS. 20A to 20C are schematic views illustrating the read timing in the case where read-out is performed when there is a difference in interconnect resistance;

FIG. 21 is a flowchart illustrating the reading of data;

FIG. 22 is a schematic circuit diagram illustrating a layout of a memory cell array and a data transfer line;

30 FIG. 23 is a block diagram illustrating the configuration of a semiconductor memory device according to a fourth embodiment;

FIG. 24 is a schematic circuit diagram illustrating the configuration of the semiconductor memory device according to the fourth embodiment;

35 FIG. 25 is a schematic graph illustrating the current-voltage characteristics of a memory cell;

FIG. 26 is a block diagram illustrating the configuration of a semiconductor memory device according to a fifth embodiment;

5 FIG. 27A is a schematic view illustrating an arrangement of sense amplifier circuits, memory cell units, and the like, and FIGS. 27B and 27C are schematic views illustrating the read timing in the case where read-out is performed when there is a difference in interconnect resistance;

10 FIG. 28A is a schematic circuit diagram illustrating a layout of a memory cell array and a data transfer line, and FIG. 28B is a schematic graph illustrating the voltage of the data transfer line at the time of reading; and

15 FIG. 29A is a schematic circuit diagram illustrating a layout of a memory cell array and a data transfer line, and FIG. 29B is a schematic graph illustrating the voltage of the data transfer line at the time of reading.

DETAILED DESCRIPTION

20 In general, according to one embodiment, a semiconductor memory device includes a memory cell array, a first sense amplifier circuit, and a second sense amplifier circuit. The memory cell array includes a plurality of first memory cell units, a plurality of second memory cell units, a plurality of first interconnects, and a plurality of second interconnects. Each of
25 the plurality of first memory cell units includes a plurality of memory cells. Each of the plurality of second memory cell units includes a plurality of memory cells. The first sense amplifier circuit is connected to the plurality of first interconnects. The second sense amplifier circuit is connected
30 to the plurality of second interconnects. Each of the plurality of first interconnects is extended in a first direction and connected to one end of each of the first memory cell units. Each of the plurality of second interconnects is extended in the first direction in each space between the first interconnects and
35 connected to one end of each of the second memory cell units. A metal is formed to be embedded in an insulating film, and

heights of upper surfaces of interconnects are equal. The plurality of first interconnects and the plurality of second interconnects formed adjacent to each other are formed of a structure in which a plurality of pairs are repeated. At least one of a width of each of the plurality of second interconnects along a second direction perpendicular to the first direction and a thickness of each of the plurality of second interconnects along a third direction perpendicular to the first direction and the second direction is set smaller than each of the plurality of first interconnects, and the first sense amplifier circuit and the second sense amplifier circuit are disposed to face each other across the memory cell array.

According to another embodiment, a semiconductor memory device includes a memory cell array, a first sense amplifier circuit, and a second sense amplifier circuit. The memory cell array includes a plurality of first memory cell units, a plurality of second memory cell units, a plurality of first interconnects, and a plurality of second interconnects. Each of the plurality of first memory cell units includes a plurality of memory cells. Each of the plurality of second memory cell units includes a plurality of memory cells. The first sense amplifier circuit is connected to the plurality of first interconnects. The second sense amplifier circuit is connected to the plurality of second interconnects. Each of the plurality of first interconnects is extended in a first direction and connected to one end of each of the first memory cell units. Each of the plurality of second interconnects is extended in the first direction in each space between the first interconnects and connected to one end of each of the second memory cell units. A metal is formed to be embedded in an insulating film, and heights of upper surfaces of interconnects are equal. The plurality of first interconnects and the plurality of second interconnects formed adjacent to each other are formed of a structure in which a plurality of pairs are repeated. The first sense amplifier circuit and the second sense amplifier circuit are formed on one side of the memory cell array. The first sense

amplifier circuit is formed nearer to the memory cell array than the second sense amplifier circuit. Data of the plurality of memory cells included in the plurality of first memory cell units is output earlier than data of the plurality of memory cells included in the plurality of second memory cell units.

According to yet another embodiment, a semiconductor memory device includes a memory cell array, a sense amplifier circuit, a switching circuit, and a control circuit. The memory cell array including a plurality of first memory cell units, a plurality of second memory cell units, a plurality of first interconnects, and a plurality of second interconnects. Each of the plurality of first memory cell units includes a plurality of memory cells. Each of the plurality of second memory cell units includes a plurality of memory cells. The sense amplifier circuit is connected to the plurality of first interconnects and the plurality of second interconnects. The switching circuit is configured to switch between a connection of the sense amplifier circuit with the plurality of first interconnects and a connection of the sense amplifier circuit with the plurality of second interconnects. Each of the plurality of second interconnects is extended in the first direction in each space between the first interconnects and connected to one end of each of the second memory cell units. The control circuit outputs data of the plurality of memory cells included in the plurality of first memory cell units earlier than data of the plurality of memory cells included in the plurality of second memory cell units.

According to yet another embodiment, a semiconductor memory device includes a memory cell array, a first sense amplifier circuit, and a second sense amplifier circuit. The memory cell array includes a plurality of first memory cell units, a plurality of second memory cell units, a plurality of first interconnects, and a plurality of second interconnects. Each of the plurality of first memory cell units includes a plurality of memory cells. Each of the plurality of second memory cell units includes a plurality of memory cells. The first sense

amplifier circuit is connected to the plurality of first interconnects. The second sense amplifier circuit is connected to the plurality of second interconnects. Each of the plurality of first interconnects is extended in a first direction and
5 connected to one end of each of the first memory cell units. Each of the plurality of second interconnects is extended in the first direction in each space between the first interconnects and connected to one end of each of the second memory cell units. A metal is formed to be embedded in an insulating film, and
10 heights of upper surfaces of interconnects are equal. The plurality of first interconnects and the plurality of second interconnects formed adjacent to each other are formed of a structure in which a plurality of pairs are repeated. The first sense amplifier circuit and the second sense amplifier circuit are
15 disposed to face each other across the memory cell array. A voltage charging a first interconnect with the first sense amplifier circuit and a voltage charging a second interconnect with the second sense amplifier circuit vary with a position of the first memory cell unit and a position of the second memory
20 cell unit when read-out of the memory cell is performed.

According to yet another embodiment, a semiconductor memory device includes a memory cell array, a first sense amplifier circuit, and a second sense amplifier circuit. The memory cell array includes a plurality of first memory cell units,
25 a plurality of second memory cell units, a plurality of first interconnects, and a plurality of second interconnects. Each of the plurality of first memory cell units includes a plurality of memory cells. Each of the plurality of second memory cell units includes a plurality of memory cells. The first sense
30 amplifier circuit is connected to the plurality of first interconnects. The second sense amplifier circuit is connected to the plurality of second interconnects. Each of the plurality of first interconnects is extended in a first direction and connected to one end of each of the first memory cell units.
35 Each of the plurality of second interconnects is extended in the first direction in each space between the first interconnects and

connected to one end of each of the second memory cell units. A metal is formed to be embedded in an insulating film, and heights of upper surfaces of interconnects are equal. The plurality of first interconnects and the plurality of second
5 interconnects formed adjacent to each other are formed of a structure in which a plurality of pairs are repeated. The first sense amplifier circuit and the second sense amplifier circuit are formed on one side of the memory cell array. A voltage
10 charging the first interconnect with the first sense amplifier circuit and a voltage charging the second interconnect with the second sense amplifier circuit vary with a position of the first memory cell unit and a position of the second memory cell unit when read-out of the memory cell is performed.

According to yet another embodiment, a semiconductor
15 memory device includes a memory cell array, a sense amplifier circuit, and a switching circuit. The memory cell array includes a plurality of first memory cell units, a plurality of second memory cell units, a plurality of first interconnects, and a plurality of second interconnects. Each of the plurality of first
20 memory cell units includes a plurality of memory cells. Each of the plurality of second memory cell units includes a plurality of memory cells. The sense amplifier circuit is connected to the plurality of first interconnects and the plurality of second interconnects. The switching circuit is configured to switch
25 between a connection of the sense amplifier circuit with the plurality of first interconnects and a connection of the sense amplifier circuit with the plurality of second interconnects. Each of the plurality of first interconnects is extended in a first direction and connected to one end of each of the first memory
30 cell units. Each of the plurality of second interconnects is extended in the first direction in each space between the first interconnects and connected to one end of each of the second memory cell units. A first voltage charging the first interconnect with the sense amplifier circuit varies with a
35 position of the first memory cell unit when read-out of the memory cell is performed. A second voltage charging the

second interconnect with the sense amplifier circuit varies with a position of the second memory cell unit when read-out of the memory cell is performed.

Exemplary embodiments of the invention will now be
5 described with reference to the drawings.

The drawings are schematic or conceptual; and the relationships between the thickness and width of portions, the proportional coefficients of sizes among portions, etc., are not necessarily the same as the actual values thereof. Further, the
10 dimensions and proportional coefficients may be illustrated differently among the drawings, even for identical portions.

In the specification and the drawings of the application, components similar to those described in regard to a drawing thereinabove are marked with like reference numerals, and a
15 detailed description is omitted as appropriate.

First embodiment

FIG. 1 is a schematic view illustrating the configuration of a semiconductor memory device according to a first
20 embodiment.

As illustrated in FIG. 1, the semiconductor memory device 510 according to this embodiment includes first to fourth data transfer lines DL1 to DL4.

In the semiconductor memory device 510, a first region
25 RG1 and a second region RG2 are provided on a major surface of a substrate (not illustrated) on which the semiconductor memory device 510 is provided. The first region RG1 is a region where a first memory cell block 1a described below is provided; and the second region RG2 is a region where a
30 second memory cell block 1b described below is provided.

Each of the first to fourth data transfer lines DL1 to DL4 is connected to one end of a memory cell unit 4 (first to fourth memory cell units MCU1 to MCU4) which includes multiple memory cells.

35 Here, a direction perpendicular to the major surface of the substrate is taken as a Z axis direction (the third direction).

One direction perpendicular to the Z axis direction is taken as an X axis direction (the first direction). A direction perpendicular to the Z axis direction and the X axis direction is taken as a Y axis direction (the second direction).

5 The first region RG1 and the second region RG2 are adjacent in the X axis direction.

Each of the first to fourth data transfer lines DL1 to DL4 is extended in the X axis direction.

10 The first and second data transfer lines DL1 and DL2 are provided in the first region RG1; and the third and fourth data transfer lines DL3 and DL4 are provided in the second region RG2.

15 The first data transfer line DL1 and the third data transfer line DL3 are adjacent in the X axis direction; and the third data transfer line DL3 is provided on a line extending from the first data transfer line DL1 in the X axis direction. The second data transfer line DL2 and the fourth data transfer line DL4 are adjacent in the X axis direction; and the fourth data transfer line DL4 is provided on a line extending from the second data transfer line DL2 in the X axis direction. In other words, in the X-Y plane, the fourth data transfer line DL4 is positioned in a diagonal direction from the first data transfer line DL1.

20 The first to fourth data transfer lines DL1 to DL4 are formed by, for example, sidewall patterning. Sidewall patterning is described below. The widths and thicknesses of the first to fourth data transfer lines DL1 to DL4 have mutually different values due to fluctuations of the sidewall patterning.

30 Herein, width is taken to be the length along the Y axis direction. For example, while the semiconductor memory device 510 is provided on the major surface of the substrate, the widths of the first to fourth data transfer lines DL1 to DL4 may be taken as, for example, the widths of the first to fourth data transfer lines DL1 to DL4 on the upper face (the face opposite to the substrate). Thickness is the length along the Z axis direction.

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The width of the second data transfer line DL2 along the Y axis direction is narrower than the width of the first data transfer line DL1 along the Y axis direction. The thickness of the second data transfer line DL2 along the Z axis direction is thinner than the thickness of the first data transfer line DL1 along the Z axis direction.

Here, at least one selected from the width and the thickness of the first data transfer line DL1 may be greater than that of the second data transfer line DL2. Also, at least one selected from the width and the thickness of the third data transfer line DL3 may be greater than that of the fourth data transfer line DL4.

The width and the thickness of the third data transfer line DL3 may be substantially the same as those of the first data transfer line DL1; and the width and the thickness of the fourth data transfer line DL4 may be substantially the same as those of the second data transfer line DL2.

For example, the depth of the first data transfer line DL1 is deeper than the depth of the second data transfer line DL2. Also, the depth of the third data transfer line DL3 is deeper than the depth of the fourth data transfer line DL4. Herein, depth is the length along the Z axis direction from the upper face to the lower face of the data transfer line.

The electrical resistance of the second data transfer line DL2 is higher than that of the first data transfer line DL1; and the electrical resistance of the fourth data transfer line DL4 is higher than that of the third data transfer line DL3. Herein, the electrical resistances of the first to fourth data transfer lines DL1 to DL4 are the resistances along the X axis direction, i.e., the so-called interconnect resistance.

In other words, in the semiconductor memory device 510 as illustrated in FIG. 1, a low resistance interconnect L1, which has a low interconnect resistance, is arranged alternately in the Y axis direction with a high resistance interconnect L2, which has an interconnect resistance higher than that of the low resistance interconnect L1.

Thus, the semiconductor memory device 510 includes: multiple first interconnects LL1 (the low resistance interconnects L1 of the first region RG1) provided in the first region RG1; second interconnects LL2 (the high resistance interconnects L2 of the first region RG1) provided in the first region RG1 in each space between the first interconnects LL1, where the second interconnect LL2 has an electrical resistance higher than that of the first interconnect LL1; multiple third interconnects LL3 (the low resistance interconnects L1 of the second region RG2) provided in the second region RG2 adjacent to the first region RG1 in the X axis direction to extend in the X axis direction on lines extending from the first interconnects LL1; and fourth interconnects LL4 (the high resistance interconnects L2 of the second region RG2) provided in the second region RG2 to extend in the X axis direction on lines extending from the second interconnects LL2, where the fourth interconnect LL4 has an electrical resistance higher than that of the third interconnect LL3. Each of the first to fourth interconnects LL1 to LL4 is connected to one end of each of the multiple memory cell units 4 respectively, where each of the multiple memory cell units 4 includes multiple memory cells. The multiple first interconnects LL1 and the multiple second interconnects LL2 are arranged alternately in the Y axis direction. The multiple third interconnects LL3 and the multiple fourth interconnects LL4 are arranged alternately in the Y axis direction.

At least one selected from the width along the Y axis direction and the thickness along the Z axis direction of the second interconnect LL2 is smaller than that of the first interconnect LL1. At least one selected from the width along the Y axis direction and the thickness along the Z axis direction of the fourth interconnect LL4 is smaller than that of the third interconnect LL3.

One of the fourth interconnects LL4 is electrically connected to one of the first interconnects LL1 between the first region RG1 and the second region RG2; and one of the third

interconnects LL3 is electrically connected to one of the second interconnects LL2 between the first region RG1 and the second region RG2.

In other words, the semiconductor memory device 510 according to this embodiment includes the first memory cell block 1a, the second memory cell block 1b adjacent to the first memory cell block 1a in the X axis direction, and a data transfer line rerouting unit 100 (the interconnect rerouting unit) provided between the first memory cell block 1a and the second memory cell block 1b.

The first memory cell block 1a includes multiple first cell units U1, multiple second cell units U2, the multiple first interconnects LL1, and the multiple second interconnects LL2. Each of the multiple first cell units U1 includes multiple memory cells; and each of the multiple second cell units U2 includes multiple memory cells.

Each of the multiple first interconnects LL1 is connected to one end of each of the first cell units U1, respectively.

Each of the multiple second interconnects LL2 is extended in each space between the first interconnects LL1 to connect to one end of each of the second cell units U2, respectively. The second interconnect LL2 has an electrical resistance higher than that of the first interconnect LL1.

The second memory cell block 1b includes multiple third cell units U3, multiple fourth cell units U4, the multiple third interconnects LL3, and the multiple fourth interconnects LL4. Each of the multiple third cell units U3 includes multiple memory cells; and each of the multiple fourth cell units U4 includes multiple memory cells.

Each of the multiple third interconnects LL3 is extended in the X axis direction on a line extending from the first interconnect LL1 in the X axis direction to connect to one end of each of the third cell units U3, respectively.

Each of the multiple fourth interconnects LL4 is extended in the X axis direction on a line extending from the second interconnect LL2 in the X axis direction to connect to one end of

each of the fourth cell units U4, respectively. The fourth interconnect LL4 has an electrical resistance higher than that of the third interconnect LL3.

5 The data transfer line rerouting unit 100 electrically connects the one of the fourth interconnects LL4 to the one of the first interconnects LL1 and electrically connects the one of the third interconnects LL3 to the one of the second interconnects LL2.

10 The multiple memory cells MC recited above are arranged along the X axis direction. Each of the multiple first to fourth cell units U1 to U4 recited above is extended in the X axis direction. The multiple first and second cell units U1 and U2 recited above are arranged alternately along the Y axis direction. The multiple third and fourth cell units U3 and U4 recited above
15 are arranged alternately along the Y axis direction.

One of the first cell units U1 is the memory cell unit MCU1 connected to the first data transfer line DL1. One of the second cell units U2 is the second memory cell unit MCU2 connected to the second data transfer line DL2. One of the
20 third cell units U3 is the third memory cell unit MCU3 connected to the third data transfer line DL3. One of the fourth cell units U4 is the fourth memory cell unit MCU4 connected to the fourth data transfer line DL4. One of the third cell units U3 is a fifth memory cell unit MCU5 connected to a fifth data transfer line
25 DL5 described below. One of the second cell units U2 is a sixth memory cell unit MCU6 connected to a sixth data transfer line DL6 described below.

For example, for one of the sets of the low resistance interconnect L1 and the high resistance interconnect L2
30 adjacent thereto in the first region RG1, the low resistance interconnect L1 may be taken to be the first data transfer line DL1; and the high resistance interconnect L2 may be taken to be the second data transfer line DL2. For one of the sets of the low resistance interconnect L1 and the high resistance
35 interconnect L2 adjacent thereto in the second region RG2, the low resistance interconnect L1 adjacent to the first data transfer

line DL1 in the X axis direction may be taken to be the third data transfer line DL3; and the high resistance interconnect L2 adjacent to the second data transfer line DL2 in the X axis direction may be taken to be the fourth data transfer line DL4.

5 The data transfer line rerouting unit 100 (the interconnect rerouting unit) between the first region RG1 and the second region RG2 electrically connects, for example, the first data transfer line DL1 to the fourth data transfer line DL4.

10 In other words, the second data transfer line DL2, which is one of the second interconnects LL2, is adjacent to the first data transfer line DL1, which is one of the first interconnects LL1, in the Y axis direction; the third data transfer line DL3, which is one of the third interconnects LL3, is disposed on a line extending from the first data transfer line DL1 in the X axis direction; the fourth data transfer line DL4, which is one of the fourth interconnects LL4, is disposed on a line extending from the second data transfer line DL2 in the X axis direction; and the fourth data transfer line DL4 is electrically connected to the first data transfer line DL1 between the first region RG1 and the second region RG2.

20 In other words, the first data transfer line DL1 is electrically connected to the fourth data transfer line DL4 disposed in the diagonal direction as viewed from the first data transfer line DL1.

25 In this specific example, each of the data transfer lines of the first region RG1 is connected to the data transfer line shifted one line in the Y axis direction in the second region RG2.

30 Here, the fifth data transfer line DL5 is taken to be the low resistance interconnect L1 adjacent to the fourth data transfer line DL4 on the side of the fourth data transfer line DL4 opposite to the third data transfer line DL3 in the Y axis direction. The sixth data transfer line DL6 is taken to be the high resistance interconnect L2 adjacent to the first data transfer line DL1 on the side of the first data transfer line DL1 opposite to the second data transfer line DL2 in the Y axis direction.

The data line rerouting unit 100 electrically connects the second data transfer line DL2 to the fifth data transfer line DL5 (connected to the one end of the fifth memory cell unit MCU5) of the second region RG2.

- 5 The data line rerouting unit 100 electrically connects the third data transfer line DL3 to the sixth data transfer line DL6 (connected to the one end of the sixth memory cell unit MCU6) of the first region RG1.

10 In other words, the fifth data transfer line DL5, which is one other of the third interconnects LL3, is adjacent to the fourth data transfer line DL4 on the side of the fourth data transfer line DL4 opposite to the third data transfer line DL3 in the Y axis direction. The sixth data transfer line DL6, which is one other of the second interconnects LL2, is adjacent to the
15 first data transfer line DL1 on the side of the first data transfer line DL1 opposite to the second data transfer line DL2 in the Y axis direction. The third data transfer line DL3 is electrically connected to the sixth data transfer line DL6 between the first region RG1 and the second region RG2 while the second data
20 transfer line DL2 is electrically connected to the fifth data transfer line DL5 between the first region RG1 and the second region RG2.

 Thus, the semiconductor memory device 510 includes:
25 the first data transfer line DL1 provided in the first region RG1 to connect to one end of the first memory cell unit MCU1 including multiple memory cells; the second data transfer line DL2 provided in the first region RG1 adjacent to the first data transfer line DL1 in the Y axis direction to connect to one end of the second memory cell unit MCU2 including multiple memory
30 cells, where the second data transfer line DL2 has an electrical resistance higher than that of the first data transfer line DL1; the third data transfer line DL3 provided in the second region RG2 to extend in the X axis direction on a line extending from the first data transfer line DL1 in the X axis direction and
35 connect to one end of the third memory cell unit MCU3 including multiple memory cells; and the fourth data transfer line DL4

provided in the second region RG2 to extend in the X axis direction on a line extending from the second data transfer line DL2 in the X axis direction and connect to one end of the fourth memory cell unit MCU4 including multiple memory cells, where
5 the fourth data transfer line DL4 has an electrical resistance higher than that of the third data transfer line DL3, and the fourth data transfer line DL4 is electrically connected to the first data transfer line DL1 between the first region RG1 and the second region RG2.

10 By such a configuration, the continuous interconnect of the first data transfer line DL1 and the fourth data transfer line DL4 forms a combination of the low resistance interconnect L1 and the high resistance interconnect L2. Similarly, the continuous interconnect of the second data transfer line DL2
15 and the fifth data transfer line DL5 forms a combination of the low resistance interconnect L1 and the high resistance interconnect L2. Similarly, the continuous interconnect of the third data transfer line DL3 and the sixth data transfer line DL6 forms a combination of the low resistance interconnect L1 and
20 the high resistance interconnect L2.

Thus, in the semiconductor memory device 510 according to this embodiment, uniform interconnect resistance is provided by connecting the data transfer lines in combinations of the low resistance interconnect L1 and the high resistance interconnect
25 L2; and data transfer lines having high interconnect resistances are eliminated. Thereby, the fluctuation of the electrical resistance of the interconnects can be compensated; the interconnect delay can be suppressed; and the operating speed and the reliability can be improved.

30 On the other hand, in a semiconductor memory device of a comparative example which does not include the data transfer line rerouting unit 100, the low resistance interconnect L1 is extended continuously between the first region RG1 and the second region RG2; and the high resistance interconnect L2 also
35 is extended continuously between the first region RG1 and the second region RG2. In other words, such a configuration

corresponds to a configuration in which, for example, the first data transfer line DL1 and the third data transfer line DL3 are connected to each other and the second data transfer line DL2 and the fourth data transfer line DL4 are connected to each other. Therefore, for example, the interconnect delay of the data transfer line of the combination of the second data transfer line DL2 and the fourth data transfer line DL4, which are the high resistance interconnects L2, increases; the operating characteristics deteriorate; and the reliability deteriorates.

Conversely, in the semiconductor memory device 510 according to this embodiment, a configuration is employed in which the data line rerouting unit 100 electrically connects the low resistance interconnect L1 and the high resistance interconnect L2 to each other. Thereby, the interconnect delay can be suppressed; and the operating speed and the reliability can be improved.

The configuration recited above in which the data transfer lines are connected to each other is one example; and the invention is not limited thereto. Various modifications are possible. Specific examples of forms of connecting the data transfer lines to each other, that is, configurations of the data line rerouting unit 100, are described below.

A semiconductor memory device of a first example according to this embodiment will now be described.

First example

FIG. 2 is a block diagram illustrating the configuration of the semiconductor memory device of the first example.

The semiconductor memory device 511 according to the first example is a NAND EEPROM.

The first and second memory cell blocks 1a and 1b are provided in the semiconductor memory device 511 as illustrated in FIG. 2. The regions where the first and second memory cell blocks 1a and 1b are provided are the first and second regions RG1 and RG2, respectively. As described below, a plurality of the memory cell units 4 are provided in the first and second

memory cell blocks 1a and 1b; and the memory cell unit 4 includes multiple nonvolatile memory cells connected in series.

The semiconductor memory device 511 further includes a data control line driver 2, a row decoder 3, a control circuit 40, a Vpgm generation circuit 41a, a Vpass generation circuit 41b, a Vread generation circuit 41c, a substrate potential control circuit 42, an input/output buffer 45, sense amplifier circuits 46, an address buffer 47, and a column decoder 48.

The sense amplifier circuits 46 detect data of the data transfer lines provided in the first and second memory cell blocks 1a and 1b and retain the data to be written. The sense amplifier circuit 46 includes a data latch and includes, for example, a flip-flop circuit.

The sense amplifier circuits 46 are connected to the input/output buffer 45, to and from which input/output data is input and output. The data transfer from the sense amplifier circuits 46 to the input/output buffer 45 is controlled by an output of the column decoder 48 which receives an address signal 47a from the address buffer 47. The input/output buffer 45 is connected to the output driver I/O.

The row decoder 3 selects memory cells of the first and second memory cell blocks 1a and 1b. Specifically, the row decoder 3 controls control gate lines described below and selection gate lines described below.

The substrate potential control circuit 42 controls the potential of, for example, a p-type substrate (or a p-type well) in which the first and second memory cell blocks 1a and 1b are formed. It is desirable to be able to increase the voltage of the substrate potential control circuit 42, particularly to an erasing voltage of 10 V or more when erasing.

The Vpgm generation circuit 41a generates a writing voltage Vpgm used when writing data to the selected memory cells of the first and second memory cell blocks 1a and 1b. The writing voltage Vpgm is increased higher than the source voltage.

The Vpass generation circuit 41b generates an

intermediate voltage V_{pass} for writing that is provided to unselected memory cells when writing data.

The V_{read} generation circuit 41c generates an intermediate voltage V_{read} for read-out that is provided to the unselected memory cells when reading data.

The V_{pgm} generation circuit 41a, the V_{pass} generation circuit 41b, and the V_{read} generation circuit 41c are controlled by the control circuit 40 to provide the necessary voltage output to the data control line driver 2 in each of the writing, erasing, and reading states.

The writing voltage V_{pgm} is, for example, a voltage not less than 10 V (volts) and not more than 30 V. The intermediate voltage V_{pass} for writing is, for example, a voltage not less than 3 V and not more than 15 V. The intermediate voltage V_{read} for read-out is, for example, a voltage not less than 1 V and not more than 9 V.

The data control line driver 2 is a switch circuit that applies the voltages recited above to the control gates described below of memory cells for which writing or reading is necessary according to the output of the row decoder 3.

FIG. 3 is a schematic circuit diagram illustrating the configuration of the semiconductor memory device of the first example.

As illustrated in FIG. 3, the first and second memory cell blocks 1a and 1b are provided in the semiconductor memory device 511.

The first and second memory cell blocks 1a and 1b include multiple memory cell units 4. Multiple data control lines 7 are connected to each of the multiple memory cell units 4.

A selection transistor is disposed at each of the end portions of the memory cell unit 4 to select one of the multiple memory cell units 4 and connect the one memory cell unit 4 to a data transfer line BL (data transfer lines BL1 to BL $2n+1$). The gate electrode of each of the selection transistors is connected to a selection gate line 5 and a selection gate line 6,

respectively.

The data transfer lines BL extend in directions mutually orthogonal to the data control lines 7 and are disposed at prescribed spacings in directions mutually orthogonal to the data control lines 7.

The memory cells MC included in the memory cell unit 4 are provided at intersections between the data transfer line BL and the data control lines 7. The writing, retention, erasing, and reading of the data are possible independently for each of the memory cells MC.

The memory cell unit 4 is plurally provided along the direction of the data transfer line BL (the X axis direction) and along the direction of the data control line 7 (the Y axis direction). The first memory cell block 1a includes multiple memory cell units 4 arranged along at least the Y axis direction; and the second memory cell block 1b includes other multiple memory cell units 4 arranged along at least the Y axis direction.

Although two memory cell blocks (the first and second memory cell blocks 1a and 1b) are provided in FIG. 3, the invention is not limited thereto. The number of memory cell blocks may be three or more. Because of the address decoding, it is desirable for the number of the memory cell blocks to be a power-of-two integer.

The data control line driver 2 (the data control line drivers 2a and 2b) that drive the data control lines 7 are provided on the one ends of the data control lines 7 (i.e., data control lines WL, e.g., data control lines WL11 to WL1b and data control lines WL21 to WL2b) connected to the multiple memory cell units 4. The data control lines WL11 to WL1b and the selection gate line 5 are connected to the data control line driver 2a; and the data control lines WL21 to WL2b and the selection gate line 5 are connected to the data control line driver 2b.

For the multiple memory cell units 4 adjacent in the X axis direction as illustrated in FIG. 3, the data control line driver 2 is subdivided into the two data control line drivers 2a and 2b

provided at the ends of the memory cell blocks, respectively, for easier disposition of the data control line driver 2 and to match the skew between the data control lines 7 of one memory cell block (e.g., the first memory cell block 1a).

5 The data control line drivers 2a and 2b are connected to row address selection circuits 3a and 3b, respectively. The memory cells MC connected to the data control lines WL11 to WL1b and the memory cells MC connected to the data control lines WL21 to WL2b may be selected independently by block.

10 Although the data control line driver 2 is divided into the data control line drivers 2a and 2b on the left and right of the drawing in the description recited above, the data control line driver 2 may be provided, for example, on either one of the right or left side.

15 In the first memory cell block 1a, the selection gate line 5 (a block selection line SG11) is provided at one end of each of the memory cell units 4; and the selection gate line 6 (a block selection line SG12) is provided at the other end. In the second memory cell block 1b, the selection gate line 5 (a block selection line SG21) is provided at one end of each of the memory cell units 4; and the selection gate line 6 (a block selection line SG22) is provided at the other end. The selection gate line 5 and the selection gate line 6 are provided parallel to the data control lines 7.

25 Although not illustrated in FIG. 3 for easier viewing of the drawing, the memory cell unit 4 and the data transfer line BL (the data transfer lines BL1 to BL2n) are connected to each other. Specifically, the memory cell units 4 are connected to the data transfer line BL on the side of either the selection gate line 5 or 6.

30 The sense amplifier circuit 46-1, 46-2 is connected to one end of the data transfer line BL. Specifically, the sense amplifier circuits 46-1, 46-2 are disposed collectively on the same side of the one ends of the data transfer lines BL instead of being embedded in and between the memory cell blocks (the first and second memory cell blocks 1a and 1b). In other

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words, the semiconductor memory device 511 includes multiple first sense amplifier circuits 46-1 provided on the side of the second memory cell block 1b opposite to the first memory cell block 1a and multiple second sense amplifier circuits 46-2 provided on the side of the second memory cell block 1b opposite to the first memory cell block 1a, where the one end of each of the multiple third interconnects LL3 is connected to each of the multiple first sense amplifier circuits 46-1, respectively, and the one end of each of the multiple fourth interconnects LL4 is connected to each of the multiple second sense amplifier circuits 46-2, respectively. Thereby, the pattern periodicity of the memory cells MC can be maintained; and interconnects can be concentrated in one side of the memory cell blocks and can be shared and reduced. Thereby, the ratio of the semiconductor memory device 511 occupied by the memory cells MC can be increased.

FIGS. 4A and 4B are schematic views illustrating the configuration of the semiconductor memory device of the first example.

Namely, FIG. 4A is a circuit diagram illustrating the circuit of the memory cell unit 4 of the semiconductor memory device 511. FIG. 4B is a schematic plan view illustrating the configuration of the memory cell unit 4 of the semiconductor memory device 511. In FIG. 4B, only the structures below the data transfer lines BL are illustrated for easier understanding of the structures of the memory cells.

FIGS. 5A and 5B are schematic cross-sectional views illustrating the configuration of the semiconductor memory device of the first example.

Namely, FIG. 5A is a cross-sectional view along line B-B' of FIG. 4B; and FIG. 5B is a cross-sectional view along line A-A' of FIG. 4B.

As illustrated in FIG. 4A, the memory cell unit 4 includes multiple memory cells MC (the memory cells M1 to Mb). Here, b is the number of the memory cells MC (b being an integer not less than 2).

The memory cell MC is a nonvolatile memory cell. The multiple memory cells MC are connected in series; and one end of the multiple memory cells MC is connected to the data transfer line BL via a selection transistor S1. The other end of the multiple memory cells MC is connected to a common source line SL via a selection transistor S2.

The transistors of the multiple memory cells MC are formed on the same well.

Here, the number b of the memory cells MC may be, for example, 16, 32, 64, 128, or 256. It is desirable for the number b of the memory cells MC to be 2^k , 2^{k+2} , or 2^{k+4} , where k is an integer not less than 3. For example, the cases where the number of the memory cells MC is 2^{k+2} or 2^{k+4} correspond to the cases where two or four dummy word lines are provided.

Using the block index n , which is an integer not less than 1, as illustrated in FIG. 3, the control electrodes of the memory cells M1 to Mb are connected to the data control lines WLn1 to WLn b , respectively.

The control electrode of the selection transistor S1 is connected to the block selection line (referred to as the block selection line SGn1 or SSL) to select one of the multiple memory cell units 4 along the data transfer line BL and connect the one of the memory cell units 4 to the data transfer line BL.

The control electrode of the selection transistor S2 is connected to the block selection line (referred to as the block selection line SGn2 or GSL).

In other words, the memory cell unit 4 is a NAND memory cell unit.

It is sufficient for either the selection gate line 5 or 6 to be provided in the memory cell unit 4. It is desirable for the selection gate lines 5 and 6 to be extended in the same direction as the data control lines 7 to increase the density.

An example of the configuration of the memory cell unit 4 will now be described with reference to FIG. 4B, FIG. 5A, and FIG. 5B.

As illustrated in FIG. 4B, FIG. 5A, and FIG. 5B, an n-type silicon region 122 is provided on a p-type silicon substrate 121; and a p-type silicon region 123 is provided on the n-type silicon region 122. The p-type silicon region 123 is divided into multiple regions by an element-separating insulating film 124.

A floating gate 126 is provided on the p-type silicon region 123 via a tunneling gate insulating film 125.

In the p-type silicon region 123, for example, the boron impurity concentration is between 10^{14} cm^{-3} and 10^{19} cm^{-3} .

The tunneling gate insulating film 125 may include, for example, a silicon oxide film, a silicon oxynitride film, or a silicon nitride film, or a stacked film including the same. The thickness of the tunneling gate insulating film 125 may be, for example, 1 nm (nanometer) to 20 nm. The floating gate 126 may include, for example, polysilicon; and the thickness of the floating gate 126 may be, for example, 10 nm to 500 nm.

A control gate 127 is provided on the floating gate 126 via an inter-layer insulating film 150.

The inter-layer insulating film 150 may include a stacked film of a silicon oxide film/silicon nitride film/silicon oxide film, a stacked film of a silicon nitride film/silicon oxide film/silicon nitride film/silicon oxide film/silicon nitride film, a stacked film of a silicon oxide film/ AlO_x film/silicon oxide film, a stacked film of a silicon oxide film/ HfAlO_x film/silicon oxide film, a stacked film of a silicon oxide film/ HfO_x film/silicon oxide film, a silicon oxide film, and the like. The thickness of the inter-layer insulating film 150 may be, for example, 2 nm to 30 nm.

The control gate 127 may include, for example, polysilicon, WSi (tungsten silicide), CoSi (cobalt silicide), NiSi (nickel silicide), a stacked film of tungsten and polysilicon, and the like. The thickness of the control gate 127 may be, for example, 10 nm to 500 nm. The control gate 127 is a gate interconnect corresponding to the data control line 7 and the selection gate lines 5 and 6 illustrated in FIG. 3.

It is desirable to provide the element-separating insulating film 124 up to the position of the floating gate 126 of

each of the elements as illustrated in FIG. 5A to increase the coupling ratio between the floating gate 126 and the control gate 127.

5 As illustrated in FIG. 4B, the control gates 127 are connected to each other between adjacent memory cell units 4 to be continuous in the Y axis direction to the boundaries of the memory cell block (the first memory cell block 1a).

10 A sidewall insulating film 143 is provided on the X axis direction side faces of the gate electrodes (the floating gate 126 and the control gate 127). The sidewall insulating film 143 may include, for example, a silicon nitride film or a silicon oxide film; and the thickness of the sidewall insulating film 143 may be, for example, 5 nm to 200 nm.

15 An n-type diffusion layer 128 forming source/drain electrodes is provided in the p-type silicon region 123 on both sides of the gate electrodes (the floating gate 126 and the control gate 127).

20 The n-type diffusion layer 128, the floating gate 126, and the control gate 127 form a floating gate nonvolatile EEPROM cell transistor.

25 The cell stores digital bit information by storing a charge injected as a tunneling current from the channel into the floating gate 126 via the tunneling gate insulating film 125 to form a nonvolatile semiconductor memory in which information is read by measuring a conductance change of the MOSFET according to the charge amount.

30 The gate length of the floating gate 126 (the width of the floating gate 126 in the X axis direction) may be, for example, not less than 0.01 μm (micrometers) and not more than 0.5 μm . The n-type diffusion layer 128 forming the source/drain regions is doped with, for example, at least one selected from phosphorus, arsenic, and antimony with a surface concentration of 10^{17} cm^{-3} to 10^{21} cm^{-3} . The depth of the n-type diffusion layer 128 is, for example, 10 nm to 500 nm.

35 The n-type diffusion layer 128 is shared by adjacent memory cells MC to realize a NAND connection.

Thus, the memory cell MC (i.e., each of the multiple memory cells MC included in, e.g., the multiple first cell units), includes: a semiconductor layer of the second conductivity type (e.g., the p-type silicon region 123) including the first diffusion region of the first conductivity type and the second diffusion region of the first conductivity type (the n-type diffusion layers 128); a memory film (e.g., the floating gate 126) provided on the semiconductor layer between the first diffusion region and the second diffusion region; and a control gate (the control gate 127) provided on the memory film. The memory film may be taken to be the floating gate 126. However, the memory film may include, for example, a charge storage layer of an insulating film such as a silicon nitride film.

As illustrated in FIG. 4B and FIG. 5B, a gate electrode 127_{SSL} and a gate electrode 127_{GSL} are gate electrodes connected to the selection gate line 6 and the selection gate line 5 (the block selection lines) illustrated in FIG. 3. The gate electrode 127_{SSL} and the gate electrode 127_{GSL} are in the same layer as the control gate 127.

The resistance may be reduced in the portions of the gate electrode 127_{SSL} and the gate electrode 127_{GSL} by omitting the inter-layer insulating film 150 to connect the floating gate 126 to the gate electrode 127_{SSL} and connect the floating gate 126 to the gate electrode 127_{GSL}.

The gate lengths of the gate electrode 127_{SSL} and the gate electrode 127_{GSL} are longer than the gate length of the gate electrode of the memory cell MC and may be set to, for example, not less than 0.02 μm and not more than 1 μm . Thereby, a large ON/OFF ratio between when the block is selected and when the block is unselected can be ensured; and malfunctions for programming and reading can be prevented.

A data transfer line side diffusion layer 128_d, i.e., one of the n-type diffusion layers 128, is connected to a data transfer line 136 (the data transfer line BL) via a contact 139 and a contact 130_d.

The data transfer line 136 may include, for example, Cu,

tungsten, tungsten silicide, aluminum, etc.

The contact 139 is a contact between the data transfer line 136 and an intermediate interconnect layer 133_d; and the contact 130_d is a contact between the intermediate interconnect layer 133_d and the diffusion layer 128_d connected to the data transfer line

Although the intermediate interconnect layer 133_d may be omitted from the connection from the data transfer line 136 to the n-type diffusion layer 128, the number of conductive layers can be prevented from increasing by providing the intermediate interconnect layer 133_d and using the intermediate interconnect layer 133_d as a portion of the data transfer line rerouting unit 100 described below.

A source line side diffusion layer 128_s, i.e., one of the n-type diffusion layers 128, is connected to an intermediate interconnect layer 133 forming the common source line SL via a contact 130_s. The common source line SL may be electrically connected between adjacent memory cell blocks in the X axis direction (e.g., the first and second memory cell blocks 1a and 1b).

The n-type diffusion layer 128 may extend to the boundary between adjacent memory cell blocks along the Y axis direction to be used as a source line (the common source line SL).

The contacts recited above (the contact 139, the contact 130_d, and the contact 130_s) may include, for example, n-type or p-type doped polysilicon, tungsten, tungsten silicide, Cu, Al, TiN, Ti, etc. The contact may be an electrical conductor region in which such materials are filled into a contact hole.

The intermediate interconnect layer 133_d and the intermediate interconnect layer 133 may include, for example, n-type or p-type doped polysilicon, tungsten, tungsten silicide, Cu, Al, TiN, Ti, etc.

The data transfer line 136 may be provided continuously in the X axis direction to be connected between adjacent memory cell blocks (e.g., the first and second memory cell

blocks 1a and 1b).

As illustrated in FIG. 4B, either a source line contact SLC or a data transfer line contact BLC is formed between the memory cell units 4 adjacent in the X axis direction. It is
 5 desirable for the source line contact SLC and the data transfer line contact BLC to be shared between the memory cell units 4 adjacent in the X axis direction to reduce the surface area of the semiconductor memory device 511.

An inter-layer insulating film 168 made of, for example,
 10 SiO_2 , is provided between the common source line SL and the transistors of the memory cells MC and between the data transfer line 136 and the transistors of the memory cells MC.

Although not-illustrated, an interconnect made of, for example, tungsten, tungsten silicide, aluminum, etc., formed in
 15 the same direction as the data control line WL is provided above the data transfer line 136 on an inter-layer insulating film 137 made of, for example, SiO_2 or SiN .

FIG. 6 is a schematic plan view illustrating the configuration of the semiconductor memory device of the first
 20 example.

Namely, FIG. 6 illustrates the configuration of the data transfer line rerouting unit 100 provided in the semiconductor memory device 511 of the first example.

FIG. 7 is a schematic cross-sectional view illustrating the configuration of the semiconductor memory device of the first
 25 example.

Namely, FIG. 7A is a cross-sectional view along line A-A' of FIG. 6; and FIG. 7B is a cross-sectional view along line B-B' of FIG. 6.

As illustrated in FIG. 6, FIG. 7A, and FIG. 7B, a first reroute interconnect 233, a second reroute interconnect 227, a first reroute contact 239, and a second reroute contact 230 are
 30 provided in the data transfer line rerouting unit 100.

The first reroute interconnect 233 may include, for
 35 example, the same material as the intermediate interconnect layers 133 and 133_d described above; and the first reroute

interconnect 233 is an interconnect in the same layer as the intermediate interconnect layers 133 and 133_d. The first reroute interconnect 233 may be formed, for example, by filling a conductive material into a trench with a barrier metal such as TaN, TiN, TaW, Ti, etc., interposed therebetween. The first reroute interconnect 233 may include tungsten, Cu, Al, AlCu, etc., having a film thickness of 30 nm to 300 nm.

The second reroute interconnect 227 may include, for example, the same material as the control gate 127; and the second reroute interconnect 227 is an interconnect in the same layer as the control gate 127. The second reroute interconnect 227 having such a configuration realizes the rerouting of the data transfer lines in the Y axis direction.

The first reroute contact 239 electrically connects the data transfer line 136 to the first reroute interconnect 233. The first reroute contact 239 also may be formed, for example, by filling a conductive material into a trench with a barrier metal such as TaN, TiN, TaW, Ti, etc., interposed therebetween.

The second reroute contact 230 electrically connects the first reroute interconnect 233 to the second reroute interconnect 227.

The data transfer line 136 also may be formed, for example, by filling a conductive material into a trench with a barrier metal such as TaN, TiN, TaW, Ti, etc., interposed therebetween.

For easier understanding of the drawing in FIG. 6, the dispositions in the X-Y plane are illustrated for the data transfer line 136, the first reroute interconnect 233, the second reroute interconnect 227, the first reroute contact 239, and the second reroute contact 230.

Thus, the interconnect rerouting unit (the data transfer line rerouting unit 100) includes the first reroute interconnect layer (e.g., the intermediate interconnect layers 133 and 133_d, the first reroute interconnect 233, etc.). The distance along the third direction (Z axis direction) between the first reroute interconnect layer and the semiconductor layer (e.g., the p-type

silicon region 123) is different from the distance along the third direction between the first interconnect LL1 and the semiconductor layer. One of the multiple fourth interconnects LL4 is electrically connected to one of the multiple first
5 interconnects LL1 via the first reroute interconnect layer.

With the substrate (e.g., the p-type silicon substrate 121) as the reference, the height of the first reroute interconnect layer is lower than that of the data transfer line 136 and higher than that of the control gate 127. In other
10 words, the distance along the third direction between the first reroute interconnect layer and the semiconductor layer (e.g., the p-type silicon region 123) is smaller than the distance along the third direction between the first interconnect LL1 and the semiconductor layer and greater than the distance along the
15 third direction between the control gate 127 and the semiconductor layer.

The interconnect rerouting unit (the data transfer line rerouting unit 100) may include the second reroute interconnect layer (e.g., the second reroute interconnect 227). The second
20 reroute interconnect layer is an interconnect in the same layer as the control gate 127. In other words, the distance along the third direction between the second reroute interconnect layer and the semiconductor layer (e.g., the p-type silicon region 123) is substantially equal to the distance along the third
25 direction between the control gate 127 and the semiconductor layer. One of the multiple third interconnects LL3 is electrically connected to one of the multiple second interconnects LL2 via the second reroute interconnect layer.

The interconnect rerouting unit may further include
30 multiple first reroute interconnect layers. The distance along the third direction between each of the multiple first reroute interconnect layers and the semiconductor layer is smaller than the distance along the third direction between the first interconnect LL1 and the semiconductor layer and greater than
35 the distance along the third direction between the control gate 127 and the semiconductor layer. One of the multiple fourth

interconnects LL4 is electrically connected to one of the multiple first interconnects LL1 via one of the multiple first reroute interconnect layers. On the other hand, one of the multiple third interconnects LL3 is electrically connected to one of the multiple second interconnects LL2 via the second reroute interconnect layer.

Also, the interconnect rerouting unit may further include multiple first reroute contacts 239 and multiple second reroute contacts 230. One of the multiple first reroute contacts 239 electrically connects one of the multiple fourth interconnects LL4 to one of the multiple first reroute interconnect layers (e.g., the first reroute interconnect 233). One other of the multiple first reroute contacts 239 electrically connects one of the multiple first interconnects LL1 to the one of the multiple first reroute interconnect layers recited above (e.g., the first reroute interconnect 233). One of the multiple second reroute contacts 230 electrically connects one other of the multiple first reroute interconnect layers to the second reroute interconnect layer (e.g., the second reroute interconnect 227). One other of the multiple second reroute contacts 230 electrically connects still one other of the multiple first reroute interconnect layers to the second reroute interconnect layer.

Thereby, one of the multiple fourth interconnects LL4 is electrically connected to one of the multiple first interconnects LL1 via one of the first reroute interconnect layers. Also, one of the multiple third interconnects LL3 is electrically connected to one of the multiple second interconnects LL2 via the second reroute interconnect layer and one other of the first reroute interconnect layers.

The data transfer line 136 extends from the first and second memory cell blocks 1a and 1b into the region of the data transfer line rerouting unit 100. The data transfer line 136 includes the low resistance interconnect L1 and the high resistance interconnect L2 alternately adjacent in the Y axis direction. Although a pitch p_y of the data transfer line 136 is the same for the low resistance interconnect L1 and the high

resistance interconnect L2, the widths of the low resistance interconnect L1 and the high resistance interconnect L2 may be different from each other (or, the thicknesses of the low resistance interconnect L1 and the high resistance interconnect L2 may be different from each other). The pitch p_y of the data transfer line 136 is, for example, not less than 20 nm and not more than 100 nm. The width of the data transfer line 136 (the interconnect width) is, for example, not less than 10 nm and not more than 50 nm. For example, the width of the low resistance interconnect L1 and the width of the high resistance interconnect L2 are different from each other; and the width of the low resistance interconnect L1 is, for example, not less than 10 nm and not more than 50 nm.

The first reroute contacts 239 mutually adjacent in the Y axis direction are formed, for example, with the same minimum pitch p_y as the data transfer line 136.

Because three types of interconnect connection patterns are used in the data transfer line rerouting unit 100 in this specific example, FIG. 6 illustrates the data transfer line 136 as the data transfer lines 136a, 136b, and 136c corresponding to the three types of interconnect connection patterns.

As described below, the data transfer line 136 is formed by sidewall patterning. The low resistance interconnect L1 of the data transfer lines 136 extending from the first memory cell block 1a is on the same line of extension in the X axis direction as the low resistance interconnect L1 of the data transfer lines 136 extending from the second memory cell block 1b. Similarly, the high resistance interconnect L2 of the data transfer lines 136 extending from the first memory cell block 1a is on the same line of extension in the X axis direction as the high resistance interconnect L2 of the data transfer lines 136 extending from the second memory cell block 1b.

It is possible to ensure a registration margin of the data transfer line 136 and the first reroute contact 239 equal to or greater than the spacing between the data transfer lines 136 in the memory cell block.

As illustrated in FIG. 6, the widths of the first reroute interconnect 233 and the second reroute interconnect 227 can be relaxed to, for example, at least twice the width of the data transfer line 136. Thereby, lithography having a low resolution of lower cost than that of the data transfer line 136 can be used; and the data transfer line rerouting unit 100 can be formed with lower costs.

As illustrated in FIG. 6, the diameter of the second reroute contact 230 may be, for example, at least 1.2 times that of the first reroute contact 239. In other words, the diameter of the second reroute contact 230 may be at least 1.2 times the diameter of the first reroute contact 239. Thereby, lithography having a low resolution of lower cost than that of the first reroute contact 239 can be used; and the data transfer rerouting unit 100 can be formed with lower costs.

It is unnecessary to bend the data transfer line 136 in the X-Y plane in the data transfer rerouting unit 100; and the data transfer line 136 in the region of the data transfer rerouting unit 100 can be disposed densely in the Y axis direction similarly to the first and second memory cell blocks 1a and 1b.

In the data transfer line rerouting unit 100, the minimum width of the first reroute interconnect 233, the minimum spacing between the first reroute interconnects 233, the minimum width of the second reroute interconnect 227, and the minimum spacing between the second reroute interconnects 227 can be ensured equal to or greater than the width of the data transfer line 136 and the spacing between the data transfer lines 136.

The data transfer line rerouting unit 100 can be formed using the interconnect components included in the first and second memory cell blocks 1a and 1b and can be formed without adding new processes.

In other words, the minimum interconnect pitch necessary in the data transfer line rerouting unit 100 is the pitch p_y of the data transfer line 136. The minimum width of

the contact and the minimum width of the spacing between the contacts are the width of the first reroute contact 239 directly connected to the data transfer line 136. Such values are values of the dimensions necessary in the processes forming the structural components included in the first and second memory cell blocks 1a and 1b; and it is unnecessary to form contacts smaller than those of conventional art or fine interconnects. Accordingly, lithography having a resolution higher than that of conventional art is unnecessary; and the desired rerouting can be realized.

In other words, the first reroute contact 239 can be formed, for example, with the same dimensions as the contacts connecting the data transfer line 136 to the memory cells; and the first reroute contact 239 can be formed without more contact processes or interconnect processes.

The data transfer line rerouting unit 100 of this specific example includes: an interconnect layer in which the data transfer lines 136 are provided to extend; two layers, i.e., the first interconnect layer (the first reroute interconnect 233) and the second interconnect layer (the second reroute interconnect 227), provided in layers different from that of the data transfer lines 136 and having a minimum interconnect width at least twice that of the data transfer line 136; the first contact (the first reroute contact 239) selectively connecting the data transfer line 136 to the first interconnect layer; and the second contact (the second reroute contact 230) connecting the first interconnect layer to the second interconnect layer, where the second contact (the second reroute contact 230) has a diameter at least 1.2 times that of the first contact (the first reroute contact 239).

As illustrated in FIG. 6, the data transfer line 136 extending from the second memory cell block 1b side is electrically connected to the data transfer line 136 positioned one line to the right on the first memory cell block 1a side.

For example, the data transfer line 136a on the second memory cell block 1b side is electrically connected to the data

transfer line 136b on the first memory cell block 1a side via the first reroute contact 239 and the first reroute interconnect 233.

The data transfer line 136b on the second memory cell block 1b side is electrically connected to the data transfer line 136c on the first memory cell block 1a side via the first reroute contact 239, the first reroute interconnect 233, and the second reroute interconnect 227.

The data transfer line 136c on the second memory cell block 1b side is electrically connected to the data transfer line 136a on the first memory cell block 1a side via the first reroute contact 239 and the first reroute interconnect 233.

By such a configuration, the data transfer lines 136 of the first and second memory cell blocks 1a and 1b disposed at mutually diagonal positions in the X-Y plane can be electrically connected to each other.

A configuration also is possible by using, for example, the configuration illustrated in FIG. 3 and FIG. 6 mirrored around the X axis direction.

Although the data transfer lines 136 disposed at mutually diagonal positions in the X-Y plane are electrically connected to each other by shifting one line along the Y axis direction in this specific example, the invention is not limited thereto. In other words, it is sufficient for the low resistance interconnect L1 of the first memory cell block 1a to be electrically connected to the high resistance interconnect L2 of the second memory cell block 1b and for the high resistance interconnect L2 of the first memory cell block 1a to be electrically connected to the low resistance interconnect L1 of the second memory cell block 1b.

For example, the data transfer line 136 of the first memory cell block 1a may be electrically connected to the data transfer line 136 of the second memory cell block 1b by shifting an odd number of lines along the Y axis direction. In the case of a configuration to reroute to an odd number of lines of three or more such as three lines, five lines, etc., it is sufficient, for example, to repeat the rerouting of one line three times, five times, etc. Therefore, the data transfer line rerouting unit 100

can be realized with the same number of layers and the same number of contact layers as the semiconductor memory device 511 by, for example, adjusting the pattern of the first reroute interconnect 233 and the second reroute interconnect 227.

5 Here, the number of the data transfer lines 136 increases according to the number of lines shifted during the rerouting. Therefore, the increase of the number of the data transfer lines 136 can be kept to a minimum by using a reroute configuration that shifts one line as in the semiconductor memory device 511;
10 and an increase of the surface area of the semiconductor memory device can be suppressed.

 The data transfer line rerouting unit 100 can reroute the data transfer lines 136 without an external signal input. Accordingly, it is unnecessary to add a circuit; and the circuit
15 surface area can be reduced. Moreover, the data transfer line rerouting unit 100 has a structure in which the data transfer lines 136 are electrically connected by electrical conductors without using a semiconductor substrate. Therefore, a leakage current does not flow from the interconnects into the
20 semiconductor substrate even when the voltage between the interconnects swings between positive and negative. Thereby, it is possible to transmit the potential of the data transfer line 136 between the first and second memory cell blocks 1a and 1b while keeping the potential changes and the current changes of
25 the data transfer line 136 small.

 In the semiconductor memory device 511, it is likable for the number of the memory cells MC included in the memory cell unit 4 belonging to the first memory cell block 1a to be substantially equal to the number of the memory cells MC
30 included in the memory cell unit 4 belonging to the second memory cell block 1b. It is likable for the length along the X axis direction of the data transfer line 136 belonging to the first memory cell block 1a to be substantially equal to the length along the X axis direction of the data transfer line 136
35 belonging to the second memory cell block 1b. The effects of suppressing the interconnect delay and improving the operating

characteristics and the reliability, in particular, in such a configuration in which the low resistance interconnect L1 and the high resistance interconnect L2 are disposed alternately (e.g., the configuration in which the interconnects are formed
5 by sidewall patterning with twice the density of the lithography).

An example of a formation method of the data transfer line 136 will now be described.

FIG. 8A to FIG. 9C are schematic cross-sectional views in
10 order of the processes, illustrating the method for constructing the data transfer lines of the semiconductor memory device of the first example by double patterning using sidewall members (Sidewall Double Patterning (SDP)).

As illustrated in FIG. 8A, an inter-layer film 402 is formed
15 on a major surface of a base film 401; and an insulating film 403 is formed on the inter-layer film 402. The base film 401 is, for example, a film on the surface of a base member in a layer below that of the data transfer lines 136 to be constructed.

The insulating film 403 may include a silicon oxide film, a
20 silicon oxynitride film, a SiON film, etc. The inter-layer film 402 may include, for example, a silicon nitride film, a SiCN film, a SiON film, etc. The base film 401 may include a material different from that of the inter-layer film 402. The base film 401 may include, for example, a silicon oxide film, a silicon
25 oxynitride film, a SiON film, etc.

After forming a core member film forming a core member
404 on the major surface of the insulating film 403, a resist is formed on the core member film by lithography with a pitch of twice the pitch p_y of the data transfer line 136. The pitch of
30 the resist may be set to, for example, the minimum pitch of the patterning resolution of the lithography. The width of the resist may be set to, for example, an interconnect width in the range of 30 nm to 200 nm. The core member film is patterned using the resist as a mask to form the core member 404. The core
35 member 404 may include a silicon oxide film or a silicon nitride film. Further, the core member 404 may include an amorphous

silicon film or a carbon film.

The core member 404 is formed with a width reduced to half of the assumed pitch of the data transfer line 136. In such a case, it can be taken that the core member 404 is formed slightly larger than half the assumed pitch of the data transfer line 136 due to the fluctuation of the width of the resist. The assumed pitch of the data transfer line 136 is a value, for example, between 10 nm and 100 nm.

As illustrated in FIG. 8B, a sidewall film 405 is formed to cover the upper face and the side faces of the core member 404. The sidewall film 405 includes a material different from that of the core member 404. The sidewall film 405 may include, for example, silicon, Al_2O_3 , etc. As long as the sidewall film 405 is a different film from the core member 404, the sidewall film 405 may include a silicon oxide film or a silicon nitride film; and further, the sidewall film 405 may include an amorphous silicon film or a carbon film. The thickness of the sidewall film 405 along the Y axis direction is set to about half the length of the assumed pitch of the data transfer line 136.

Then, anisotropic etching is performed to expose a portion of the insulating film 403. Thereby, the sidewall film 405 is formed on the sidewalls of the core member 404.

The core member 404 is removed as illustrated in FIG. 8C. The removal of the core member 404 may be performed by etching using, for example, a hydrofluoric acid-based etchant or RIE (Reactive Ion Etching).

As illustrated in FIG. 9A, the insulating film 403 and the inter-layer film 402 are etched using the sidewall film 405 as a mask. Such etching may be anisotropic etching. In such a case, the base film 401 may include a material different from that of the inter-layer film 402 (a material having an etching rate lower than that of the inter-layer film 402) such that the etching stops at the interface between the inter-layer film 402 and the base film 401. This process is a so-called sidewall transfer process.

As illustrated in FIG. 9B, the sidewall film 405 that was

used as a mask is removed; and a barrier metal 406 is formed on the exposed upper face of the base film 401, the side faces of the inter-layer film 402, and the upper face and side faces of the insulating film 403. The barrier metal 406 may include, for example, TaN, TaW, Ti, TiN, etc. The thickness of the barrier metal 406 may be, for example, 1 nm to 10 nm.

A metal film 407 is formed on the barrier metal 406 to fill the trench; and planarizing is performed by, for example, CMP (Chemical Mechanical Polishing). The metal film 407 may include a material having a resistance lower than that of the barrier metal 406. The metal film 407 may include, for example, Cu, Al, and W. The metal film 407 (including the barrier metal 406) filled into the trench forms the data transfer line 136. The data transfer line 136 forms a so-called damascene structure. The cross-sectional configuration of the data transfer line 136 (the cross-sectional configuration when the data transfer line 136 is cut in a plane perpendicular to the first direction) is a reverse-tapered configuration.

The manufacturing method described above in regard to FIG. 8A to FIG. 8C and FIG. 9A to FIG. 9C can realize a double pitch of the pitch constructed by the lithography by using the sidewall film 405. Such double pitch construction technology is referred to as double patterning using sidewall members (Sidewall Double Patterning (SDP)).

As illustrated in FIG. 9A, the width of the trench made in the inter-layer film 402 and the insulating film 403 fluctuates with the fluctuation of the dimensions of the resist and with twice the fluctuation of the film thickness of the sidewall film 405. Therefore, wide trenches and narrow trenches are made to be arranged alternately.

Therefore, as illustrated in FIG. 9C, the wide data transfer lines 136 are arranged alternately with the narrow data transfer lines 136.

Further, as illustrated in FIG. 9C, the wide trenches are deep and the narrow trenches are shallow due to microloading effects. Therefore, the film thickness of the wide data transfer

line 136 is thick; and the film thickness of the narrow data transfer line 136 is thin.

As the data transfer line 136 becomes narrower and shallower, there is a trend for the crystal grain size of the metal thereof to decrease. Thereby, the resistance of the crystal grain boundary of the metal and the boundary resistance between the metal film 407 and the barrier metal 406 increases. Such effects cause greater differences of resistances than those due to differences of the cross-sectional areas of the metal film 407.

Thus, the width and the thickness of the data transfer lines 136 fluctuate due to the fluctuation of the sidewall patterning; and the effects of the fluctuation of the crystal grain size is added such that the difference of the resistance values of the alternately repeating low resistance and high resistance of the data transfer lines 136 is even greater.

As illustrated in FIG. 9C, the fluctuation of the width of the insulating film between the data transfer lines 136 (the difference between a width s_a and a width s_b) is determined by the fluctuation of the thickness (the thickness along the Y axis direction) of the sidewall film 405.

The fluctuation of the width of the data transfer line 136 (the fluctuation of a width s_d) is determined by the sum of the fluctuation of the width (the width along the Y axis direction) of the sidewall film 405 and the fluctuation of the width (the width along the Y axis direction) of the core member 404. Accordingly, the difference of the widths of adjacent data transfer lines 136 (the difference between a width s_c and the width s_d) is greater than the difference of the widths of adjacent insulating films between the data transfer lines 136 (the difference between the width s_a and the width s_b).

In other words, variance of widths of insulating films between the plurality of first interconnects and the plurality of second interconnects is smaller than variance of widths of upper surface height portions of the plurality of first interconnects.

In other words, in the semiconductor memory device 511

as illustrated in FIG. 9C, the high resistance interconnect L2 (the second interconnect) of the first region further includes the sixth data transfer line DL6 adjacent to the first data transfer line DL1 on the side of the first data transfer line DL1 opposite to the second data transfer line DL2 to connect to one end of the sixth memory cell unit MCU6 which includes multiple memory cells, where the sixth data transfer line DL6 has an electrical resistance higher than that of the first data transfer line DL1.

10 The width of the sixth data transfer line DL6 is the almost same as the width of the second data transfer line DL2. The absolute value of the difference between the width (the width w_{sc}) of the first data transfer line DL1 and the width (the width w_{sd}) of the second data transfer line DL2 is greater than the absolute value of the difference between the width (the width w_{sb}) of a first insulating region RGI1 from the first data transfer line DL1 to the second data transfer line DL2 and the width (the width w_{sa}) of a second insulating region RGI2 from the first data transfer line DL1 to the sixth data transfer line DL6.

20 As illustrated in FIG. 9C, the width of the data transfer line 136 can be defined as to be the top face width (the width w_{sc} and the width w_{sd}) of the data transfer line 136 along the Y axis direction. Now, "top face" is defined as the face on the side opposite to the base film 401, i.e., the p-type silicon substrate 121.

25 The thickness of the data transfer line 136 is the thickness along the Z axis direction (a thickness t_c and a thickness t_d) of the data transfer line 136.

30 The feature recited above in which the fluctuation of the width of the insulating film between the data transfer lines 136 is smaller than the fluctuation of the width of the data transfer line 136 at the top face is an advantageous structure for ensuring the breakdown voltage of the insulating film between the data transfer lines 136.

35 In the semiconductor memory device 510 according to this embodiment and the semiconductor memory device 511

according to the first example, the fluctuation of the electrical resistance of the interconnects can be compensated by providing the data transfer line rerouting unit 100, the interconnect delay can be suppressed, and the operating characteristics and the reliability can be improved even in the case where the low resistance interconnect L1 and the high resistance interconnect L2 are formed due to the fluctuation of the sidewall patterning as recited above.

For example, the resistance of the first data transfer line DL1 belonging to the first memory cell block 1a is taken to be a first resistance R_1 ; and the resistance of the second data transfer line DL2 belonging to the first memory cell block 1a is taken to be $R_1(1 + \Delta R)$. Here, ΔR is taken to be a positive value. The capacitances of the regions including the first data transfer line DL1 and the second data transfer line DL2 are taken to be a first capacitance C_1 by replacing the capacitances with a lumped constant.

On the other hand, the resistance of the third data transfer line DL3 belonging to the second memory cell block 1b is taken to be a second resistance R_2 ; and the resistance of the fourth data transfer line DL4 belonging to the second memory cell block 1b can be approximated as $R_2(1 + \Delta R)$. The capacitances of the regions including the third data transfer line DL3 and the fourth data transfer line DL4 are taken to be a second capacitance C_2 by replacing the capacitances with a lumped constant. Because the ratio of the resistances of the data transfer lines 136 adjacent to each other on the line of extension in the X axis direction is the ratio of the first resistance R_1 and the second resistance R_2 , the second capacitance C_2 can be approximated by $C_1 \times (R_2/R_1)$ in the case where the capacitance between the data transfer lines is dominant.

In such a case, the resistances are averaged by providing the data transfer line rerouting unit 100 in the semiconductor memory device 510 according to this embodiment and the semiconductor memory device 511 according to the first

example by electrically connecting the low resistance interconnect L1 and the high resistance interconnect L2 to each other. In other words, the time constant of the interconnect delay from the sense amplifier circuit 46 to the memory cell unit 4 positioned most distally thereto is $\{R1C1 \times (1 + \Delta R) + R2C2\}$ or $\{R1C1 + R2C2 \times (1 + \Delta R)\}$ when the change of the resistance of the data transfer line rerouting unit 100 is sufficiently small.

The difference of the time constants between adjacent data transfer lines BL (the data transfer lines 136) is $(R1C1 - R2C2) \times \Delta R$.

Here, in the case where the lengths of the data transfer lines BL are substantially equal between the first memory cell block 1a and the second memory cell block 1b, the difference of the time constants recited above of $(R1C1 - R2C2) \times \Delta R$ is substantially zero.

FIG. 10 is a schematic circuit diagram illustrating the configuration of a semiconductor memory device of a comparative example.

As illustrated in FIG. 10, the data transfer line rerouting unit 100 is not provided in the semiconductor memory device 519 of the comparative example. In other words, for example, the first data transfer line DL1 and the third data transfer line DL3 of FIG. 1 are connected to each other; and the second data transfer line DL2 and the fourth data transfer line DL4 are connected to each other. In other words, the low resistance interconnects L1 adjacent in the X axis direction are connected to each other; and the high resistance interconnects L2 adjacent in the X axis direction are connected to each other. Otherwise, the semiconductor memory device 519 is the same as the semiconductor memory device 511, and a description is therefore omitted.

In the semiconductor memory device 519 of the comparative example, the time constant of the interconnect delay from the sense amplifier circuit 46 to the memory cell unit 4 positioned most distally thereto for the high resistance interconnect L2 is $(R1C1 + R2C2) \times (1 + \Delta R)$ for the maximum

case and is greater than that of the semiconductor memory device 511 according to the first example.

The difference of the time constants between adjacent data transfer lines BL (the data transfer lines 136) is $(R1C1 + R2C2) \times \Delta R$ which is greater than that of the semiconductor memory device 511 according to the first example and cannot be zero.

Therefore, in the semiconductor memory device 519, the read-out speed decreases; the read-out margin decreases; electromigration and stress induced migration occur easily; and the reliability deteriorates.

In other words, in the data transfer lines BL having high interconnect resistances, the interconnect delay is large when reading the information stored in the memory cells MC; and the read-out speed decreases. Because the interconnect resistance is connected in series with the memory cells MC, the current flowing in the memory cells MC decreases as the interconnect resistance increases. Therefore, it becomes difficult to discriminate between the cut off state and the conducting state of the memory cells MC; and the read-out margin decreases. For example, in a NAND flash memory array, an interconnect having a length of, for example, not less than 2 mm may be used as the data transfer line BL to increase the proportion occupied by the memory cells MC; and the sense amplifier circuit 46 is electrically connected to the end of the data transfer line BL. A delay occurs based on the time constant of the interconnect between the memory cells MC proximal to the sense amplifier circuit 46 and the memory cells MC most distal to the sense amplifier circuit 46; and it is necessary to increase the margin of the read-out time because the memory cells MC are read at the same speed.

Moreover, reliability deterioration such as electromigration and stress induced migration may occur in the data transfer lines BL having narrow widths.

Conversely, in the semiconductor memory device 510 according to this embodiment and the semiconductor memory

device 511 according to the first example, the fluctuation of the electrical resistance of the interconnects is compensated by providing the data transfer line rerouting unit 100; the interconnect delay can be suppressed; and the operating speed
 5 and the reliability can be improved.

Reducing the difference between the number NA of the memory cells MC included in the memory cell unit 4 of the first memory cell block 1a and the number NB of the memory cells MC included in the memory cell unit 4 of the second memory
 10 cell block 1b to not more than 10% can suppress the difference of the time constants between adjacent data transfer lines BL to not more than 10% of the difference of $(R1C1 + R2C2) \times \Delta R$ of the time constants of the semiconductor memory device 519 of the comparative example, which is desirable for circuit
 15 operations.

In other words, by such settings, the circuit variance due to the time constant fluctuation originated from the interconnect structure fluctuation can be suppressed to not more than 10%; and a circuit having small operational
 20 fluctuations can be realized. Relative fluctuations of the width of the data transfer line 136 of about 10% are tolerated to guarantee the dimensional accuracy of the lithography. By suppressing the relative fluctuation of the time constants of the mutually adjacent interconnects recited above to not more than
 25 10%, the fluctuation of the time constant can be smaller than the relative fluctuation of the width of the data transfer line 136; and the entire fluctuation of the time constants can be reduced further.

In other words, the number of the memory cells MC included in the first memory cell unit MCU1 can be set equal to the number of the memory cells MC included in the second memory cell unit MCU2; and the number of the memory cells MC included in the third memory cell unit MCU3 can be set
 30 equal to the number of the memory cell MC included in the fourth memory cell unit MCU4. The absolute value of $(NA - NB)/(NA + NB)$ can be 0.1 or less, where NA is the number of
 35

the memory cells MC included in the first memory cell unit MCU1 and NB is the number of the memory cells MC included in the third memory cell unit MCU3.

5 Thereby, the fluctuation of the time constants can be reduced; and the operating characteristics can be improved even more.

It is more likeable for the absolute value of $(NA - NB)/(NA + NB)$ to be not more than 0.05. Thereby, the operating characteristics can be improved even more.

10 According to the semiconductor memory device 511 of this example, in the cases where the read-out is performed simultaneously and the writing is performed simultaneously on the memory cells MC included in the memory cell blocks connected by adjacent data transfer lines BL, normal operations
15 of the circuit are possible even when the circuit operation margin is reduced by an amount of the difference of the delay times between the data transfer lines BL; and the circuit operation speed can be increased. Thereby, the read-out and the writing can be realized at speeds higher than those of the
20 comparative example.

Further, it is possible to match the operation timing of the sense amplifier circuits 46 connected to adjacent data transfer lines BL; and as an entirety, it is possible to realize circuit operations having matched delay characteristics and
25 matched skew. The fluctuation of the delay time between the data transfer lines BL also can be reduced; and disturbance of the pulse waveform due to the difference of the time constants also can be reduced.

In the case where the lengths (the lengths along the X
30 axis direction) of the data transfer lines BL included in the first memory cell block 1a and the second memory cell block 1b are substantially equal, the interconnect delay can be smaller than that of the comparative example by an amount of $(R1C1) \times \Delta R$ or more; and a charge/discharge time of the interconnects can be
35 reduced further. Thereby, normal operations of the circuit are possible even when the circuit operation margin is reduced; and

the speed of the circuit operations can be increased. Thereby, the read-out and the writing can be realized at speeds higher than those of the comparative example.

In the semiconductor memory device 511 according to this example, the difference of the resistance from the sense amplifier circuit 46 to the memory cell unit 4 most distal to the sense amplifier circuit 46 can be reduced even in the case where, for example, the difference of the current amount flowing in the data transfer line BL affects the threshold voltage determination read-out, and this structure is advantageous because the threshold voltage determination can be performed stably due to reducing the resistance variations of data transfer lines .

That is, in the case of the comparative example in which the interconnect rerouting of the data transfer lines BL is not performed, the interconnect resistance of the low resistance interconnect L1 is $(R1 + R2)$ as described above while the interconnect resistance of the high resistance interconnect L2 is $(R1 + R2) \times (1 + \Delta R)$. Thus, in the comparative example, a difference of the interconnect resistances between the low resistance interconnect L1 and the high resistance interconnect L2 occurs; and a difference of the amount of flowing current occurs.

Conversely, in the semiconductor memory device 511 according to this example, the time constant of the interconnect delay is $\{R1C1 \times (1 + \Delta R) + R2C2\}$ or $\{R1C1 + R2C2 \times (1 + \Delta R)\}$ as described above; and the difference of the time constants between adjacent data transfer lines BL is $(R1C1 - R2C2) \times \Delta R$.

In the case where the lengths of the data transfer lines BL of the first memory cell block 1a and the second memory cell block 1b are substantially equal, the difference of the time constants recited above of $(R1C1 - R2C2) \times \Delta R$ can be substantially zero.

Thereby, in the cases where the read-out is performed simultaneously and the writing is performed simultaneously on the memory cells MC connected to the adjacent data transfer

lines BL, the circuit operation margin can be reduced by an amount of the difference of the interconnect resistances between the data transfer lines BL; and, therefore, the speed of the circuit operations can be increased. Also, the difference of the current due to the difference of the interconnect resistances can be reduced by reducing the difference of the interconnect resistances; and the difference of the threshold voltages can be detected with better precision. Thereby, the read-out and the writing can be realized at high speeds.

Moreover, in the case where the lengths of the data transfer lines BL included in the first and second memory cell blocks 1a and 1b are substantially equal, the interconnect resistance can be smaller than that of the comparative example by an amount of $R1 \times \Delta R$ or more; the interconnect resistance can be reduced further; and the current of the memory cells MC can be increased.

Second example

FIG. 11 is a schematic plan view illustrating the configuration of a semiconductor memory device of a second example.

Namely, FIG. 11 illustrates the configuration of the data transfer line rerouting unit 100 provided in the semiconductor memory device 512 of the second example according to the first embodiment. The configuration of the semiconductor memory device 512 other than the data transfer line rerouting unit 100 is similar to that of the semiconductor memory device 511 of the first example, and a description is therefore omitted.

In a region RGa of the data transfer line rerouting unit 100 of the semiconductor memory device 512 as illustrated in FIG. 11, one contact set is formed of two first reroute contacts 239 and one contact lithography supplemental pattern 339 (not actually made through to contact). In one contact set, the two first reroute contacts 239 and the one contact lithography supplemental pattern 339 (not actually made through to contact) are disposed diagonally in the X-Y plane. Such a

contact set is multiply disposed repeatedly along the Y axis direction. In other words, the two first reroute contacts 239 and the one contact lithography supplemental pattern 339 (not actually made through to contact) are repeatedly disposed in a staggered configuration (a zigzag configuration) along the Y axis direction.

The contact lithography supplemental pattern 339 (not actually made through to contact) is disposed to increase the regularity of the contacts in the X-Y plane. The contact lithography supplemental pattern 339 (not actually made through to contact) is formed, for example, smaller than the size of the first reroute contact 239 by an amount in the range of 3 nm to 30 nm. As a result, a portion of the contact lithography supplemental pattern 339 (not actually made through to contact) is not actually made into a contact hole and does not perform an electrical connection between the conductive layers.

As illustrated in FIG. 11, the first data transfer line DL1 is electrically connected to the fourth data transfer line DL4 via the first reroute contact 239 and the first reroute interconnect 233.

For example, the second data transfer line DL2 is electrically connected to the fifth data transfer line DL5 via the first reroute contact 239 and the first reroute interconnect 233. For example, the third data transfer line DL3 is electrically connected to the sixth data transfer line DL6 via the first reroute contact 239, the first reroute interconnect 233, and the second reroute interconnect 227.

Thereby, in the semiconductor memory device 512 as well, the fluctuation of the electrical resistance of the interconnects can be compensated; the interconnect delay can be suppressed; and the operating speed and the reliability can be improved.

The contacts of the data transfer lines BL in the memory cell blocks also may include the periodically disposed three contacts, i.e., the two first reroute contacts 239 and the one

contact lithography supplemental pattern 339 (not actually made through to contact). Thereby, the data transfer line rerouting unit 100 can be formed with the same lithography conditions as the memory cell blocks; and the process margin
5 can be increased even more.

Third example

FIG. 12 is a schematic plan view illustrating the configuration of a semiconductor memory device of a third
10 example.

Namely, FIG. 12 illustrates the configuration of the data transfer line rerouting unit 100 provided in the semiconductor memory device 513 of the third example according to the first embodiment. The configuration of the semiconductor memory
15 device 513 other than the data transfer line rerouting unit 100 is similar to that of the semiconductor memory device 511 of the first example, and a description is therefore omitted.

In the semiconductor memory device 513 as illustrated in FIG. 12, the dividing position of the data transfer lines 136 (the position of the end portions of the data transfer lines 136 in the X axis direction) is extended between the low resistance
20 interconnect L1 and the high resistance interconnect L2.

As illustrated in FIG. 12, for example, the first data transfer line DL1 is electrically connected to the fourth data transfer line DL4 via the first reroute contact 239, the first reroute interconnect 233, and the second reroute interconnect
25 227.

The second data transfer line DL2 is electrically connected to the fifth data transfer line DL5 via the first reroute contact 239 and the first reroute interconnect 233. The third data transfer line DL3 is electrically connected to the sixth data transfer line DL6 via the first reroute contact 239 and the first reroute interconnect 233.
30

Thereby, in the semiconductor memory device 513 as well, the fluctuation of the electrical resistance of the interconnects can be compensated; the interconnect delay can
35

be suppressed; and the operating speed and the reliability can be improved.

Thus, according to the semiconductor memory device 510 (and the semiconductor memory devices 511 to 513 according to the first to third examples) according to this embodiment, the problems of the interconnect delay increasing and the read-out speed decreasing during the read-out of the memory cells MC can be mitigated.

In a structure in which the sense amplifier circuit 46 and the data transfer line BL (the data transfer line 136) are connected in series to the memory cell unit 4, the current flowing in the memory cells MC decreases as the interconnect resistance increases. Therefore, the difference between the cell current in the cut off state and the cell current in the conducting state decreases; it becomes difficult to discriminate between the states of the memory cells MC; and the read-out margin decreases. However, according to this embodiment, the minimum current flowing in the memory cells MC can be greater than that of the comparative example; and the read-out margin can be increased even more.

Particularly in a NAND flash memory, an interconnect having a length of, for example, not less than 2 mm may be used as the data transfer line BL to increase the proportion occupied by the memory cells MC; and the sense amplifier circuit 46 is electrically connected to the end of the data transfer line BL. In such a configuration, a delay due to the time constant of the data transfer line BL occurs between the memory cells MC connected to the data transfer line BL proximally to the sense amplifier circuit 46 and the memory cells MC connected at positions distal to the sense amplifier circuit 46. In the case where such memory cells MC are read at equivalent speeds, a read-out timing with an ample margin is set to be able to read the memory cells MC distal to the sense amplifier circuit 46. However, by applying this embodiment, the fluctuation of the time constants between the data transfer lines 136 can be reduced. Thereby, the read-out time margin

of the memory cells MC can be greater than that of conventional art.

The amount of the voltage drop occurring in the data transfer line BL is proportional to the interconnect resistance. Accordingly, in the case where the width of the metal interconnect forming the data transfer line BL is uniformly narrow, problems of increased metal interconnect resistance and increased interconnect delays, electromigration, and stress induced migration easily occur. Conversely, by applying this embodiment, the problem of the current flowing in the memory cells MC decreasing as the interconnect resistance increases can be mitigated. Therefore, the read-out margin can be greater than that of conventional art. Further, the problems of increased metal interconnect resistance and increased interconnect delays, electromigration, and stress induced migration do not occur as easily as in the case where the width of the metal interconnect is uniformly narrow.

The semiconductor memory device 510 (and the semiconductor memory devices 511 to 513 according to the first to third examples) according to this embodiment have the following feature A.

Namely, the relative positions (e.g., the positions along the Y axis direction) can be mutually the same for the data transfer lines BL of the first memory cell block 1a and the data transfer lines BL of the second memory cell block 1b; and modifications to conventional art are unnecessary.

Therefore, it is sufficient only to shift the physical/logical address allocation between the memory cells MC by an odd number of bits. In other words, it is unnecessary to modify the voltage applied to the data transfer lines BL between the first and second memory cell blocks 1a and 1b; and a configuration similar to that of conventional art can be applied as-is.

Further, the relative relationship between the data transfer lines BL of the first memory cell block 1a and the data transfer lines BL of the second memory cell block 1b is the same relative relationship as that between the memory cells MC

of the first memory cell block 1a and the memory cells MC of the second memory cell block 1b. Because the relative relationship of adjacent data transfer lines BL is the same as the relative relationship of adjacent cells, it is unnecessary to
5 change the parameters against the interference and the disturbance between the memory cells MC of the first memory cell block 1a and the second memory cell block 1b; the various design parameters can be handled equally with or without the rerouting; and the advantage of high design efficiency is
10 provided.

Second embodiment

FIG. 13 is a schematic view illustrating the configuration of a semiconductor memory device according to a second
15 embodiment.

As illustrated in FIG. 13, the low resistance interconnect L1 (the first interconnect LL1 and the third interconnect LL3) and the high resistance interconnect L2 (the second interconnect LL2 and the fourth interconnect LL4) are provided
20 also in the semiconductor memory device 520 according to this embodiment. In other words, the semiconductor memory device 520 also includes the first to fourth data transfer lines DL1 to DL4. The configuration of the rerouting of the first to fourth data transfer lines DL1 to DL4 in the semiconductor
25 memory device 520 differs from that of the semiconductor memory device 510. Otherwise, the semiconductor memory device 520 is similar to the semiconductor memory device 510, and a description is therefore omitted.

In the semiconductor memory device 520, the third data
30 transfer line DL3 is electrically connected to the second data transfer line DL2 between the first region RG1 (the first memory cell block 1a) and the second region RG2 (the second memory cell block 1b) while the fourth data transfer line DL4 is electrically connected to the first data transfer line DL1.

35 In such a configuration as well, the interconnect resistance can be uniform by connecting the low resistance

interconnect L1 of the first region RG1 to the high resistance interconnect L2 of the second region RG2 and by connecting the high resistance interconnect L2 of the first region RG1 to the low resistance interconnect L1 of the second region RG2.

5 Thereby, effects similar to those described in regard to the first embodiment can be obtained. Namely, the fluctuation of the electrical resistance of the interconnects can be compensated; the interconnect delay can be suppressed; and the operating speed and the reliability can be improved.

10 The semiconductor memory device 520 according to the second embodiment exhibits effects similar to those of the first embodiment excluding the "feature A" described in regard to the first embodiment. Moreover, compared to the first embodiment, the rerouting of the data transfer lines BL in the
15 semiconductor memory device 520 according to this embodiment can be performed without adding the odd number of the data transfer lines BL (the odd number of lines $\times$ the number of memory cell blocks). Thereby, the circuit area can be reduced.

20

Fourth example

FIG. 14 is a schematic circuit diagram illustrating the configuration of a semiconductor memory device of a fourth example.

25 As illustrated in FIG. 14, the configuration of the data transfer line rerouting unit 100 of the semiconductor memory device 524 according to the fourth example of the second embodiment differs from that of the semiconductor memory device 511 according to the first example. Otherwise, the
30 semiconductor memory device 524 is similar to the semiconductor memory device 511.

Namely, in the semiconductor memory device 524, the data transfer lines BL are rerouted by crossing two from each of the first and second memory cell blocks 1a and 1b.

35 FIG. 15 is a schematic plan view illustrating the configuration of the semiconductor memory device of the fourth

example.

Namely, FIG. 15 illustrates the configuration of the data transfer line rerouting unit 100 provided in the semiconductor memory device 524 of the fourth example.

5 In the semiconductor memory device 524 as illustrated in FIG. 15, for example, the first data transfer line DL1 is electrically connected to the fourth data transfer line DL4 via the first reroute contact 239 and the first reroute interconnect 233.

10 The second data transfer line DL2 is electrically connected to the third data transfer line DL3 via the first reroute contact 239, the first reroute interconnect 233, and the second reroute interconnect 227.

15 Thereby, in the semiconductor memory device 524 as well, the fluctuation of the electrical resistance of the interconnects can be compensated; the interconnect delay can be suppressed; and the operating speed and the reliability can be improved.

20 The formation methods of the element-separating insulating film 124, the inter-layer insulating film 150, and the inter-layer insulating film 168 of any of the semiconductor memory devices according to the first and second embodiments recited above may include, for example, methods that implant oxygen ions into a deposited silicon film and methods that oxidize a deposit silicon film as well as, for example, methods that convert silicon into a silicon oxide film or a silicon nitride film.

30 Although a conductive film made of polycrystalline silicon is used as the floating gate 126 in the specific example recited above, an insulative charge storage layer may be used as the floating gate 126. The charge storage layer may include, for example, a single-layer film of one selected from the group consisting of SiN, SiON, TiO₂, Al₂O₃, tantalum oxide film, strontium titanate, barium titanate, and lead zirconium titanate
35 or a stacked film including at least two selected from the group.

Although the p-type silicon substrate 121 is used as the

semiconductor substrate in which the semiconductor memory device is formed in the specific examples recited above, the semiconductor substrate may include a p-type SOI substrate including an SOI (Silicon On Insulator) and a substrate including
5 a p-type monocrystalline semiconductor layer including silicon such as a SiGe mixed crystal, a SiGeC mixed crystal, etc.

Although a configuration is described in the specific examples recited above in which an n-type FET is formed on the p-type silicon region 123, a configuration may be used in which
10 a p-type FET is formed on an n-type silicon region. In such a case, it is sufficient for "n-type" recited above to be replaced with "p-type," "p-type" recited above to be replaced with "n-type," and the doping impurity types of As, P, and Sb to be replaced with In or B.

15 The floating gate 126 and the control gate 127 may include a Si semiconductor, a SiGe mixed crystal, or a SiGeC mixed crystal, a polycrystal of the same, or a stacked film of the same. The floating gate 126 and the control gate 127 may include amorphous Si, an amorphous SiGe mixed crystal, or an
20 amorphous SiGeC mixed crystal, or a stacked film of the same.

A metal lining layer may be provided on the control gate 127 by depositing. Or, for example, a silicide layer may be formed and used as the metal lining layer by causing the control gate 127 to react with at least one selected from the group
25 consisting of Ti, Co, Ni, Mo, Pd, and Pt.

The memory cell MC recited above may include a semiconductor memory cell transistor having the two values of "0" and "1;" or, a semiconductor memory cell transistor storing multiple bits of three values or more may be used. Greater
30 effects can be obtained by applying this embodiment in the case where a multi-level semiconductor memory cell transistor is used because the spacings between the multiple threshold voltage distributions are narrow and the increase of the threshold voltage distributions due to capacitive coupling
35 between adjacent memory cells; and problems easily occur such as program-disturbance. It is desirable for the number of

threshold voltage distributions stored in one memory cell MC to be a power-of-two integer to simplify the decoding of the information data.

Although the sense amplifier circuit 46 is provided on the second memory cell block 1b side in the specific examples recited above, the sense amplifier circuits 46 may be provided on the first memory cell block 1a side and the second memory cell block 1b side with the functions thereof dispersed therebetween.

10

Third embodiment

FIG. 16 is a block diagram illustrating the configuration of a semiconductor memory device according to a third embodiment

15 A NAND EEPROM is used again as an example to describe a semiconductor memory device 530 according to the third embodiment.

A memory cell array 1 is provided in the semiconductor memory device 530 as illustrated in FIG. 16. The first and second memory cell blocks 1a and 1b are provided in the memory cell array 1. The regions where the first and second memory cell blocks 1a and 1b are provided are the first and second regions RG1 and RG2, respectively. As described below, the plural memory cell units 4 are provided in the first and second memory cell blocks 1a and 1b; and the memory cell unit 4 includes multiple nonvolatile memory cells connected in series.

The semiconductor memory device 530 further includes the data control line driver 2, the row decoder 3, the control circuit 40, the Vpgm generation circuit 41a, the Vpass generation circuit 41b, the Vread generation circuit 41c, the substrate potential control circuit 42, the input/output buffer 45, a sense amplifier circuit 461 (a first sense amplifier circuit), a sense amplifier circuit 462 (a second sense amplifier circuit), the address buffer 47, a first column decoder 481, a second column decoder 482, and a data switching circuit 447.

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The sense amplifier circuit 461 and the sense amplifier circuit 462 detect data from a data transfer line provided in the memory cell array 1 or retain write data. The sense amplifier circuit 461 and the sense amplifier circuit 462 function also as a data latch and include, for example, a flip-flop circuit. The sense amplifier circuit 461 and the sense amplifier circuit 462 are provided to face each other across the memory cell array 1.

In this embodiment, the sense amplifier circuit 461 is connected to the control circuit 40, and the sense amplifier circuit 462 is connected to the control circuit 40. The control circuit 40 controls the order of the outputs from the sense amplifier circuit 461 and the sense amplifier circuit 462.

Further, the sense amplifier circuit 461 is connected to the data switching circuit 447, and the sense amplifier circuit 462 is connected to the data switching circuit 447. The data switching circuit 447 is connected to the input/output buffer 45, to and from which input/output data is input and output.

The data switching circuit 447 switches the input/output between the sense amplifier circuit 461 and the sense amplifier circuit 462. The data switching circuit 447 includes a switching control circuit, in which address data are input.

The column decoder 481 for designating the address of the sense amplifier circuit 461 and the column decoder 482 for designating the address of the sense amplifier circuit 462 are provided. These select a column of which the address is designated by the column decoder, and form a circuit necessary for performing the read-out and writing of data.

Therefore, the data transfer from the sense amplifier circuit 461 to the input/output buffer 45 can be controlled by the output of the column decoder 481 that receives the address signal 47a from the address buffer 47. The data transfer from the sense amplifier circuit 462 to the input/output buffer 45 can be controlled by the output of the column decoder 482 that receives the address signal 47a from the address buffer 47.

The input/output buffer 45 is connected to the output driver I/O and the address buffer 47. The address buffer 47 is

connected to the column decoder 481, and the address buffer 47 is connected to the column decoder 482.

The row decoder 3 selects memory cells in the memory cell array 1. Specifically, the row decoder 3 controls the control gate line 7 and the selection gate lines 5 and 6.

FIG. 17 is a schematic circuit diagram illustrating the configuration of the semiconductor memory device according to the third embodiment.

As described above, the memory cell array 1 is provided in the semiconductor memory device 530, and the first and second memory cell blocks 1a and 1b are provided in the memory cell array 1. The first and second memory cell blocks 1a and 1b include multiple memory cell units 4. Multiple data control lines 7 are connected to each of the multiple memory cell units 4.

A selection transistor is disposed at each of the end portions of the multiple memory cell units 4 to select one of the multiple memory cell units 4 and connect the one memory cell unit 4 to the data transfer line BL (the data transfer lines BL1 to BL2n). The gate electrode of each of the selection transistors is connected to the selection gate line 5 and the selection gate line 6, respectively.

The data transfer lines BL extend in directions mutually orthogonal to the data control lines 7 and are disposed at prescribed spacings in directions mutually orthogonal to the data control lines 7.

The memory cell MC included in the memory cell unit 4 is provided at the intersection of the data transfer line BL and the data control line 7. The writing, retention, erasing, and reading of the data are possible independently for each of the memory cells MC.

The memory cell unit 4 is plurally provided along the stretching direction of the data transfer line BL (the X axis direction) and the stretching direction of the data control line 7 (the Y axis direction). The first memory cell block 1a includes multiple memory cell units 4 arranged along at least the Y axis

direction; and the second memory cell block 1b includes other multiple memory cell units 4 arranged along at least the Y axis direction.

Although two memory cell blocks (the first and second memory cell blocks 1a and 1b) are provided in FIG. 17, the number of memory cell blocks may be appropriately modified. Because of the address decoding, it is desirable for the number of the memory cell blocks to be a power-of-two integer.

The sense amplifier circuit 461 and the sense amplifier circuit 462 are connected to one end of the data transfer line BL.

In this embodiment, the sense amplifier circuit 461 and the sense amplifier circuit 462 are disposed on the one ends of the data transfer lines BL instead of being embedded in and between the memory cell blocks (the first and second memory cell blocks 1a and 1b). Thereby, the pattern periodicity of the memory cells MC can be maintained; and interconnects can be concentrated in one side of the memory cell blocks and can be shared and reduced. Thereby, the ratio of the semiconductor memory device 530 occupied by the memory cells MC can be increased.

The data control line driver 2 (the data control line drivers 2a and 2b) that drives the data control line 7 is provided on one end of the data control line 7 (i.e., the data control line WL, e.g. the data control lines WL11 to WL1b and the data control lines WL21 to WL2b) connected to the multiple memory cell units 4. The data control lines WL11 to WL1b and the selection gate line 5 are connected to the data control line driver 2a; and the data control lines WL21 to WL2b and the selection gate line 5 are connected to the data control line driver 2b.

For the multiple memory cell units 4 adjacent in the X axis direction as illustrated in FIG. 17, the data control line driver 2 is subdivided into the two data control line drivers 2a and 2b provided at the ends of the memory cell blocks, respectively, for easier disposition of the data control line driver

2 and to match the skew between the data control lines 7 of one memory cell block (e.g., the first memory cell block 1a).

In this embodiment, the data transfer lines (e.g. BL1, BL3, BL5, ..., BL $2n-3$, BL $2n-1$) of odd numbers (odd indexes) 5 in the Y axis direction are connected to the sense amplifier circuit 462. The data transfer lines (e.g. BL2, BL4, BL6, ..., BL $2n-2$, BL $2n$) of the even numbers (even indexes) in the Y axis direction are connected to the sense amplifier circuit 461.

As illustrated in FIG. 1, in the case where the data 10 transfer line is formed by sidewall patterning, the low resistance interconnect L1, which has a low interconnect resistance, is arranged alternately in the Y axis direction with the high resistance interconnect L2, which has an interconnect resistance higher than that of the low resistance interconnect L1. Thereby, 15 the interconnect resistance can be made uniform among the odd-numbered (odd index) data transfer lines and among the even-numbered (even index) data transfer lines. As a result, the delay time (interconnect delay) can be made uniform among the odd-numbered (odd index) data transfer lines and among 20 the even-numbered (even index) data transfer lines.

In other words, when the odd-numbered (odd index) data transfer lines and the even-numbered (even index) data transfer lines are each regarded as a group, the delay time (interconnect delay) can be made more uniform in each group 25 than in the case where the odd-numbered (odd index) data transfer lines and the even-numbered (even index) data transfer lines are mixed together.

Therefore, the fluctuation of the delay time (interconnect delay) between the data transfer lines connected to each of the 30 sense amplifier circuit 461 and the sense amplifier circuit 462 can be made smaller than the fluctuation of the delay time (interconnect delay) between all the data transfer lines.

Consequently, in the case where the read-out is performed simultaneously and the writing is performed 35 simultaneously on the memory cell units 4 connected to either the odd-numbered (odd index) data transfer lines or the

even-numbered (even index) data transfer lines, normal operations of the circuit are possible even when the circuit operation margin is reduced by an amount of the difference of the delay times (interconnect delay); and the circuit operation speed can be increased. Thereby, the read-out and the writing can be realized at speeds higher than those of conventional art.

Next, the case will now be illustrated where the read-out at still higher speed can be realized.

In this specific example, the read-out is performed separately with different timings between the odd-numbered (odd index) data transfer lines and the even-numbered (even index) data transfer lines. Here, when the read-out is performed simultaneously on adjacent data transfer lines, capacitive coupling due to a voltage fluctuation occurring in the data transfer lines influences both the adjacent data transfer lines. That is, capacitive coupling noise is a problem. In this specific example, the read-out is performed separately with different timings, and therefore the capacitive coupling noise can be reduced.

As described above, since there is a difference in interconnect resistance between the odd-numbered (odd index) data transfer line and the even-numbered (even index) data transfer line, a difference occurs in delay time (interconnect delay). Accordingly, at the time of the reading in this specific example, the read-out is performed with different timings between the odd-numbered (odd index) data transfer line and the even-numbered (even index) data transfer line.

In this case, the output of the sense amplifier circuit 461 or the sense amplifier circuit 462 connected to data transfer lines with a low interconnect resistance and capable of making a read-out speed higher may be selectively allotted to, for example, an even physical address.

For example, in the case where the interconnect resistance of the data transfer line connected to the sense amplifier circuit 461 is lower than the interconnect resistance of the data transfer line connected to the sense amplifier circuit

462, the output of the sense amplifier circuit 461 may be allotted to addresses 0, 2, 4, 6, ..., $2n$ (n being a positive integer), and the output of the sense amplifier circuit 462 may be allotted to addresses 1, 3, 5, 7, ..., $2n+1$ (n being a positive integer).

On the other hand, conversely, in the case where the interconnect resistance of the data transfer line connected to the sense amplifier circuit 462 is lower than the interconnect resistance of the data transfer line connected to the sense amplifier circuit 461, the output of the sense amplifier circuit 462 may be allotted to addresses 0, 2, 4, 6, ..., $2n$ (n being a positive integer), and the output of the sense amplifier circuit 461 may be allotted to addresses 1, 3, 5, 7, ..., $2n+1$ (n being a positive integer).

In both cases, the allotment of address can be performed using the data switching circuit 447.

The data of a memory cell allotted to an even address is output earlier. For example, in the case where the data of addresses "0, 1, 2, 3, ..." are continuously read out, in the case where the data of addresses "4, 5, 6, 7, ..." are continuously read out, etc., data output at still higher speed can be performed by making replacement in which the data of the memory cells allotted to the even addresses are output earlier.

This is because, in the case where, for example, data for every two bytes are output, data output at still higher speed can be performed if the data of the first one byte allotted to an even address allowing high-speed reading are output earlier when outputting one byte as a unit at a time via the I/O.

Which of the odd-numbered (odd index) data transfer line and the even-numbered (even index) data transfer line has the larger interconnect resistance may fluctuate with process fluctuations and the like. Therefore, a configuration may be employed in which alteration of the allotment of address is ready to be stored in, for example, a fuse, a ROM (read only memory), or the like and determined in a test process after lot trial manufacture or the like. In this case, the allotment of

address is preferably ready to be altered in a test process after the wafer process. Then, for example, the data stored in the fuse, ROM (read only memory), or the like are input into the input/output buffer 45, and the allotment of address is altered
5 with the data switching circuit 447.

Next, a description will now be given in which a necessary timing (read timing) for measuring the memory cell current at the time of reading, i.e., the time setting, is set differently between the sense amplifier circuit 461 and the
10 sense amplifier circuit 462 to speed up the reading.

FIGS. 18A and 18B are schematic views illustrating the read-out timing in the case where the read-out is performed when there is a difference in interconnect resistance. More specifically, the drawings are schematic views illustrating the
15 read-out timing in the case where the read-out is performed when there is a difference in interconnect resistance between the odd-numbered (odd index) data transfer line and the even-numbered (even index) data transfer line connected.

FIG. 18A is a schematic view illustrating an arrangement
20 of sense amplifier circuits, memory cell units, and the like. What is illustrated in FIG. 18A has a similar arrangement to what is illustrated in FIG. 17. A memory cell unit 4c is connected to the sense amplifier circuit 461 and represents the memory cell unit farthest from the sense amplifier circuit 461.
25 A memory cell unit 4b is connected to the sense amplifier circuit 462 and represents the memory cell unit farthest from the sense amplifier circuit 462. "c" represents the data transfer line end farthest from the sense amplifier circuit 461, and "b" represents the data transfer line end farthest from the sense
30 amplifier circuit 462.

Here in FIG. 18A, the odd-numbered (odd index) data transfer lines BL1, BL3, BL5, ... BL(2n-1) are connected to the sense amplifier circuit 462 drawn on the upper side. Furthermore, the even-numbered (even index) data transfer
35 lines BL2, BL4, BL6, ..., BL2n are connected to the sense amplifier circuit 461 drawn on the lower side. In this case, it is

assumed that the interconnect resistance of the odd-numbered (odd index) data transfer line is lower than the interconnect resistance of the even-numbered (even index) data transfer line. In the case where the interconnect resistance of the odd-numbered (odd index) data transfer line is higher than the interconnect resistance of the even-numbered (even index) data transfer line, a discussion can be provided on the supposition that the odd-numbered (odd index) data transfer line is replaced with the even-numbered (even index) data transfer line, and a description of the case is therefore omitted.

FIG. 18B is a schematic graph illustrating the change in voltage in "b" and "c" in the case where the sense amplifier circuit 461 and the sense amplifier circuit 462 are driven simultaneously.

As illustrated in FIG. 18B, a voltage is applied to the data transfer line by the sense amplifier circuit 461 and the sense amplifier circuit 462 from GND to VBL in a period from t_0 to t_1 . That is, charging is carried out from GND to VBL in the period from t_0 to t_1 . In this case, charging can be carried out in an almost equal period of time between data transfer lines, because the capacitance between data transfer lines is large and charging is performed so that adjacent data transfer lines may reach the same voltage VBL.

After that, the voltage of the data transfer line is kept constant from t_1 to t_2 . That is, a period (from t_1 to t_2) of keeping the voltage VBL constant is provided. Here, when the read-out of the memory cell is performed, for the memory cell to which current terminals are connected in series to the read-out memory cell, V_{read} , which is an electric potential higher than the maximum threshold voltage of the memory cell is applied to the data control line connected to the control gate.

In this case, assuming that the voltage of the data control line involved in the reading is V_{ref} , since the electric potential of a data control line adjacent thereto is V_{read} , the voltage of the data control line involved in the reading fluctuates from the voltage V_{ref} due to capacitive coupling. In

order to prevent misreading in the case of exceeding the threshold voltage due to the voltage fluctuation, the voltage of the data transfer line is kept constant for the period from t_1 to t_2 , which is longer than the time constant for stabilizing the voltage fluctuation by the capacitive coupling.

Here, for example, during the period from t_0 to t_1 , the voltage of the data control line involved in the reading is taken to be, for example, V_{ref} , the voltages of the other data control lines are taken to be V_{read} , and the selection transistor on the source line side and the selection transistor on the drain side are changed from the cutoff state to the conduction state to increase the electric potential of the data transfer line. Consequently, the NAND string involved in the reading is turned into the conduction state to increase the electric potential, and thereby the voltage of the data control line involved in the reading can be increased earlier than the voltages of the other data control lines. Therefore, a voltage increase due to the capacitive coupling of the channel portion of the NAND string caused by the voltage increases of the other data control lines to V_{read} can be prevented.

Next, during the period from t_1 to t_2 , the selection transistor on the source line side or the selection transistor on the drain side is changed from the conduction state to the cutoff state.

Subsequently, during the period from t_2 to t_3 , the charges stored in the data transfer line are discharged by, for example, changing the selection transistor on the source line side or the selection transistor on the drain side from the cutoff state to the conduction state.

At this time, the magnitude of the charge of the memory cell is evaluated with the sense amplifier circuit 461 and the sense amplifier circuit 462. For example, the magnitude of the charge of the memory cell is evaluated by measuring the magnitude of the electric potential of the data transfer line with the sense amplifier circuit 461 and the sense amplifier circuit 462 by comparing with a reference value (for example, V_{BL_th}

illustrated in FIG. 18B). Alternatively, the magnitude of the charge of the memory cell may be evaluated by measuring the current flowing through the data transfer line with the sense amplifier circuit 461 and the sense amplifier circuit 462.

5 Hereinbelow, although the two values of "1" and "0" of the erase state and the write state are used as an example, this embodiment can be applied also to multiple values as a matter of course. In that case, a threshold adjacent to an erase state and a write state may be taken as the threshold of the two
10 values.

 Here, it is assumed that the interconnect resistance of the odd-numbered (odd index) data transfer line is lower than the interconnect resistance of the even-numbered (even index) data transfer line. Accordingly, a larger discharge current can
15 be passed through the memory cell 4b connected to the odd-numbered (odd index) data transfer line than that through the memory cell 4c connected to the even-numbered (even index) data transfer line by a lowered amount of the interconnect resistance of the data transfer line even in the
20 case where the threshold voltages of the memory cells (the channel resistances of the memory cell transistors) are equal.

 Therefore, in the case where the logical value of the memory cell is "0" in FIG. 18B, that is, in the case of the write state (the threshold voltage of the memory cell being larger
25 than V_{ref}), since the V_{ref} value is lower than the write threshold voltage, the memory cell current does not flow and the electric potential of VBL is kept in both the memory cell connected to the even-numbered (even index) data transfer line and the memory cell connected to the odd-numbered (odd
30 index) data transfer line.

 On the other hand, in the case where the logical value of the memory cell is "1" in FIG. 18B, that is, in the case of, for example, the erase state (the threshold voltage of the memory cell being smaller than V_{ref}), since the V_{ref} value is higher than
35 the erase threshold voltage, the memory cell current flows and the voltage of the data transfer line decreases. In particular,

because the memory cell 4b connected to the odd-numbered (odd index) data transfer line has an interconnect resistance of the data transfer line lower than that of the memory cell 4c connected to the even-numbered (even index) data transfer line, the voltage decrease of the data transfer line is larger in the memory cell 4b.

Therefore, in the case where, for example, the logical value is evaluated through the threshold voltage of V_{BL_th} , in regard to a memory cell that is connected to the odd-numbered (odd index) data transfer line with a lower interconnect resistance and has the memory cell data of "1", the data transfer line voltage becomes lower than V_{BL_th} at the time of t_3' ; therefore, the evaluation of read data is possible on and after t_3' . On the other hand, in regard to a memory cell connected to the even-numbered (even index) data transfer line with a higher interconnect resistance, since the current flowing through the data transfer line is small, it is necessary to wait until the time of t_3 longer than t_3' in order that the data transfer line voltage may become lower than V_{BL_th} .

Here, in the conventional technology, the sense amplifier circuit 461 and the sense amplifier circuit 462 are driven simultaneously with the same timing. That is, the read-out is performed with the same timing between the memory cell connected to the even-numbered (even index) data transfer line and the memory cell connected to the odd-numbered (odd index) data transfer line. Therefore, it is necessary to wait until the longer timing of t_3 as the time of discharging the charges stored in the data transfer line.

Hereinbelow, it is assumed that t_3' is a shorter time than t_3 and t_4' is a shorter time than t_4 .

FIG. 19 is a flowchart illustrating the reading of data.

As illustrated in FIG. 19, the sense amplifier circuit 461 and the sense amplifier circuit 462 are used to output earlier the data of the memory cell connected to the data transfer line with a low interconnect resistance.

First, in step SE1, the data of the memory cell in the

memory cell unit 4 connected to the odd-numbered (odd index) data transfer line are read out with the read-out timings of t_1 , t_2 , t_3 , and t_4 and stored in the data latch of the sense amplifier circuit 461.

5 Subsequently, in step SE2, the data of the memory cell of the memory cell unit 4 connected to the even-numbered (even index) data transfer line are read out with the read-out timings of t_1 , t_2 , t_3 , and t_4 and stored in the data latch of the sense amplifier circuit 462.

10 In this case, in the conventional technology, the read-out performed in steps SE1 and SE2 is performed with the same read-out timing. Therefore, the read time is the same between the sense amplifier circuit 461 and the sense amplifier circuit 462. In other words, the read-out performed in steps SE1 and
15 SE2 are in accord with the longer read time.

Next, in step SE3, the data stored in the data latch of the sense amplifier circuit 461 and the data stored in the data latch of the sense amplifier circuit 462 are output through the input/output buffer 45 in the predetermined order.

20 In this case, a logical address of the memory cell stored in the data latch of the sense amplifier circuit 461, a logical address of the memory cell stored in the data latch of the sense amplifier circuit 462 are allotted in advance in a prescribed way and are not changed.

25 Accordingly, also in this case, since an even-numbered (even index) data transfer line and an even-numbered (even index) data transfer line form a group, the delay time (interconnect delay) can be made more uniform than in the case where the odd-numbered (odd index) data transfer line
30 and the even-numbered (even index) data transfer line are mixed together.

As a consequence, the fluctuation of delay time (interconnect delay) between the data transfer lines connected to each of the sense amplifier circuit 461 and the sense
35 amplifier circuit 462 can be made smaller than the fluctuation of delay time (interconnect delay) in the case where all the data

transfer lines are mixed together to be connected to the sense amplifier.

Therefore, in the cases where the read-out is performed simultaneously or the writing is performed simultaneously on the data stored in the memory cells included in the memory cell units 4 connected to either the odd-numbered (odd index) data transfer lines or the even-numbered (even index) data transfer lines, normal operations of the circuit are possible even when the circuit operation margin is reduced by an amount of the difference of the delay times (interconnect delay); and the circuit operation speed can be increased. Thereby, the read-out and the writing can be realized at speeds higher than those of conventional art.

Also in the case where the memory cell connected to the even-numbered (even index) data transfer line is replaced with the memory cell connected to the odd-numbered (odd index) data transfer line in the above case, the logical address as a memory is allotted in advance in a prescribed way. In this case, in the conventional technology, the read-out performed in steps SE1 and SE2 is performed with the same read-out timing. Therefore, the read time is the same between the sense amplifier circuit 461 and the sense amplifier circuit 462. The read-out performed in steps SE1 and SE2 are in accord with the longer read time.

FIGS. 20A to 20C are schematic views illustrating another example of the read-out timing in the case where the read-out is performed when there is a difference in interconnect resistance. More specifically, these are schematic views illustrating another example of the read-out timing in the case where the read-out is performed when there is a difference in interconnect resistance between the odd-numbered (odd index) data transfer line and the even-numbered (even index) data transfer line connected.

FIG. 20A is a schematic view illustrating an arrangement of sense amplifier circuits, memory cell units, and the like. What is illustrated in FIG. 20A has a similar arrangement to

what is illustrated in FIG. 17.

A memory cell unit 4a is connected to the sense amplifier circuit 461 and represents the memory cell unit nearest to the sense amplifier circuit 461. The memory cell unit 4c is
 5 connected to the sense amplifier circuit 461 and represents the memory cell unit farthest from the sense amplifier circuit 461. A memory cell unit 4d is connected to the sense amplifier circuit 462 and represents the memory cell unit nearest to the sense amplifier circuit 462. The memory cell unit 4b is connected to
 10 the sense amplifier circuit 462 and represents the memory cell unit farthest from the sense amplifier circuit 462. "c" represents the data transfer line end farthest from the sense amplifier circuit 461, and "b" represents the data transfer line end farthest from the sense amplifier circuit 462.

15 Here, in FIG. 20A, the odd-numbered (odd index) data transfer lines BL1, BL3, BL5, ..., BL(2n-1) are connected to the sense amplifier circuit 462 drawn on the upper side. Furthermore, the even-numbered (even index) data transfer lines BL2, BL4, BL6, ..., BL2n are connected to the sense
 20 amplifier circuit 461 drawn on the lower side. In this case, it is assumed that the interconnect resistance of the odd-numbered (odd index) data transfer line is lower than the interconnect resistance of the even-numbered (even index) data transfer line. In the case where the interconnect resistance of the
 25 odd-numbered (odd index) data transfer line is higher than the interconnect resistance of the even-numbered (even index) data transfer line, a discussion can be provided on the supposition that the odd-numbered (odd index) data transfer line is replaced with the even-numbered (even index) data transfer
 30 line, and a description of the case is therefore omitted.

FIG. 20B is a schematic graph illustrating the change in voltage in the case where the sense amplifier circuit 461 and the sense amplifier circuit 462 are driven with different timings. A description similar to that of FIG. 18B described above is
 35 omitted as appropriate.

FIG. 20B illustrates the change in voltage at or around

the connection of the memory cell 4b.

The case illustrated in FIG. 20A assumes that the interconnect resistance of the odd-numbered (odd index) data transfer line is lower than the interconnect resistance of the even-numbered (even index) data transfer line. Therefore, even in the case where the memory cells have the same resistance, a larger discharge current can be passed through the memory cells 4b and 4d connected to the odd-numbered (odd index) data transfer line than that through the memory cells 4c and 4a connected to the even-numbered (even index) data transfer line by a lowered amount of the interconnect resistance of the data transfer line.

Accordingly, in the case where the logical value of the memory cell is "0" in FIG. 20B, that is, in the write state, since the V_{ref} value is lower than the write threshold voltage, the memory cell current does not flow, and the electric potential of VBL is kept in both the memory cell connected to the even-numbered (even index) data transfer line and the memory cell connected to the odd-numbered (odd index) data transfer line.

On the other hand, in the case where the logical value of the memory cell is "1" in FIG. 20B, that is, for example, in the case of the erase state, since the V_{ref} value is higher than the erase threshold voltage, the memory cell current flows and the voltage of the data transfer line decreases. In particular, because the memory cell 4b connected to the odd-numbered (odd index) data transfer line has an interconnect resistance of the data transfer line lower than that of the memory cell 4c connected to the even-numbered (even index) data transfer line, the voltage decrease of the data transfer line is larger in the memory cell 4b.

Therefore, in the case where, for example, the logical value is evaluated through the threshold voltage of V_{BL_th} , in regard to a memory cell that is connected to the odd-numbered (odd index) data transfer line with a lower interconnect resistance and has the memory cell data of "1", the data

transfer line voltage becomes lower than VBL_{th} at the time of $t3'$; therefore, the evaluation of read data is possible on and after $t3'$. On the other hand, in regard to a memory cell connected to the even-numbered (even index) data transfer line with a higher interconnect resistance, since the current flowing through the data transfer line is small, it is necessary to wait until the time of $t3$ longer than $t3'$ in order that the data transfer line voltage may become lower than VBL_{th} .

Here, because the memory cells nearer to the sense amplifier circuit 461 and the sense amplifier circuit 462 have a lower interconnect resistance of the data transfer line, the voltage decrease amount of the read-out voltage of the data transfer line corresponding to a read-out signal amount is greater. For example, as illustrated in FIG. 20C, even for memory cells connected to the same data transfer line, the read time can be shortened more in the memory cell 4d nearer to the sense amplifier circuit 462 than in the memory cell 4b. That is, the read time $t3'$ of the memory cell 4d illustrated in FIG. 20C can be made shorter than the read time $t3$ of the memory cell 4b illustrated in FIG. 20B.

FIG. 21 is a flowchart illustrating the reading of data in the case described in FIGS. 20A to 20C.

As illustrated in FIG. 21, the sense amplifier circuit 461 and the sense amplifier circuit 462 are used to output earlier the data of a memory cell nearer to the sense amplifier circuit out of the memory cells connected to the data transfer line with a low interconnect resistance.

First, in step SE4, it is evaluated whether or not the period of the read sequence (the period from the start of the reading to the end, i.e., from $t0$ to $t4$ or $t4'$) is shorter in the memory cell connected to the sense amplifier circuit 461 via the data transfer line than in the memory cell connected to the sense amplifier circuit 462 via the data transfer line.

In this case, the evaluation criteria can be found by, for example, checking the read times of the memory cells 4b and 4c after the manufacturing of the semiconductor memory device.

For example, the evaluation criteria can be found by measuring the read time from t_1 to t_4 or from t_1 to t_4' using the memory cell 4c connected to the sense amplifier circuit 461 and the memory cell 4b connected to the sense amplifier circuit 462.

- 5 Then, the timings allowing the reading in a short time are set shorter than t_1 , t_2 , t_3' , and t_4' or t_1 , t_2 , t_3 , and t_4 .

This setting may use, for example, data stored in a ROM in the semiconductor memory device or data stored in a fuse.

- 10 This specific example has a feature in which a parameter determining the timing of the read time of the memory cell connected to the sense amplifier circuit 461 and a parameter determining the timing of the read time of the memory cell connected to the sense amplifier circuit 462 are separately retained in a ROM or a fuse.

- 15 In the case of the option "Yes" in step SE4, a memory cell of a memory cell unit 4 connected to one data control line is read out to the data latch of the sense amplifier circuit 461 with the read-out timings of t_1 , t_2 , t_3' , and t_4' in step SE5.

- 20 In this specific example, the data of the memory cell connected to the data transfer line with a low interconnect resistance are read out earlier, and therefore the discharge time of the data transfer line can be made shorter than in the case of step SE1 described above.

- 25 Subsequently, in step SE6, the data of a memory cell connected to the same data control line as that read out in step SE5 are read out to the data latch of the sense amplifier circuit 462 with the read-out timings of t_1 , t_2 , t_3 , and t_4 .

- 30 Subsequently, in step SE7, the data stored in the data latch of the sense amplifier circuit 461 are firstly output through the input/output buffer 45.

Subsequently, in step SE8, the data stored in the data latch of the sense amplifier circuit 462 are output through the input/output buffer 45.

- 35 Thereby, the data read out at the sense amplifier circuit 461 with an earlier timing than at the sense amplifier circuit 462 can be output earlier in step SE7. Therefore, faster data

output can be performed.

In the case of the option "No" in step SE4, in step SE9 a memory cell of a memory cell unit 4 connected to one data control line is read out to the data latch of the sense amplifier circuit 462 with the read-out timings of t_1 , t_2 , t_3' , and t_4' .

In this specific example, the data transfer line with a low interconnect resistance is read out, and therefore the discharge time of the data transfer line can be made shorter than in the case of step SE1 described above.

Subsequently, in step SE10, the data of a memory cell connected to the same data control line as that read out in step SE9 are read out to the data latch of the sense amplifier circuit 461 with the read-out timings of t_1 , t_2 , t_3 , and t_4 .

Subsequently, in step SE11, the data stored in the data latch of the sense amplifier circuit 462 are firstly output through the input/output buffer 45.

Subsequently, in step SE12, the data stored in the data latch of the sense amplifier circuit 461 are output through the input/output buffer 45.

Thereby, the data read out at the sense amplifier circuit 462 with an earlier timing than at the sense amplifier circuit 461 can be output earlier in step SE11. Therefore, faster data output can be performed.

By using step SE4 to step SE12 described above, in this specific example, the logical addresses of the memory cells are interchanged between the data of the memory cell stored in the data latch of the sense amplifier circuit 461 and the data of the memory cell stored in the data latch of the sense amplifier circuit 462. Thereby, the data of the memory cell connected to the data transfer line with a low interconnect resistance can be output earlier than the data of the memory cell connected to the data transfer line with a high interconnect resistance.

In this specific example, in regard to the timings t_0 , t_1 , and t_2 of the data reading of the even-numbered (even index) data transfer line and the odd-numbered (odd index) data transfer line, the read-out may be performed simultaneously for

the even-numbered (even index) data transfer line and the odd-numbered (odd index) data transfer line to shorten the time of the read sequence.

For example, during the period from t_0 to t_1 , the voltage of the data control line involved in the reading is taken to be, for example, V_{ref} , the voltages of the other data control lines are taken to be V_{read} , and the selection transistor on the source line side and the selection transistor on the drain side are changed from the cutoff state to the conduction state to increase the electric potential of the data transfer line. Consequently, the NAND string involved in the reading is turned into the conduction state to increase the electric potential, and thereby the voltage of the data control line involved in the reading can be increased earlier than the voltages of the other data control lines. Therefore, a voltage increase due to the capacitive coupling of the channel portion of the NAND string caused by the voltage increases of the other data control lines to V_{read} can be prevented.

Next, during the period from t_1 to t_2 , the selection transistor on the source line side or the selection transistor on the drain side is changed from the conduction state to the cutoff state.

Then, for example, during the period from t_2 to t_3' in step SE5 or step SE9, the selection transistor on the source line side or the selection transistor on the drain side is changed from the cutoff state to the conduction state to read out the data of the memory cell to the sense amplifier circuit.

Furthermore, during the period from t_2 to t_3 in step SE6 or step SE10, the selection transistor on the source line side or the selection transistor on the drain side is changed from the cutoff state to the conduction state to read out the data of the memory cell to the sense amplifier circuit.

According to the semiconductor memory device 530 according to the third embodiment, the odd-numbered (odd index) data transfer lines and the even-numbered (even index) data transfer lines are each regarded as a group and can

thereby make the delay time (interconnect delay) more uniform than in the case where all the data transfer lines are mixed together.

Therefore, the fluctuation of delay time (interconnect delay) between the data transfer lines connected to each of the sense amplifier circuit 461 and the sense amplifier circuit 462 can be made smaller than the fluctuation of delay time (interconnect delay) in the case where all the data transfer lines are mixed together to be connected to the sense amplifier circuit.

As a consequence, in the cases where the read-out is performed simultaneously and the writing is performed simultaneously on the memory cell units 4 connected to either the odd-numbered (odd index) data transfer lines or the even-numbered (even index) data transfer lines, normal operations of the circuit are possible even when the circuit operation margin is reduced by an amount of the difference of the delay times (interconnect delay); and the circuit operation speed can be increased. Thereby, the read-out and the writing can be realized at speeds higher than those of conventional art.

Furthermore, the output from the sense amplifier circuit 461 and the output from the sense amplifier circuit 462 are performed with different timings by the control circuit 40. Thus, the circuit operation speed can be increased, and therefore the read-out and the writing can be realized at speeds higher than those of conventional art.

Furthermore, the data of the memory cell connected to the data transfer line with a low interconnect resistance can be output earlier. For example, the output from the sense amplifier circuit connected to the data transfer line with a low interconnect resistance can be performed earlier than the output from the sense amplifier circuit connected to the data transfer line with a high interconnect resistance. Consequently, the read-out and the writing at higher speeds can be realized.

Furthermore, the data of a memory cell nearer to the sense amplifier circuit out of the memory cells connected to the

data transfer line can be output earlier. The output for a memory cell placed nearer to the sense amplifier circuit 461 on the data transfer line can be performed earlier than the output for a memory cell placed in a farther position. Furthermore, 5 the output for a memory cell placed nearer to the sense amplifier circuit 462 on the data transfer line can be performed earlier than the output for a memory cell placed in a farther position.

That is, in the case where the data read time of the 10 multiple memory cells included in the multiple first memory cell units connected to the multiple first interconnects is shorter than the data read time of the multiple memory cells included in the multiple second memory cell units connected to the multiple second interconnects, the control circuit 40 allows the data of 15 the multiple memory cells included in the multiple first memory cell units to be output earlier than the data of the multiple memory cells included in the multiple second memory cell units. Consequently, the read-out and the writing at still higher speed can be realized. Therefore, a semiconductor memory device 20 with improved operating characteristics and reliability can be provided.

Next, a variation of the semiconductor memory device according to the third embodiment will now be described.

FIG. 22 is a schematic circuit diagram illustrating a 25 layout of the memory cell array and the data transfer line.

As illustrated in FIG. 22, in a semiconductor memory device 531, the sense amplifier circuit 461 and the sense amplifier circuit 462 are not provided to face each other across the memory cell array 1, but are disposed collectively on one 30 side of the memory cell array 1.

That is, the sense amplifier circuit 461 and the sense amplifier circuit 462 are collectively disposed.

In other words, in this variation, the sense amplifier circuit 461 connected to one end of the even-numbered (even 35 index) data transfer line and the sense amplifier circuit 462 connected to one end of the odd-numbered (odd index) data

transfer line are collectively disposed on the same side with respect to the memory cell array 1. Therefore, a peripheral circuit and a power source interconnect can be disposed concentratedly. Furthermore, by disposing the sense amplifier circuit 461 and the sense amplifier circuit 462 collectively in this way, the lengths of the data transfer lines connected to each of the sense amplifier circuit 461 and the sense amplifier circuit 462 can be made almost equal. Therefore, there is also an effect in which the fluctuation between the data transfer lines for the memory cells connected to each of the sense amplifier circuit 461 and the sense amplifier circuit 462 can be made small.

In this case, since the even-numbered (even index) data transfer line connected to the sense amplifier circuit 462 crosses over the sense amplifier circuit 461, the length of the even-numbered (even index) data transfer line is longer than the length of the odd-numbered (odd index) data transfer line.

Accordingly, in regard to the sense amplifier circuit, the sense amplifier circuit 462 has a larger CR time constant and requires a longer read time than the sense amplifier circuit 461. Therefore, the read time is measured in the memory cell 4c connected to the sense amplifier circuit 461 and the memory cell 4b connected to the sense amplifier circuit 462, and the timings allowing the reading in a short time are set shorter than t_1 , t_2 , t_3' , or t_4' or t_1 , t_2 , t_3 , and t_4 . Then, as described in the third embodiment described above, the read-out timing is switched between the sense amplifier circuit 461 and the sense amplifier circuit 462; thereby, the read time can be shortened.

In this case, as described in the third embodiment described above, the parameter determining the timing of the read time of the sense amplifier circuit 461 and the parameter determining the timing of the read time of the sense amplifier circuit 462 are retained separately in a ROM or a fuse.

In the case of this variation, the wording of the phrase may be changed as follows: the memory cell 4b is connected to the sense amplifier circuit 462 and represents a memory cell far

from the sense amplifier circuit 462; and the memory cell 4c is connected to the sense amplifier circuit 461 and represents a memory cell far from the sense amplifier circuit 461.

Also the semiconductor memory device according to this variation can obtain effects similar to those of the semiconductor memory device 530 according to the third embodiment described above.

Furthermore, since the sense amplifier circuit 461 and the sense amplifier circuit 462 are disposed collectively on one side of the memory cell array 1, a peripheral circuit and a power source interconnect can be disposed concentratedly. Furthermore, by disposing the sense amplifier circuit 461 and the sense amplifier circuit 462 collectively in this way, the lengths of the data transfer lines connected to each of the sense amplifier circuit 461 can be made almost equal, and the lengths of the data transfer lines connected to each of the sense amplifier circuit 462 can be made almost equal. Therefore, there is also an effect to reduce the fluctuation among the data transfer lines for the memory cells connected to each of the sense amplifier circuit 461, and to reduce the fluctuation among the data transfer lines for the memory cells connected to each of the sense amplifier circuit 462.

Fourth embodiment

FIG. 23 is a block diagram illustrating the configuration of a semiconductor memory device according to a fourth embodiment.

A NAND EEPROM is used again as an example to describe a semiconductor memory device 540 according to the fourth embodiment.

What is illustrated in FIG. 23 is the same as what is illustrated in FIG. 16 except that the even-numbered (even index) data transfer line and the odd-numbered (odd index) data transfer line are connected to one sense amplifier circuit 463 via a data transfer line switching circuit 491. A description of matters similar to what are illustrated in FIG. 16 and the like

is omitted as appropriate.

The first and second memory cell blocks 1a and 1b are provided in the memory cell array 1. The regions where the first and second memory cell blocks 1a and 1b are provided are the first and second regions RG1 and RG2, respectively. As described below, the plural memory cell units 4 are provided in the first and second memory cell blocks 1a and 1b; and the memory cell unit 4 includes multiple nonvolatile memory cells connected in series.

The sense amplifier circuit 463 is provided on one side of the memory cell array 1 via the data transfer line switching circuit 491 to detect data from the data transfer line provided in the memory cell array 1 or retain write data. The sense amplifier circuit 463 functions also as a data latch and includes, for example, a flip-flop circuit.

The sense amplifier circuit 463 is connected to the input/output buffer 45. A column decoder 483 for designating the address of the sense amplifier circuit 463 is provided. These select a column of which the address is designated by the column decoder 483, and form a circuit necessary for performing the read-out and writing of data.

Accordingly, the data transfer from the sense amplifier circuit 463 to the input/output buffer 45 is controlled by the output of the column decoder 483 that receives the address signal 47a from the address buffer 47.

The row decoder 3 selects memory cells in the memory cell array 1. Specifically, the row decoder 3 controls the control gate line 7 and the selection gate lines 5 and 6.

FIG. 24 is a schematic circuit diagram illustrating the configuration of the semiconductor memory device according to the fourth embodiment.

As described above, the memory cell array 1 is provided in the semiconductor memory device 540, and the first and second memory cell blocks 1a and 1b are provided in the memory cell array 1. The first and second memory cell blocks 1a and 1b include multiple memory cell units 4. Multiple data

control lines 7 are connected to each of the multiple memory cell units 4.

A selection transistor is disposed at each of the end portions of the memory cell unit 4 to select one of the multiple memory cell units 4 and connect the one memory cell unit 4 to the data transfer line BL (the data transfer lines BL1 to BL2n). The gate electrode of each of the selection transistors is connected to the selection gate line 5 and the selection gate line 6, respectively.

The data transfer lines BL extend in directions mutually orthogonal to the data control line 7 and are disposed at prescribed spacings in directions mutually orthogonal to the data control line 7.

The memory cells MC included in the memory cell unit 4 are provided at intersections between the data transfer line BL and the data control lines 7. The writing, retention, erasing, and reading of the data are possible independently for each of the memory cells MC.

The memory cell unit 4 is plurally formed along the direction of the data transfer line and the direction of the data control line 7 to form a memory cell matrix. In FIG. 24, the connection portion between the memory cell units 4 and the data transfer line is omitted for easier viewing of the drawing. However, as illustrated in FIG. 4B, these are connected to the data transfer line via the selection transistor on the block selection line SSL side.

The sense amplifier circuit 463 is connected to one end of the data transfer line via a transistor Q1 or Q2. In this embodiment, the sense amplifier circuit 463 is disposed collectively at one ends of the data transfer lines BL instead of being embedded in and between the memory cell blocks (the first and second memory cell blocks 1a and 1b) to increase the occupation ratio of the memory cells by maintaining the pattern periodicity of the memory cells and using a configuration having an interconnect and transistor pattern simpler than that of the sense amplifier circuit.

The data transfer line switching circuit 491 switches between the connection of the sense amplifier circuit 463 with the even-numbered (even index) data transfer line and the connection of the sense amplifier circuit 463 with the odd-numbered (odd index) data transfer line.

In this embodiment, the data transfer line switching circuit 491 is composed of the transistors Q1 and Q2 illustrated in FIG. 24. The data transfer line switching circuit 491 formed of the transistors Q1 and Q2 forms a circuit for connecting the even-numbered (even index) data transfer line (e.g. BL2, BL4, BL6, ..., BL2n-2, BL2n) and the odd-numbered (odd index) data transfer line (e.g. BL1, BL3, BL5, ..., BL2n-3, BL2n-1) selectively to the sense amplifier circuit 463.

The control circuit 40 controls the signal to the control gate terminals SEN1 and SEN2 of the transistors Q1 and Q2 composing the data transfer line switching circuit 491. Thereby, the odd-numbered (odd index) data transfer line and the even-numbered (even index) data transfer line are switched. That is, by a control circuit 40a, the output of the memory cell unit connected to the odd-numbered (odd index) data transfer line and the output of the memory cell unit connected to the even-numbered (even index) data transfer line can be performed with different timings.

As illustrated in FIG. 24, the data control line driver 2 (the data control line drivers 2a and 2b) that drives the data control line 7 is provided at one end of the data control line 7 to which multiple memory cell units 4 are connected.

Here, for the multiple memory cell units 4 adjacent in the X axis direction as illustrated in FIG. 24, the data control line driver 2 is subdivided into the two data control line drivers 2a and 2b provided at the both ends of the memory cell blocks, respectively, for easier disposition of the data control line drivers 2 and to match the skew between data control lines 7 of one memory cell block (e.g. the first memory cell block 1a).

As illustrated in FIG. 1, in the case where the data transfer line is formed by sidewall patterning, the low resistance

interconnect L1, which has a low interconnect resistance, is arranged alternately in the Y axis direction with the high resistance interconnect L2, which has an interconnect resistance higher than that of the low resistance interconnect L1. As a consequence, the interconnect resistance can be made uniform among the odd-numbered (odd index) data transfer lines, and among the even-numbered (even index) data transfer lines. Consequently, the delay time (interconnect delay) can be made uniform among the odd-numbered (odd index) data transfer lines, and among the even-numbered (even index) data transfer lines.

That is, when the odd-numbered (odd index) data transfer lines and the even-numbered (even index) data transfer lines are each regarded as a group, the delay time (interconnect delay) can be made more uniform in each group than in the case where the odd-numbered (odd index) data transfer lines and the even-numbered (even index) data transfer lines are mixed together.

Therefore, the fluctuation of the delay time (interconnect delay) between data transfer lines can be made smaller in the case where either the odd-numbered (odd index) data transfer lines or the even-numbered (even index) data transfer lines are connected to the sense amplifier circuit 463 by the data transfer line switching circuit 491 than in the case where all the data transfer lines are mixed together to be connected to the sense amplifier circuit.

As a consequence, in the cases where the read-out is performed simultaneously and the writing is performed simultaneously on the memory cell units 4 connected to either the odd-numbered (odd index) data transfer lines or the even-numbered (even index) data transfer lines, normal operations of the circuit are possible even when the circuit operation margin is reduced by an amount of the difference of the delay times (interconnect difference); and the circuit operation speed can be increased. Thereby, the read-out and the writing can be realized at speeds higher than those of

conventional art.

Here, similarly to what is illustrated in the third embodiment, the timings allowing the reading may be set different between the even-numbered (even index) data transfer line and the odd-numbered (odd index) data transfer line, i.e., set to t_1 , t_2 , t_3' , or t_4' and t_1 , t_2 , t_3 , and t_4 , respectively. Thereby, the read time can be shortened.

Similarly to what is illustrated in FIG. 21, first, the read time of the memory cell farthest from the sense amplifier circuit 463 connected to the odd-numbered (odd index) data transfer line and the read time of the memory cell farthest from the sense amplifier circuit 463 connected to the even-numbered (even index) data transfer line are compared. Then, the timings allowing the reading in a short time are set shorter than t_1 , t_2 , t_3' , and t_4' or t_1 , t_2 , t_3 , and t_4 . This setting may be use, for example, data stored in a ROM in the semiconductor memory device or data stored in a fuse.

Therefore, this embodiment has a feature in which the parameter determining the timing of the read time of the memory cell connected to the odd-numbered (odd index) data transfer line and the parameter determining the timing of the read time of the memory cell connected to the even-numbered (even index) data transfer line are separately retained in a ROM or a fuse.

Furthermore, in this embodiment, the logical address as a memory is replaced between the data of the memory cell connected to the odd-numbered (odd index) data transfer line and the data of the memory cell connected to the even-numbered (even index) data transfer line. Thereby, the data of the memory cell connected to the data transfer line with a low interconnect resistance can be output earlier than the data of the memory cell connected to the data transfer line with a high interconnect resistance.

Also in this embodiment, in regard to the timings t_0 , t_1 , and t_2 of the data reading of the even-numbered (even index) data transfer line and the odd-numbered (odd index) data

transfer line, the read-out may be performed simultaneously for the even-numbered (even index) data transfer line and the odd-numbered (odd index) data transfer line to shorten the time of the read sequence.

5 For example, during the period from t_0 to t_1 , the voltage of the data control line involved in the reading is taken to be, for example, V_{ref} , the voltages of the other data control lines are taken to be V_{read} , and the selection transistor on the source line side and the selection transistor on the drain side
10 are changed from the cutoff state to the conduction state to increase the electric potential of the data transfer line. Consequently, the NAND string involved in the reading is turned into the conduction state to increase the electric potential, and thereby the voltage of the data control line involved in the
15 reading can be increased earlier than the voltages of the other data control lines. Therefore, a voltage increase due to the capacitive coupling of the channel portion of the NAND string caused by the voltage increases of the other data control lines to V_{read} can be prevented.

20 Next, during the period from t_1 to t_2 , the selection transistor on the source line side or the selection transistor on the drain side is changed from the conduction state to the cutoff state.

 Then, for example, during the period from t_2 to t_3' in
25 step SE5 or step SE9 described above, the selection transistor on the source line side or the selection transistor on the drain side is changed from the cutoff state to the conduction state to read out the data of the memory cell to the sense amplifier circuit.

30 Furthermore, during the period from t_2 to t_3 in step SE6 or step SE10 described above, the selection transistor on the source line side or the selection transistor on the drain side is changed from the cutoff state to the conduction state to read out the data of the memory cell to the sense amplifier circuit.

35 Also in the semiconductor memory device 540 according to the fourth embodiment, the odd-numbered (odd index) data

transfer lines and the even-numbered (even index) data transfer lines each are regarded as a group and can thereby make the delay time (interconnect delay) more uniform than in the case where all the data transfer lines are mixed together.

5 Therefore, the fluctuation of the delay time (interconnect delay) between data transfer lines can be made smaller in the case where either the odd-numbered (odd index) data transfer lines or the even-numbered (even index) data transfer lines are connected to the sense amplifier circuit 463 by the data transfer
10 line switching circuit 491 than in the case where all the data transfer lines are mixed together to be connected to the sense amplifier circuit.

 As a consequence, normal operations of the circuit are possible even when the circuit operation margin is reduced by
15 an amount of the difference of the delay times (interconnect delay); and the circuit operation speed can be increased. Thereby, the read-out and the writing can be realized at speeds higher than those of conventional art.

 Furthermore, by the control circuit 40a, the output of the
20 memory cell included in the memory cell unit connected to the odd-numbered (odd index) data transfer line and the output of the memory cell included in the memory cell unit connected to the even-numbered (even index) data transfer line are performed with different timings. Thus, the circuit operation
25 speed can be increased. Thereby, the read-out and the writing can be realized at speeds higher than those of conventional art.

 Furthermore, the data of the memory cell connected to the data transfer line with a low interconnect resistance can be output earlier. For example, the output of the memory cell
30 included in the memory cell unit connected to the data transfer line with a low interconnect resistance can be performed earlier than the output of the memory cell included in the memory cell unit connected to the data transfer line with a high interconnect resistance. Consequently, the read-out and the writing can be
35 realized at higher speeds.

 Moreover, the data of a memory cell nearer to the sense

amplifier circuit out of the memory cells connected to the data transfer line with a low interconnect resistance can be output earlier. The data output of a memory cell provided nearer to the sense amplifier circuit 463 on the data transfer line with a low interconnect resistance can be performed earlier than the data output of a memory cell provided in a farther position. The data output of the memory cell provided nearer to the sense amplifier circuit 463 on the data transfer line with a high interconnect resistance can be performed earlier than the data output of a memory cell provided in a farther position. That is, in the case where the data read time of the memory cells included in the first memory cell units 1b connected to the first interconnects is shorter than the data read time of the memory cells included in the second memory cell units 1a connected to the second interconnects, the control circuit 40a allows the data of the memory cells included in the first memory cell units to be output earlier than the data of the memory cells included in the second memory cell units. Consequently, the read-out and the writing can be realized at still higher speeds. Therefore, a semiconductor memory device with improved operating characteristics and reliability can be provided.

Fifth embodiment

Next, a semiconductor memory device according to a fifth embodiment will now be illustrated.

First, a description is given of a decrease in read speed caused by a decrease of a current I_{cell} flowing through the memory cell.

In the case where the voltage applied to the data transfer line is constant, the current I_{cell} flowing through the memory cell connected farthest from the sense amplifier circuit is small compared to memory cells connected near to the sense amplifier circuit because the series resistance of the data transfer line is added one upon another in the memory cell farthest from the sense amplifier circuit.

FIG. 25 is a schematic graph illustrating the

current-voltage characteristics of the memory cell.

FIG. 25 illustrates the case where, for example, a constant voltage between 0.3 V and 1 V is applied to the drain electrode. The horizontal axis represents the gate voltage to the source voltage of the memory cell transistor, and the vertical axis represents the logarithmic expression of the drain current of the memory cell.

As illustrated in FIG. 25, the variation width in threshold voltage due to the subthreshold coefficient increases as the current (drain current) flowing through the memory cell decreases.

The solid line in the drawing represents the current-voltage characteristics of a memory cell having a typical threshold voltage. In the case where the drain current of the memory cell is sufficiently low as compared to the pentode threshold voltage, subthreshold characteristics depending on the gate voltage logarithmically are exhibited.

The broken line in the drawing represents the current-voltage characteristics of a memory cell with a low threshold voltage. Here, in the memory cell with a low threshold voltage, for example, the effective gate length is shorter than that in the memory cell with a normal threshold voltage. When a constant voltage between 0.3 V and 1 V is applied to the drain electrode, a large amount of punch through current flows between drain and source as compared to the case of the memory cell having a normal threshold voltage, leading to the worsening of the short channel effects. Consequently, the gradient of the subthreshold characteristics is larger than those in the case of the memory cell having a normal threshold voltage.

On the other hand, the alternate long and short dash line in the drawing represents the current-voltage characteristics of a memory cell with a high threshold voltage. Here, in the memory cell with a high threshold voltage, for example, the effective gate length is longer than in the memory cell with a normal threshold voltage. When a constant voltage between

0.3 V and 1 V is applied to the drain electrode, the punch through current flowing between drain and source is suppressed as compared to the case of the memory cell having a normal threshold voltage, improving the short channel effects.

5 Consequently, the gradient of the subthreshold characteristics is smaller than those in the case of the memory cell having a normal threshold voltage.

Here, the variation in the threshold voltage of the memory cell is compared between I1 that is a large amount of drain current flowing through the memory cell and I2 that is a small amount of drain current. As illustrated in FIG. 25, the variation in threshold voltage in the case of the drain current I1 is threshold width 1, and the variation in threshold voltage in the case of the drain current I2 is threshold width 2. Threshold

10 voltage width 2 in the case where the current is lower is larger than threshold voltage width 1. Such a variation in the subthreshold coefficient of the memory cell increases the variation in threshold voltage between memory cells in the case where the current flowing through the memory cell is lower.

20 On the other hand, if it is attempted to make large the voltage amplitude ΔV of the data transfer line end connected to the sense amplifier circuit, the problem occurs in which a sufficient memory cell current cannot be obtained in the memory cell farthest from the sense amplifier circuit.

25 Furthermore, what influence the time until the current of the data transfer line is stabilized include a component proportional to (Data transfer line capacitance) $\times$ ($\Delta V/I_{\text{cell}}$), other than the delay corresponding to the time constant of the product of (Capacitance of data transfer line) $\times$ (Resistance of data transfer line), due to capacitive coupling between data

30 transfer lines. Accordingly, the delay increases as the voltage amplitude ΔV of the data transfer line end connected to the sense amplifier circuit increases.

In this case, if the voltage amplitude ΔV of the data transfer line end is made small, a sense amplifier circuit with a

35 high sensitivity is needed. To obtain a sense amplifier circuit

with a high sensitivity, for example, it is necessary for the transistor used for the input of the sense amplifier circuit to have a large gate area, which results in an increase in the sense amplifier circuit area.

5 Therefore, in this embodiment, when the read-out is performed on a memory cell far from the sense amplifier circuit, the voltage variation of the data transfer line is increased to increase the memory cell current to suppress degradation of read-out speed.

10 FIG. 26 is a block diagram illustrating the configuration of a semiconductor memory device according to the fifth embodiment.

 A NAND EEPROM is used again as an example to describe a semiconductor memory device 550 according to the fifth
15 embodiment.

 What is illustrated in FIG. 26 is different from what is illustrated in FIG. 16 in respect of further including a register 471 (first register) connected to the sense amplifier circuit 461 and a register 472 (second register) connected to the sense
20 amplifier circuit 462. A description of matters similar to what are illustrated in FIG. 16 and the like is omitted as appropriate.

 The interconnect resistance value up to each of the memory cell units 4 connected to the odd-numbered (odd index) data transfer line and the even-numbered (even index)
25 data transfer line is measured in advance and stored in the registers 471 and 472.

 These interconnect resistance values are measured in advance by, for example, a test before the product shipment or the like and stored in the registers 471 and 472.

30 What are stored in the registers 471 and 472 are not limited to the interconnect resistance values, but may include the difference (ΔR) obtained by subtracting the series resistance value of the odd-numbered (odd index) data transfer line from the series resistance value of the even-numbered
35 (even index) data transfer line. Furthermore, a voltage near $\Delta R \times I_{\text{cell}}$ may be stored in the registers 471 and 472. Here,

Icell can be measured by, for example, a test before the product shipment or the like.

That is, the registers 471 and 472 store the interconnect resistance value measured in advance for each memory cell unit
5 4 and the like.

The semiconductor memory device 550 according to the fifth embodiment changes the data transfer line voltage during the reading between memory cell units near to the sense amplifier circuits 461 and 462 and memory cell units far from
10 the sense amplifier circuits 461 and 462.

That is, when the read-out is performed on the memory cell, the voltage charging the data transfer line with the sense amplifier circuit 461 and the voltage charging the data transfer line with the sense amplifier circuit 462 vary with the position of
15 the memory cell unit.

In other words, the sense amplifier circuit 461 changes the voltage applied to the data transfer line based on the position of the memory cell unit and the interconnect resistance value stored in the register 471 when performing the read-out
20 on the memory cell. Furthermore, the sense amplifier circuit 462 changes the voltage applied to the data transfer line based on the position of the memory cell unit and the interconnect resistance value stored in the register 472 when performing the read-out on the memory cell.

For example, in the case where the read-out is performed on a memory cell unit far from the sense amplifier circuit, a higher voltage is applied to the data transfer line to pass a larger current flowing through the memory cell than that in the case where the read-out is performed on a memory cell unit
30 near to the sense amplifier circuit. At this time, the current flowing through the memory cell connected to the odd-numbered (odd index) data transfer line and the current flowing through the memory cell connected to the even-numbered (even index) data transfer line are made almost
35 equal to make the read current more constant.

Hereinbelow, although operations during the reading will

be described, operations during the verifying of writing are similar. Therefore, a description of the operations during the writing is omitted.

5 The circuit configuration of the semiconductor memory device 550 is almost similar to the circuit configuration of the semiconductor memory device 530 described above, but this embodiment has a feature in the driving method during the reading.

10 Therefore, a description is given using the case of a memory cell arrangement similar to that illustrated in FIG. 18A as an example.

FIG. 27A is a schematic view illustrating an arrangement of sense amplifier circuits, memory cell units, and the like. What is illustrated in FIG. 27A has a similar arrangement to
15 what is illustrated in FIG. 18A.

The memory cell unit 4c is connected to the sense amplifier circuit 461 and represents the memory cell unit farthest from the sense amplifier circuit 461. The memory cell unit 4b is connected to the sense amplifier circuit 462 and
20 represents the memory cell unit farthest from the sense amplifier circuit 462. "c" represents the data transfer line end farthest from the sense amplifier circuit 461, and "b" represents the data transfer line end farthest from the sense amplifier circuit 462. "a" represents the data transfer line position
25 nearest to the sense amplifier circuit 461, and "d" represents the data transfer line position nearest to the sense amplifier circuit 462.

Here, in FIG. 27A, the odd-numbered (odd number) data transfer lines BL1, BL3, BL5, ..., BL(2n-1) are connected to the
30 sense amplifier circuit 462 drawn on the upper side. Furthermore, the even-numbered (even index) data transfer lines BL2, BL4, BL6, ..., BL2n are connected to the sense amplifier circuit 461 drawn on the lower side.

FIG. 27B is a schematic view illustrating the read-out
35 timing in the case of performing simultaneous read-out when there is a difference in interconnect resistance. That is, the

drawing is a schematic view illustrating the read-out timing in the case of performing simultaneous read-out when there is a difference in interconnect resistance between the odd-numbered (odd index) data transfer line and the even-numbered (even index) data transfer line.

For example, the drawing is a schematic graph illustrating the change in voltage in the memory cell 4c and the memory cell 4d in the case where the sense amplifier circuit 461 and the sense amplifier circuit 462 are simultaneously driven. In this case, the drawing illustrates the voltage and the timing of the data transfer line in the case of performing the read-out on a memory cell nearer to the sense amplifier circuit 462 than to the sense amplifier circuit 461.

As illustrated in FIG. 27B, a voltage is applied to the even-numbered (even index) data transfer line by the sense amplifier circuit 461 from GND to VBL1-e during the period from t_0 to t_1 . On the other hand, a voltage is applied to the odd-numbered (odd index) data transfer line by the sense amplifier circuit 462 from GND to VBL2-o during the period from t_0 to t_1 . That is, the even-numbered (even index) data transfer line and the odd-numbered (odd index) data transfer line are charged from GND to VBL1-e and VBL2-o, respectively, during the period from t_0 to t_1 .

Here, the voltage applied to the even-numbered (even index) data transfer line is taken to be VBL1-e and VBL2-e, and the voltage applied to the odd-numbered (odd index) data transfer line is taken to be VBL1-o and VBL2-o. However, both may be collectively referred to as simply VBL1 and VBL2. VBL1-e and VBL1-o, or VBL2-e and VBL2-o may be the same value or different values.

Here, in the case where the read-out is performed on a memory cell nearer to the sense amplifier circuit 462 than to the sense amplifier circuit 461, the memory cell connected to the odd-numbered (odd index) data transfer line has a short data transfer line length up to the sense amplifier circuit 462 and a low series resistance of the data transfer line. On the

other hand, the memory cell connected to the even-numbered (even index) data transfer line has a long data transfer line length up to the sense amplifier circuit 461 and a higher series resistance of the data transfer line.

5 In this case, in the case where the read-out is performed on a memory cell nearer to the sense amplifier circuit 462 than to the sense amplifier circuit 461, $VBL1-e$ is a value obtained by adding $\Delta R \times I_{cell}$ to $VBL2-o$, where ΔR is the difference obtained by subtracting the series resistance of the
10 odd-numbered (odd index) data transfer line from the series resistance of the even-numbered (even index) data transfer line and I_{cell} is the current flowing through the memory cell during the reading. Thereby, the current passed through the memory cell can be made almost equal between a memory cell placed
15 far from the sense amplifier circuit 461 and a memory cell placed near to the sense amplifier circuit 462.

For example, it is preferable that $VBL1-e$ is set to a voltage that results in a current flowing through a memory cell to which the series resistance of an interconnect corresponding
20 to $3/4$ of the length of the data transfer line is connected, and the voltage is equal between data transfer lines. Here, the difference obtained by subtracting the series resistance of the nearest position of the data transfer line connected to the sense amplifier circuit from the series resistance up to the farthest
25 position of the data transfer line to which the memory cell is connected is denoted by $\Delta R1$. Furthermore, the current flowing through a memory cell to which the series resistance of an interconnect corresponding to $1/4$ of the length of the data transfer line is connected during the reading is denoted by I_{cell} .

30 At this time, $VBL2-o$ may be set to a value obtained by subtracting $(1/2) \times \Delta R1 \times I_{cell}$ from $VBL1-e$. Thereby, the current flowing through a memory cell placed far from the sense amplifier circuit 461 and the current flowing through a memory cell placed near to the sense amplifier circuit 461 can be made
35 more constant. Specifically, in the case where $\Delta R1$ is sufficiently smaller than the series resistance component of the

memory cell other than the resistance of the data transfer line, the interconnect resistance variation in the position on the data transfer line according to the arrangement position of the memory cell (being occasionally a memory cell block to which
5 memory cells belong) in the memory cell array 1 can be made lowest, or $\pm(1/4) \times \Delta R1 \times I_{\text{cell}}$ or less.

Furthermore, in what is illustrated in FIGS. 18A and 18B, the voltage of the data transfer line at the time of the reading is set equal between the even-numbered (even index) data
10 transfer line and the odd-numbered (odd index) data transfer line. However, by setting VBL1-e to a voltage higher than VBL2-o by an amount, for example, between 0.1 V and 1 V as in the case of this embodiment, the difference in the current
15 flowing through the memory cell between the memory cell 4c disposed in a position far from the sense amplifier circuit 461 and the memory cell 4d disposed in a position near to the sense amplifier circuit 462 can be reduced.

Furthermore, by this way, the current flowing through the memory cell connected to the odd-numbered (odd index) data
20 transfer line can be made small while the minimum current flowing through the memory cell is maintained, as compared to the case where the voltage of VBL1-e is applied to both of the even-numbered (even index) data transfer line and the odd-numbered (odd index) data transfer line. Accordingly, the
25 power consumption of the semiconductor memory device can be reduced more, and a decrease of the reliability of the interconnect due to a large current flowing through the odd-numbered (odd index) data transfer line can be suppressed.

30 FIG. 27C is a schematic graph illustrating the change in voltage in the memory cell 4a and the memory cell 4b in the case where the sense amplifier circuit 461 and the sense amplifier circuit 462 are driven simultaneously. That is, the drawing illustrates the voltage and the timing of the data
35 transfer line in the case of performing the read-out on a memory cell nearer to the sense amplifier circuit 461 than to

the sense amplifier circuit 462.

As illustrated in FIG. 27C, a voltage is applied to the even-numbered (even index) data transfer line by the sense amplifier circuit 461 from GND to VBL2-e during the period from t0 to t1. On the other hand, a voltage is applied to the odd-numbered (odd index) data transfer line by the sense amplifier circuit 462 from GND to VBL1-o during the period from t0 to t1. That is, the even-numbered (even index) data transfer line and the odd-numbered (odd index) data transfer line are charged from GND to VBL1-o and VBL2-e, respectively, during the period from t0 to t1.

Here, in the case where the read-out is performed on a memory cell nearer to the sense amplifier circuit 461 than to the sense amplifier circuit 462, the memory cell connected to the even-numbered (even index) data transfer line has a short data transfer line length up to the sense amplifier circuit 461 and a low series resistance of the data transfer line. On the other hand, the memory cell connected to the odd-numbered (odd index) data transfer line has a long data transfer line length up to the sense amplifier circuit 462 and a higher series resistance of the data transfer line.

Here, in the case where the read-out is performed on a memory cell nearer to the sense amplifier circuit 461 than to the sense amplifier circuit 462, VBL1-o is a value obtained by adding $\Delta R \times I_{\text{cell}}$ to VBL2-e, where ΔR is the difference obtained by subtracting the series resistance of the even-numbered (even index) data transfer line from the series resistance of the odd-numbered (odd index) data transfer line and I_{cell} is the current flowing through the memory cell during the reading. To derive ΔR , the series resistance of the data transfer line is taken as the resistance between the sense amplifier and the memory cell. Thereby, the current passed through the memory cell can be made almost equal between a memory cell placed far from the sense amplifier circuit 462 and a memory cell placed near to the sense amplifier circuit 461.

Furthermore, by this way, the current flowing through the

memory cell connected to the even-numbered (even index) data transfer line can be made small while the minimum current flowing through the memory cell is maintained, as compared to the case where the voltage of VBL1-o is applied to both of the even-numbered (even index) data transfer line and the odd-numbered (odd index) data transfer line. Accordingly, the power consumption of the semiconductor memory device can be reduced more, and a decrease of the reliability of the interconnect due to a large current flowing through the even-numbered (even index) data transfer line can be suppressed.

Next, as illustrated in FIGS. 27B and 27C, the voltage of the data transfer line is kept constant between t_1 and t_2 . That is, a period (from t_1 to t_2) of keeping VBL1 and VBL2 constant is provided. Here, when the read-out of the memory cell is performed, for the memory cell to which current terminals are connected in series to the read-out memory cell, V_{read} , which is an electric potential higher than the maximum threshold voltage of the memory cell is applied to the data control line connected to the control gate.

In this case, assuming that the voltage of the data control line involved in the reading is V_{ref} , since the electric potential of a data control line adjacent thereto is V_{read} , the voltage of the data control line involved in the reading fluctuates from the voltage V_{ref} due to capacitive coupling. In order to prevent misreading in the case of exceeding the threshold voltage due to the voltage fluctuation, the voltage of the data transfer line is kept constant for the period from t_1 to t_2 , which is longer than the time constant for stabilizing the voltage fluctuation by the capacitive coupling.

Here, for example, during the period from t_0 to t_1 , the voltage of the data control line involved in the reading is taken to be, for example, V_{ref} , the voltages of the other data control lines are taken to be V_{read} , and the selection transistor on the source line side and the selection transistor on the drain side are changed from the cutoff state to the conduction state to

increase the electric potential of the data transfer line. Consequently, the NAND string involved in the reading is turned into the conduction state to increase the electric potential, and thereby the voltage of the data control line involved in the reading can be increased earlier than the voltages of the other data control lines. Therefore, a voltage increase due to the capacitive coupling of the channel portion of the NAND string caused by the voltage increases of the other data control lines to V_{read} can be prevented.

Next, during the period from t_1 to t_2 , the selection transistor on the source line side or the selection transistor on the drain side is changed from the conduction state to the cutoff state.

Subsequently, during the period from t_2 to t_3 , the charges stored in the data transfer line are discharged by, for example, changing the selection transistor on the source line side or the selection transistor on the drain side from the cutoff state to the conduction state.

At this time, the magnitude of the charge of the memory cell is evaluated with the sense amplifier circuit 461 and the sense amplifier circuit 462. For example, the magnitude of the charge of the memory cell is evaluated by measuring the magnitude of the electric potential of the data transfer line at the end connected to the sense amplifier circuit 461 with the sense amplifier circuit 461 by comparing with a reference value (for example, V_{BL1_th} illustrated in FIG. 27B). Furthermore, the magnitude of the charge of the memory cell is evaluated by measuring the magnitude of the electric potential of the data transfer line at the end connected to the sense amplifier circuit 462 with the sense amplifier circuit 462 by comparing with a reference value (for example, V_{BL2_th} illustrated in FIG. 27B).

Here, in the case where the logical value of the memory cell is "0" in FIG. 27B, that is, in the case of the write state (the threshold voltage of the memory cell being larger than V_{ref}), since the evaluation is made through the V_{ref} value lower than the write threshold voltage, the memory cell current does not

flow and the electric potential of the even-numbered (even index) data transfer line is kept VBL1-e. Furthermore, the electric potential of the odd-numbered (odd index) data transfer line is kept VBL2-o.

5 On the other hand, in the case where the logical value of the memory cell is "1" in FIG. 27B, that is, in the case of, for example, the erase state (the threshold voltage of the memory cell being smaller than V_{ref}), since the evaluation is made through the V_{ref} value higher than the erase threshold voltage, the memory cell current flows and the electric potentials of the even-numbered (even index) data transfer line and the odd-numbered (odd index) data transfer line decrease.

10 The above description is based on the case where the logical state of the memory cell connected to the even-numbered (even index) data transfer line and the logical state of the memory cell connected to the odd-numbered (odd index) data transfer line are the same. However, it goes without saying that there is a case where the logical state of the memory cell connected to the even-numbered (even index) data transfer line and the logical state of the memory cell connected to the odd-numbered (odd index) data transfer line are different.

15 In the case illustrated in FIG. 27C, the magnitude of the charge of the memory cell is evaluated by measuring the magnitude of the electric potential of the data transfer line at the end connected to the sense amplifier circuit 462 with the sense amplifier circuit 462 by comparing with a reference value (for example, VBL1_th illustrated in FIG. 27C). Furthermore, the magnitude of the charge of the memory cell is evaluated by measuring the magnitude of the electric potential of the data transfer line at the end connected to the sense amplifier circuit 461 with the sense amplifier circuit 461 by comparing with a reference value (for example, VBL2_th illustrated in FIG. 27C).

20 Here, in the case where the logical value of the memory cell is "0" in FIG. 27C, that is, in the case of the write state (the threshold voltage of the memory cell being larger than V_{ref}),

since the evaluation is made through the V_{ref} value lower than the write threshold voltage, the memory cell current does not flow and the electric potential of the even-numbered (even index) data transfer line is kept VBL2-e. Furthermore, the
 5 electric potential of the odd-numbered (odd index) data transfer line is kept VBL1-o.

On the other hand, in the case where the logical value of the memory cell is "1" in FIG. 27C, that is, in the case of, for example, the erase state (the threshold voltage of the memory
 10 cell being smaller than V_{ref}), since the evaluation is made through the V_{ref} value higher than the erase threshold voltage, the memory cell current flows and the electric potentials of the even-numbered (even index) data transfer line and the odd-numbered (odd index) data transfer line decrease.

Here, as described above, since the difference in cell current I_{cell} between memory cells far from the sense amplifier circuits 461 and 462 and memory cells near to the sense amplifier circuits 461 and 462 can be reduced, the difference between VBL1-o and VBL1-th of the data transfer line and the
 15 difference between VBL2-e and VBL2-th can be made small. Therefore, the time between t_2 and t_3 (the time of measuring the memory cell current) can be made almost equal.

The magnitude of the charge of the memory cell may be evaluated by measuring the current flowing through the data
 25 transfer line with the sense amplifier circuit 461 and the sense amplifier circuit 462. In this case, even if the data transfer line lengths from the sense amplifier circuit are different, the current flowing through the memory cell can be made uniform between the even-numbered (even index) data transfer line and the odd-numbered (odd index) data transfer line. Therefore,
 30 the time necessary for evaluating the magnitude of the charge of the memory cell with the sense amplifier circuit 461 and the sense amplifier circuit 462, which corresponds to the time between t_2 and t_3 , can be made more uniform.

35 In this case, the voltage applied to the bit line contact of the memory cell unit can be made more uniform between the

even-numbered (even index) data transfer line and the odd-numbered (odd index) data transfer line. Consequently, the threshold voltage variation (read disturbance) due to the potential difference between the voltage V_{read} during reading and the channel can be made uniform between the even-numbered (even index) data transfer line and the odd-numbered (odd index) data transfer line to provide a semiconductor memory device with higher reliability. Furthermore, the threshold voltage variation (read disturbance) due to the potential difference between the voltage V_{read} and the channel can be made uniform between a memory cell far from the sense amplifier circuit 463 and a memory cell near to the sense amplifier circuit 463 to provide a semiconductor memory device with higher reliability.

The foregoing takes the two values of the erase state ("1") and the write state ("0") as an example, but as a matter of course, this embodiment can be applied also to the case of multiple values. In such a case, for example, it is possible to provide the threshold of a state adjacent to an erase state and a write state.

Here, in the case where the sense amplifier circuit 461 and the sense amplifier circuit 462 are simultaneously driven with the same timing (the case illustrated in FIGS. 18A and 18B), it is necessary to wait until the timing of t_3 as the time of discharging the charges stored in the data transfer line in order to perform the read-out with the same timing between the memory cell connected to the even-numbered (even index) data transfer line and the memory cell connected to the odd-numbered (odd index) data transfer line. Then, during the period from t_3 to t_4 , the charges stored in the data transfer line are further discharged into the GND potential to prepare the next reading.

In this embodiment, during the reading or verify reading, the voltage applied to the data transfer line is changed with the position in the longitudinal direction of the data transfer line (the distance from the sense amplifier circuit) of each memory

cell unit. Therefore, the current flowing through each memory cell can be made more uniform.

Here, methods for changing the voltage applied to the data transfer line include, for example, a method in which
5 switching is performed so that such voltage application as is illustrated in FIG. 27B may be performed on the first memory cell block 1a nearer to the sense amplifier circuit 462 than to the sense amplifier circuit 461 and such voltage application as is illustrated in FIG. 27C may be performed on the second
10 memory cell block 1b nearer to the sense amplifier circuit 461 than to the sense amplifier circuit 462.

In this case, a circuit that applies at least two kinds of voltages to the data transfer line or a circuit that changes the voltage applied to the data transfer line in accordance with the
15 position of the memory cell unit may be added to the sense amplifier circuit 461 and the sense amplifier circuit 462.

Here, since the interconnect resistance value measured in advance for each memory cell unit 4 is stored in the registers 471 and 472, at least two kinds of voltages may be switched or
20 the voltage applied to the data transfer line may be changed based on the interconnect resistance value stored.

Although this embodiment illustrates the case where a voltage is applied to two kinds of data transfer lines, a voltage may be applied to two or more kinds of data transfer lines as
25 below. Thereby, the effects of this embodiment can be made more effective.

For example, in the case where the difference between the length of the even-numbered (even index) data transfer line and the length of the odd-numbered (odd index) data transfer
30 line is small, that is, the difference between the distance from the sense amplifier circuit 461 to the memory cell unit and the distance from the sense amplifier circuit 462 to the memory cell unit is small, a voltage intermediate between VBL1 and VBL2 may be applied to the even-numbered (even index) data
35 transfer line and the odd-numbered (odd index) data transfer line. Thereby, the current flowing through the memory cell can

be made more constant.

Furthermore, applying a voltage intermediate between VBL1 and VBL2 allows the current of the memory cell to be made small as compared to the case where the voltage of VBL1 is applied to both of the even-numbered (even index) data transfer line and the odd-numbered (odd index) data transfer line.

Therefore, the power consumption of the semiconductor memory device can be reduced more, and a degradation of the reliability of the interconnect due to a large current flowing through the data transfer line can be suppressed.

According to this embodiment, in the case where the read-out is performed simultaneously and the writing is performed simultaneously on the memory cell units connected to either the even-numbered (even index) data transfer lines or the odd-numbered (odd index) data transfer lines, the current Icell flowing through the memory cell can be kept more constant regardless of the interconnect length of the data transfer line. Furthermore, the time necessary for measuring the current of the memory cell can be made more uniform to a certain value.

Here, as illustrated in FIG. 25, the variation width of the threshold voltage due to the subthreshold coefficient increases as the current flowing through the memory cell decreases. In particular, this is significant in a memory cell belonging to a memory cell block located far from the sense amplifier circuit. According to this embodiment, since the minimum value of the current flowing through the memory cell can be made large, the sense current of the sense amplifier circuit can be made constant and the variation width of the threshold voltage can be made smaller.

In this case, when the sense current of the sense amplifier circuit is not constant as illustrated in FIG. 25, the current and the threshold voltage have a positive dependence due to the gradient of the subthreshold characteristics, which makes the threshold voltage variation larger. Therefore, it is

clear that the variation in threshold voltage can be made smaller by making constant the value of the current flowing through the memory cell in the erase state ("1").

On the other hand, when it is attempted to make large
5 the voltage amplitude ΔV of the data transfer line end connected to the sense amplifier circuit, a sufficient memory cell current I_{cell} cannot be obtained in the memory cell farthest from the sense amplifier circuit because of a high interconnect resistance of the data transfer line.

10 Furthermore, what influence the time until the current of the data transfer line is stabilized include a component proportional to (Data transfer line capacitance) $\times$ ($\Delta V/I_{\text{cell}}$), other than the delay corresponding to the time constant of the product of (Capacitance of data transfer line) $\times$ (Resistance of
15 data transfer line), due to capacitive coupling between data transfer lines. Accordingly, the delay increases as the voltage amplitude ΔV of the data transfer line end connected to the sense amplifier circuit increases.

According to this embodiment, since the minimum value
20 of the current flowing through the memory cell can be made large, the delay time proportional to (Data transfer line capacitance) $\times$ ($\Delta V/I_{\text{cell}}$) can be made short. In the case where the voltage amplitude ΔV of the data transfer line end is small, a sense amplifier circuit with a high sense amplifier
25 sensitivity is needed. To obtain a sense amplifier circuit with a high sense amplifier sensitivity, for example, it is necessary for the transistor used for the input of the sense amplifier circuit to have a large gate area, which results in an increase in the sense amplifier circuit area.

30 According to this embodiment, since the difference between the maximum value and the minimum value of the memory cell current I_{cell} at the time of the reading can be made smaller, the area increase of the sense amplifier circuit can be prevented. Therefore, this embodiment allows the
35 circuit to normally operate even if the circuit operation margin is reduced by the difference of the delay time between

interconnects, enabling the speeding up of the circuit operation. Therefore, faster reading and verify reading can be implemented.

Next, a variation of the semiconductor memory device according to the fifth embodiment will now be illustrated.

FIG. 28A is a schematic circuit diagram illustrating a layout of the memory cell array and the data transfer line. FIG. 28B is a schematic graph illustrating the voltage of the data transfer line at the time of the reading.

The layout of the memory cell array and the data transfer line in this variation is similar to that illustrated in FIG. 22. Therefore, matters similar to what are illustrated in FIG. 22 are omitted as appropriate.

As illustrated in FIG. 28A, in a semiconductor memory device 551, the sense amplifier circuit 461 and the sense amplifier circuit 462 are not provided to face each other across the memory cell array 1, but disposed collectively on one side of the memory cell array 1.

That is, the sense amplifier circuit 461 and the sense amplifier circuit 462 are collectively disposed.

That is, in this variation, the sense amplifier circuit 461 connected to one end of the even-numbered (even index) data transfer line and the sense amplifier circuit 462 connected to one end of the odd-numbered (odd index) data transfer line are collectively disposed on the same side of the memory cell array 1. Therefore, a peripheral circuit and a power source interconnect can be disposed concentratedly. Furthermore, by configuring the sense amplifier circuit 461 and the sense amplifier circuit 462 collectively in this way, the lengths of the data transfer lines connected to each of the sense amplifier circuit 461 and the sense amplifier circuit 462 can be made almost equal. Therefore, there is also an effect in which the fluctuations between the data transfer lines for the memory cells connected to each of the sense amplifier circuit 461 and the sense amplifier circuit 462 can be made small.

Furthermore, unlike an embodiment in which the sense

amplifier circuits are formed on both sides of the memory cell array, in this variation, the sense amplifier circuits are formed on one side of the memory cell. Thereby, array noise from an adjacent data transfer line during the reading can be made smaller. This is because the charge voltage of the data transfer line, which varies with the position of the memory cell block, increases as the read memory cell block becomes farther from the sense amplifier circuit. Therefore, in the case where the logical value of the memory cell is "0" (the threshold voltage of the memory cell being larger than V_{ref}) at the time of the reading, the data transfer line voltage of a memory cell block far from the sense amplifier circuit is V_{BL1} higher than V_{BL2} .

Therefore, in the case where the sense amplifier circuits are formed on both sides of the memory cell array, the voltage of a data transfer line adjacent to the data transfer line connected to a memory cell near to the sense amplifier circuit is V_{BL1} higher than V_{BL2} . Accordingly, in the case where the logical value of the memory cell is "0", the problem is caused that the electric potential of the data transfer line connected to a memory cell for which the current is measured increases more due to the capacitive coupling from the channel of the adjacent memory cell.

Furthermore, there is a case where, in regard to the voltages of two adjacent data transfer lines, the voltage is V_{BL2} in the data transfer line connected to a memory cell with a logical value of memory cell of "1", the logical value of a memory cell (referred to as an "adjacent memory cell") adjacent to this memory cell is "0", and the data transfer line connected to the adjacent memory cell is V_{BL1} higher than V_{BL2} . Accordingly, it is difficult to suppress the leak current occurring between the contacts connected to the respective data transfer lines.

On the other hand, in the case where the sense amplifiers are formed on one side of the memory cell array, when memory cells connected to the same data selection line are read, the voltages of adjacent data transfer lines can be

made almost uniform. Consequently, the leak current between the contacts between the data transfer lines can be suppressed more.

Also in this embodiment, when performing the read-out
5 on the memory cell, the sense amplifier circuit 461 changes the voltage applied to the data transfer line based on the position of the memory cell unit and the interconnect resistance value stored in the register 471. Furthermore, when performing the read-out on the memory cell, the sense amplifier circuit 462
10 changes the voltage applied to the data transfer line based on the position of the memory cell unit and the interconnect resistance value stored in the register 472. Changing the applied voltage is similar to that described above, and a description thereof is therefore omitted as appropriate.

15 FIG. 28B illustrates the voltage and the timing of the data transfer line in the case where the sense amplifier circuit 461 and the sense amplifier circuit 462 are simultaneously driven to perform the read-out on the memory cell.

Here, for example, the data transfer line voltage in the
20 case of the memory cell unit provided in the first memory cell block 1a located far from the sense amplifier circuit 461 and the sense amplifier circuit 462 is denoted by VBL1. Furthermore, for example, the data transfer line voltage in the case of the memory cell unit provided in the second memory cell block 1b
25 located near to the sense amplifier circuit 461 and the sense amplifier circuit 462 is denoted by VBL2 lower than VBL1.

In this case, for example, it is preferable that VBL1 is set to a voltage that results in a current flowing through a memory cell to which the series resistance of an interconnect
30 corresponding to 3/4 of the length of the data transfer line is connected, and the voltage is equal between data transfer lines. Here, the difference obtained by subtracting the series resistance of the nearest position of the data transfer line connected to the sense amplifier circuit from the series
35 resistance up to the farthest position of the data transfer line to which the memory cell is connected is denoted by $\Delta R1$.

Furthermore, the current flowing through a memory cell to which the series resistance of an interconnect corresponding to $1/4$ of the length of the data transfer line is connected during the reading is denoted by I_{cell} .

5 At this time, $VBL2$ may be set to a value obtained by subtracting $(1/2) \times \Delta R1 \times I_{cell}$ from $VBL1$. Thereby, the current flowing through a memory cell disposed in a position far from the sense amplifier circuit 461 and the current flowing through a memory cell disposed in a position near to the sense
10 amplifier circuit 461 can be made more constant. Specifically, in the case where $\Delta R1$ is sufficiently smaller than the series resistance component of the memory cell other than the resistance of the data transfer line, the interconnect resistance fluctuation of the position on the data transfer line according to
15 the arrangement position of the memory cell (being occasionally a memory cell block to which memory cells belong) in the memory cell array 1 can be made lowest, or $\pm(1/4) \times \Delta R1 \times I_{cell}$ or less.

 Here, $VBL1$ is a value obtained by adding $\Delta R \times I_{cell}$ to
20 $VBL2$, where ΔR is the difference obtained by subtracting the series resistance value of the odd-numbered (odd index) data transfer line from the series resistance value of the even-numbered (even index) data transfer line and I_{cell} is the current flowing through the memory cell during the reading. To
25 derive ΔR , the series resistance of the data transfer line is taken as the resistance between the sense amplifier and the memory cell. Thereby, the difference in the current flowing through the memory cell can be made smaller between a memory cell disposed in a position far from the sense amplifier
30 circuit 461 and a memory cell disposed in a position near to the sense amplifier circuit 462, and the current can be made more constant. Therefore, this is preferable.

 By setting $VBL1$ to a voltage higher than $VBL2$ by an amount, for example, between 0.1 V and 1 V as in the case of
35 this variation, the difference in the current flowing through the memory cell between the memory cell 4c disposed in a position

far from the sense amplifier circuit 461 and the memory cell 4b disposed in a position near to the sense amplifier circuit 462 can be reduced.

Furthermore, by applying VBL2 lower than VBL1, the
5 current flowing through a memory cell near to the sense amplifier circuit 461 and the sense amplifier circuit 462 can be made small as compared to the case where the voltage of VBL1 is applied constantly to the data transfer line. Accordingly, the power consumption of the semiconductor memory device can be
10 reduced more, and a degradation of the reliability of the interconnect due to a large current flowing through the data transfer line can be suppressed.

Furthermore, since the difference in cell current I_{cell} between memory cells far from the sense amplifier circuits 461
15 and 462 and memory cells near to the sense amplifier circuits 461 and 462 can be reduced, the difference between VBL1 and VBL1_th of the data transfer line and the difference between VBL2 and VBL2_th can be made small. Therefore, the time between t_2 and t_3 (the time of measuring the memory cell
20 current) can be made almost equal.

The magnitude of the charge of the memory cell may be evaluated by measuring the current flowing through the data transfer line with the sense amplifier circuit 461 and the sense amplifier circuit 462. In this case, even if the position of the
25 memory cell unit connected to the data transfer line changes, the current flowing through the memory cell can be made uniform. Therefore, the time necessary for evaluating the magnitude of the charge of the memory cell with the sense amplifier circuit 461 and the sense amplifier circuit 462, which
30 corresponds to the time between t_2 and t_3 , can be made more uniform.

In this case, even if the position of the memory cell unit connected to the data transfer line changes, the voltage applied to the bit line contact of the memory cell unit can be made
35 more uniform. Consequently, the threshold voltage fluctuation (read disturbance) due to the potential difference between the

voltage V_{read} at the time of the reading and the channel can be made uniform between the even-numbered (even index) data transfer line and the odd-numbered (odd index) data transfer line to provide a semiconductor memory device with higher reliability. Furthermore, the threshold voltage fluctuation (read disturbance) due to the potential difference between the voltage V_{read} at the time of the reading and the channel can be made uniform between a memory cell far from the sense amplifier circuit 463 and a memory cell near to the sense amplifier circuit 463 to provide a semiconductor memory device with higher reliability.

Sixth embodiment

Next, a semiconductor memory device according to a sixth embodiment will now be described.

A semiconductor memory device 560 according to the sixth embodiment has a configuration almost similar to the semiconductor memory device 540 according to the fourth embodiment described above. However, there is a difference in that the data transfer line voltage at the time of the reading is changed between a memory cell unit near to the sense amplifier circuit 463 and a memory cell unit far from the sense amplifier circuit 463.

That is, when the reading of the memory cell is performed, the voltage charging the data transfer line with the sense amplifier circuit 463 varies with the position of the memory cell unit.

In other words, there is a difference in that the sense amplifier circuit 463 changes the voltage applied to the data transfer line based on the position of the memory cell unit and the interconnect resistance value stored in a register 473 when the read-out is performed on the memory cell.

In this case, in the case where the read-out is performed on a memory cell far from the sense amplifier circuit 463, a higher voltage is applied to the data transfer line to increase the current flowing through the memory cell than in the case

where the read-out is performed on a memory cell near to the sense amplifier circuit 463. Therefore, the current flowing through the memory cell can be made more constant regardless of the position of the memory cell unit.

5 Hereinbelow, operations during the reading will be described, but operations during the verifying of writing are similar. Therefore, a description of the operations during the writing is omitted. Furthermore, since the semiconductor memory device 560 according to this embodiment has a
10 configuration similar to the semiconductor memory device 540 according to the fourth embodiment described above, a description of matters similar to what are illustrated in FIG. 24 and the like is omitted as appropriate.

FIG. 29A is a schematic circuit diagram illustrating a
15 layout of the memory cell array and the data transfer line. FIG. 29B is a schematic graph illustrating the voltage of the data transfer line at the time of the reading.

As illustrated in FIG. 29A, in this embodiment, the sense amplifier circuit 463 is collectively disposed on one side of one
20 end of the data transfer line. The odd-numbered (odd index) data transfer line is connected to the sense amplifier circuit 463 via the current terminal of the transistor Q1, and the even-numbered (even index) data transfer line is connected to the sense amplifier circuit 463 via the current terminal of the
25 transistor Q2.

The register 473 is connected to the sense amplifier circuit 463.

The interconnect resistance value up to each of the memory cell units 4 connected to the odd-numbered (odd
30 index) data transfer lines and the even-numbered (even index) data transfer lines is measured in advance and stored in the register 473.

That is, the register 473 stores the interconnect resistance value measured in advance for each memory cell unit
35 4.

In this embodiment, since the sense amplifier circuit 463

is collectively disposed on the same one side of the memory cell array, a peripheral circuit and a power source interconnect can be disposed concentratedly. In this case, by disposing the sense amplifier circuit 463 in this way, the lengths of the data transfer lines connected to the sense amplifier circuit 463 can be made equal. Therefore, there is an effect in which the fluctuation of the current flowing through the memory cell connected to the sense amplifier circuit 463 between data transfer lines can be made small.

10 FIG. 29B illustrates the voltage and the timing of the data transfer line in the case where the sense amplifier circuit 463 is driven to perform the read-out on the memory cell.

 Here, for example, the data transfer line voltage in the case of the memory cell unit provided in the first memory cell block 1a located far from the sense amplifier circuit 463 is denoted by VBL1. Furthermore, for example, the data transfer line voltage in the case of the memory cell unit provided in the second memory cell block 1b located near to the sense amplifier circuit 463 is denoted by VBL2 lower than VBL1.

20 In this case, for example, VBL1 is set to a voltage that results in a current flowing through a memory cell to which the series resistance of an interconnect corresponding to $3/4$ of the length of the data transfer line is connected, and VBL2 is set to a voltage that results in a current flowing through a memory cell to which the series resistance of an interconnect corresponding to $1/4$ of the length of the data transfer line is connected. VBL1 and VBL2 are set so that the currents flowing through these memory cells may become equal. Thereby, the fluctuation of current between memory cells can be suppressed.

30 By setting VBL1 to a voltage higher than VBL2 by an amount, for example, between 0.1 V and 1 V as in the case of this embodiment, the difference in the current flowing through the memory cell between the memory cell 4c disposed in a position far from the sense amplifier circuit 463 and the memory cell 4b disposed in a position near to the sense amplifier circuit 463 can be reduced.

Furthermore, by applying VBL2 lower than VBL1, the current flowing through a memory cell near to the sense amplifier circuit 463 can be made small as compared to the case where the voltage of VBL1 is applied constantly to the data transfer line. Accordingly, the power consumption of the semiconductor memory device can be reduced more, and a degradation of the reliability of the interconnect due to a large current flowing through the data transfer line can be suppressed.

Furthermore, since the difference in cell current I_{cell} between a memory cell far from the sense amplifier circuit 463 and a memory cell near to the sense amplifier circuit 463 can be reduced, the difference between VBL1 and VBL1_{th} of the data transfer line and the difference between VBL2 and VBL2_{th} can be made small. Therefore, the time between t_2 and t_3 (the time of measuring the memory cell current) can be made almost equal.

The magnitude of the charge of the memory cell may be evaluated by measuring the current flowing through the data transfer line with the sense amplifier circuit 463. In this case, even if the position of the memory cell unit connected to the data transfer line changes, the current flowing through the memory cell can be made uniform. Therefore, the time necessary for evaluating the magnitude of the charge of the memory cell with the sense amplifier circuit 463, which corresponds to the time between t_2 and t_3 , can be made more uniform.

In this case, even if the position of the memory cell unit connected to the data transfer line changes, the voltage applied to the bit line contact of the memory cell unit can be made more uniform. Consequently, the threshold voltage variation (read disturbance) due to the potential difference between the voltage V_{read} at the time of the reading and the channel can be made uniform between a memory cell far from the sense amplifier circuit 463 and a memory cell near to the sense amplifier circuit 463 to provide a semiconductor memory device

with higher reliability.

In the specification of this application, "perpendicular" and "parallel" refer to not only strictly perpendicular and strictly parallel but also include, for example, the fluctuation due to manufacturing processes, etc. It is sufficient to be substantially perpendicular and substantially parallel.

Hereinabove, exemplary embodiments of the invention are described with reference to specific examples. However, the invention is not limited to these specific examples. For example, one skilled in the art may appropriately select specific configurations of components included in semiconductor memory devices such as first to fourth interconnects, low resistance interconnects, high resistance interconnects, first to sixth data transfer interconnects, memory cells, memory cell units, memory cell blocks, first and second regions, first and second insulating regions, data transfer line reroute units, reroute interconnects, reroute contacts from, and the like known art and similarly practice the invention. Such practice is included in the scope of the invention to the extent that similar effects thereto are obtained.

Further, any two or more components of the specific examples may be combined within the extent of technical feasibility; and such combinations are included in the scope of the invention to the extent that the purport of the invention is included.

Furthermore, although an example in which the register 472 is connected to the sense amplifier circuit 462 is illustrated in the fifth embodiment, they may not be directly connected. For example, a circuit configuration is possible in which the register 472 is electrically connected to the sense amplifier circuit 462 via a digital/analog conversion circuit and the data transfer line voltage can be adjusted by the output of the analog conversion circuit.

Furthermore, although an example in which the register 471 is connected to the sense amplifier circuit 461 is illustrated, they may not be directly connected. For example, a circuit

configuration is possible in which the register 471 is electrically connected to the sense amplifier circuit 461 via a digital/analog conversion circuit and the data transfer line voltage can be adjusted by the output of the analog conversion circuit.

5 Moreover, the register 471 and the register 472 may not store the interconnect resistance value itself but encode and store the corresponding digital data.

 Furthermore, although an example in which the register 473 is connected to the sense amplifier circuit 463 is illustrated
10 in the sixth embodiment, they may not be directly connected. For example, a circuit configuration is possible in which the register 473 is electrically connected to the sense amplifier circuit 463 via a digital/analog conversion circuit and the data transfer line voltage can be adjusted by the output of the
15 analog conversion circuit.

 Moreover, the register 473 may not store the interconnect resistance value itself but encode and store the corresponding digital data.

 While certain embodiments have been described, these
20 embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments
25 described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modification as would fall within the scope and spirit of the inventions.

CLAIMS:

1. A semiconductor memory device comprising:

a memory cell array including:

5 a plurality of first memory cell units, each of the plurality of first memory cell units including a plurality of memory cells;

a plurality of second memory cell units, each of the plurality of second memory cell units including a plurality of memory cells;

10 a plurality of first interconnects, each of the plurality of first interconnects extending in a first direction and being connected to one end of each of the first memory cell units; and

15 a plurality of second interconnects, each of the plurality of second interconnects extending in the first direction and being connected to one end of each of the second memory cell units, heights of upper surfaces of the second interconnects being equal to heights of upper surfaces of the first interconnects;

a first sense amplifier circuit connected to the plurality of first interconnects; and

20 a second sense amplifier circuit connected to the plurality of second interconnects,

the plurality of first interconnects and the plurality of second interconnects formed adjacent to each other being formed of a structure in which a plurality of pairs are repeated, and

25 at least one of a width of each of the plurality of second interconnects along a second direction perpendicular to the first direction and a thickness of each of the plurality of second interconnects along a third direction perpendicular to the first direction and the second direction being set smaller

than each of the plurality of first interconnects, and the first sense amplifier circuit and the second sense amplifier circuit being disposed to face each other across the memory cell array.

5 2. The device according to claim 1, wherein read time of the plurality of memory cells included in the plurality of first memory cell units is shorter than read time of the plurality of memory cells included in the plurality of second memory cell units, and a mode of outputting data of the plurality of memory cells included in the plurality of first memory cell units earlier than data of the plurality
10 of memory cells included in the plurality of second memory cell units is provided.

3. The device according to claim 1, wherein variance of widths of insulating films between the plurality of first interconnects and the plurality of second
15 interconnects is smaller than variance of widths of upper surface of the plurality of first interconnects.

4. A semiconductor memory device comprising:
a memory cell array including:

20 a plurality of first memory cell units, each of the plurality of first memory cell units including a plurality of memory cells;

 a plurality of second memory cell units, each of the plurality of second memory cell units including a plurality of memory cells; a plurality of first interconnects, each of the plurality of first interconnects extending
25 in a first direction and being connected to one end of each of the first memory cell units; and

a plurality of second interconnects, each of the plurality of second interconnects extending in the first direction and being connected to one end of each of the second memory cell units, heights of upper surfaces of the second interconnects being equal to heights of upper surfaces of the first interconnects;

5

a first sense amplifier circuit connected to the plurality of first interconnects; and

a second sense amplifier circuit connected to the plurality of second interconnects,

10

the plurality of first interconnects and the plurality of second interconnects formed adjacent to each other being formed of a structure in which a plurality of pairs are repeated,

15

at least one of a width of each of the plurality of second interconnects along a second direction perpendicular to the first direction and a thickness of each of the plurality of second interconnects along a third direction perpendicular to the first direction and the second direction being set smaller than each of the plurality of first interconnects,

the first sense amplifier circuit and the second sense amplifier circuit being formed on one side of the memory cell array,

20

the first sense amplifier circuit being formed nearer to the memory cell array than the second sense amplifier circuit, and

data of the plurality of memory cells included in the plurality of first memory cell units being output earlier than data of the plurality of memory cells included in the plurality of second memory cell units.

25

5. The device according to claim 4, wherein variance of widths of insulating films between the plurality of first interconnects and the plurality of second

interconnects is smaller than variance of widths of upper surface of the plurality of first interconnects.

6. A semiconductor memory device comprising:

5 a memory cell array including:

a plurality of first memory cell units, each of the plurality of first memory cell units including a plurality of memory cells;

a plurality of second memory cell units, each of the plurality of second memory cell units including a plurality of memory cells;

10 a plurality of first interconnects, each of the plurality of first interconnects extending in a first direction and being connected to one end of each of the first memory cell units; and

a plurality of second interconnects, each of the plurality of second interconnects extending in the first direction and being connected to one end of each of the second memory cell units,

15 heights of upper surfaces of the second interconnects being equal to heights of upper surfaces of the interconnects, and

the plurality of first interconnects and the plurality of second interconnects formed adjacent to each other being formed of a structure in which a plurality of pairs are repeated,

20 a sense amplifier circuit connected to the plurality of first interconnects and the plurality of second interconnects; and

a switching circuit configured to switch between a connection of a sense amplifier circuit with the plurality of first interconnects and a connection of the sense amplifier circuit with the plurality of second interconnects;

25 at least one of a width of each of the plurality of second interconnects along a second direction perpendicular to the first direction and a thickness of

each of the plurality of second interconnects along a third direction perpendicular to the first direction and the second direction being set smaller than each of the plurality of first interconnects, and

a control circuit outputting data of the plurality of memory cells included
5 in the plurality of first memory cell units earlier than data of the plurality of memory cells included in the plurality of second memory cell units.

7. The device according to claim 6, wherein variance of widths of insulating films between the plurality of first interconnects and the plurality of second
10 interconnects is smaller than variance of widths of upper surface of the plurality of first interconnects.

8. The device according to claim 1, wherein:

a first voltage charging a first interconnect with the first sense amplifier
15 circuit varies with a position of the first memory cell unit when read-out of the memory cell is performed, and

a second voltage charging a second interconnect with the second sense amplifier circuit varies with a position of the second memory cell unit when read-out of the memory cell is performed.

20

9. The device according to claim 8, wherein the first voltage increases as the position of the first memory cell unit becomes farther from the first sense amplifier circuit, and the second voltage increases as the position of the second memory cell unit becomes farther from the second sense amplifier circuit.

25

10. The device according to claim 9, further comprising a first register connected to the first sense amplifier circuit, the first sense amplifier circuit

changes a voltage applied to the first interconnect based on the position of the first memory cell unit and an interconnect resistance value stored in the first register when read-out of the memory cell is performed; and

a second register connected to the second sense amplifier circuit,

5 the second sense amplifier circuit changes a voltage applied to the second interconnect based on the position of the second memory cell unit and an interconnect resistance value stored in the second register when read-out of the memory cell is performed.

10 11. The device according to claim 9, wherein the first sense amplifier circuit changes the first voltage applied to the first interconnect and the second sense amplifier circuit changes the second voltage applied to the second interconnect when read-out of the memory cell is performed so that a current flowing through the plurality of memory cells included in the first memory cell unit and a current
15 flowing through the plurality of memory cells included in the second memory cell unit become equal.

12. A semiconductor memory device comprising:

a memory cell array including:

20 a plurality of first memory cell units, each of the plurality of first memory cell units including a plurality of memory cells;

a plurality of second memory cell units, each of the plurality of second memory cell units including a plurality of memory cells;

25 a plurality of first interconnects, each of the plurality of first interconnects extending in a first direction and being connected to one end of each of the first memory cell units; and

a plurality of second interconnects, each of the plurality of second interconnects extending in the first direction in each space between the first interconnects and being connected to one end of each of the second memory cell units, heights of upper surfaces of the second interconnects being equal to heights of upper surfaces of the first interconnects;

5 a first sense amplifier circuit connected to the plurality of first interconnects;

a second sense amplifier circuit connected to the plurality of second interconnects;

10 the plurality of first interconnects and the plurality of second interconnects formed adjacent to each other being formed of a structure in which a plurality of pairs are repeated,

at least one of a width of each of the plurality of second interconnects along a second direction perpendicular to the first direction and a thickness of each of the plurality of second interconnects along a third direction perpendicular to the first direction and the second direction being set smaller than each of the plurality of first interconnects,

the first sense amplifier circuit and the second sense amplifier circuit being formed on one side of the memory cell array,

20 a first voltage charging the first interconnect with the first sense amplifier circuit varying with a position of the first memory cell unit when read-out of the memory cell is performed, and

a second voltage charging the second interconnect with the second sense amplifier circuit varying with a position of the second memory cell unit when read-out of the memory cell is performed.

13. The device according to claim 12, wherein the first sense amplifier circuit

is formed nearer to the memory cell array than the second sense amplifier circuit.

14. The device according to claim 12, wherein the first voltage increases as
5 the position of the first memory cell unit becomes farther from the first sense amplifier circuit, and the second voltage increases as the position of the second memory cell unit becomes farther from the second sense amplifier circuit.

15. The device according to claim 12, further comprising a first register
10 connected to the first sense amplifier circuit, the first sense amplifier circuit changes a voltage applied to the first interconnect based on the position of the first memory cell unit and an interconnect resistance value stored in the first register when read-out of the memory cell is performed; and

a second register connected to the second sense amplifier circuit,

15 the second sense amplifier circuit changes a voltage applied to the second interconnect based on the position of the second memory cell unit and an interconnect resistance value stored in the second register when read-out of the memory cell is performed.

20 16. The device according to claim 12, wherein the first sense amplifier circuit changes the first voltage applied to the first interconnect and the second sense amplifier circuit changes the second voltage applied to the second interconnect when read-out of the memory cell is performed so that a current flowing through the plurality of memory cells included in the first memory cell unit and a current
25 flowing through the plurality of memory cells included in the second memory cell unit become equal.

17. A semiconductor memory device comprising:

a memory cell array including:

a plurality of first memory cell units, each of the plurality of first
5 memory cell units including a plurality of memory cells;

a plurality of second memory cell units, each of the plurality of
second memory cell units including a plurality of memory cells;

a plurality of first interconnects, each of the plurality of first
interconnects extending in a first direction and being connected to one
10 end of each of the first memory cell units; and

a plurality of second interconnects, each of the plurality of second
interconnects extending in the first direction in each space between the
first interconnects and being connected to one end of each of the second
memory cell units;

15 a sense amplifier circuit connected to the plurality of first interconnects
and the plurality of second interconnects; and

a switching circuit configured to switch between a connection of the
sense amplifier circuit with the plurality of first interconnects and a connection of
the sense amplifier circuit with the plurality of second interconnects,

20 at least one of a width of each of the plurality of second interconnects
along a second direction perpendicular to the first direction and a thickness of
each of the plurality of second interconnects along a third direction
perpendicular to the first direction and the second direction being set smaller
than each of the plurality of first interconnects,

25 a first voltage charging the first interconnect with the sense amplifier
circuit varying with a position of the first memory cell unit when read-out of the
memory cell is performed, and

a second voltage charging the second interconnect with the sense amplifier circuit varying with a position of the second memory cell unit when read-out of the memory cell is performed.

5 18. The device according to claim 17, wherein the first voltage increases as the position of the first memory cell unit becomes farther from the sense amplifier circuit, and the second voltage increases as the position of the second memory cell unit becomes farther from the sense amplifier circuit.

10 19. The device according to claim 17, further comprising a register connected to the sense amplifier circuit; wherein the sense amplifier circuit changes the first voltage applied to the first interconnect based on the position of the first memory cell unit and an interconnect resistance value stored in the register when read-out of the memory cell is performed, and

15 the sense amplifier circuit changes the second voltage applied to the second interconnect based on the position of the second memory cell unit and an interconnect resistance value stored in the register when read-out of the memory cell is performed.

20 20. The device according to claim 17, the first voltage is the same as the second voltage.

21. The device according to claim 17, the first voltage is different from the second voltage.

25

22. A semiconductor memory device comprising:
a memory cell array including:

a plurality of first memory cell units, each of the plurality of first memory cell units including a plurality of memory cells;

a plurality of second memory cell units, each of the plurality of second memory cell units including a plurality of memory cells;

5 a plurality of first interconnects, each of the plurality of first interconnects extending in a first direction and being connected to one end of each of the first memory cell units; and

 a plurality of second interconnects, each of the plurality of second interconnects extending in the first direction in each space between the
10 first interconnects and being connected to one end of each of the second memory cell units, heights of upper surfaces of the second interconnects being equal to heights of upper surfaces of the first interconnects;

a first sense amplifier circuit connected to the plurality of first interconnects; and

15 a second sense amplifier circuit connected to the plurality of second interconnects;

 the plurality of first interconnects and the plurality of second interconnects formed adjacent to each other being formed of a structure in which a plurality of pairs are repeated,

20 at least one of a width of each of the plurality of second interconnects along a second direction perpendicular to the first direction and a thickness of each of the plurality of second interconnects along a third direction perpendicular to the first direction and the second direction being set smaller than each of the plurality of first interconnects,

25 a first read time until reading out data of the first memory cell unit to the first sense amplifier circuit after charging the first interconnect

varying with a position of the first memory cell unit in the first direction when read-out of the memory cell is performed, and

5 a second read time until reading out data of the second memory cell unit to the second sense amplifier circuit after charging the second interconnect varying with a position of the second memory cell unit in the first direction when read-out of the memory cell is performed.

23. The device according to claim 22, wherein the first sense amplifier circuit and the second sense amplifier circuit are formed on one side of the memory
10 cell array.