METHOD OF PACKAGING AN INTEGRATED CIRCUIT DEVICE

FIELD OF THE INVENTION

The present invention relates to electronic devices. In particular, the present invention relates to the packaging of integrated circuits.

BACKGROUND OF THE INVENTION

As the trend towards miniaturisation and compact products continues in the electronic industry, lighter, smaller, thinner and faster electronic packaging are critically demanded. The use of Flip-Chip has inherent advantages over other methods for electronic packaging due to its high density and short signal-propagation path. In Flip-Chip technology, integrated circuit (IC) chips are electrically connected via solder bumps to the input/output (I/O) pads of the substrate by a reflowing process. In order to achieve a reliable solder interconnection, a fluxing agent is typically applied to the terminals to rid them of oxides. Following proper soldering, the fluxing agent is removed by washing, after which a filling material is applied to fill the gap between the IC device and the substrate to form an encapsulated package. This material is generally known as an underfill material.

The underfill material is generally made from silica filled epoxy which is designed to have a relatively lower coefficient of thermal expansion (CTE) close to that of the solder material. As a result, the thermo-mechanical stress resulting from assembling the chip to the organic

substrate can be transferred from the fragile solder bump to the more strain-tolerant substrate through the underfill.

The process of flowing the underfill material to the gap between the chip and the substrate is a tedious one. To eliminate this step, no-flow underfill materials have been developed in which fluxing agents such as organic acids have been added such that the underfill material possesses fluxing ability. In this way, the reflow step is combined with the encapsulation step, and the cleaning step is eliminated. This shortened process, as described in US patent no. 5,128,746, involves dispensing the no-flow underfill material directly onto the substrate before placement of the bump side of the chip thereon. This is followed by reflowing of the solder bumps.

Although no-flow underfill materials have the advantage of allowing the packaging process to be simplified, they generally do not contain silica-fillers, and have a CTE much higher than conventional underfill materials. As a result, packages using this type of material tend to give solder bump cracks, particularly for large die sizes. To solve this problem, US patent no. 5,814,401 describes a selectively filled thermally curable adhesive film that contains a central interior region and a boundary region. The central region consists of an adhesive that is filled with an inert filler to reduce the CTE of the material. The boundary region consists of an adhesive and a fluxing agent. When the solder bumps on the die are reflowed, the fluxing agent acts to remove any oxides present on the solderable surface of the substrate or the die, and thus eliminate the need for additional fluxes. The film is used to adhesively bond a flip chip die to a substrate. The central region of the adhesive film lies under the centre of the die where there are no solder bumps, and acts to stabilise the die after

bonding to the substrate. This arrangement, however, is only useful for chips in which solder bumps are only present on the periphery, and cannot be used for flip chips that have bumps on the entire surface. Furthermore, the use of a film typically requires some pressure or holding force to press the chip onto the substrate during the reflow process to ensure proper soldering. Such a requirement is incompatible with surface mount technology (SMT) processes.

In wafer level packaging, it has been proposed that an epoxy material may be applied to the bumped side of the wafer to encapsulate the wafer before singulation into chips, followed by direct reflow onto a printed circuit board. The CTE of the encapsulation material, however, still needs to be maintained close to that of the solder bump in order to ensure reliability.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a method for packaging that reduces the aforementioned problems.

Accordingly, the present invention provides, in one aspect, a method of packaging a bumped electronic chip or a bumped wafer by utilizing a combination of two different encapsulants. The first encapsulant (low CTE encapsulant) contains an adhesive filled with a CTE-reducing filler. The second encapsulant (fluxing encapsulant) contains an adhesive containing a fluxing agent or a precursor of a fluxing agent. In another aspect, the low CTE encapsulant is applied directly onto the bumped surface while still allowing part of the solder bump to be exposed for soldering onto the corresponding I/O pad of the prescribed substrate. The solder joint is reflowed in the presence of a layer of fluxing encapsulant that causes the final adhesion between the bumped surface and the substrate.

In the preferred embodiment, the fluxing encapsulant is in a liquid state, such that the reflow process may be performed under standard conditions without the need for a holding force to keep the chip and the substrate together during reflowing. The use of a liquid fluxing encapsulant gives the important benefit of being SMT (surface mount technology) compatible.

The present method may be applied to various semi-conductor packaging technology. According to one embodiment of the present invention, a bumped wafer is packaged by applying and curing the low-CTE encapsulant onto the bumped surface of the wafer before singulation into chips. The singulated chip can then be soldered onto an appropriate substrate of an electronic component, such as a printed circuit board

(PCB) by applying the fluxing adhesive onto the prescribed surface of the PCB, and reflowing the assembly.

In the preferred method, the low-CTE adhesive is cured or partially cured onto the bumped surface, and the exposed ends of each bumps is cleaned of any adhesive. Post-curing may be performed after reflowing of the bumps in the presence of the fluxing adhesive.

The product produced thereof comprises a first and second electronic component that are electrically connected through solder joints. The space between the solder joints is filled with two layers of encapsulant material. The first encapsulant material, in direct contact with the bumped surface of the first electronic component, contains a low-CTE adhesive. A second encapsulant layer, containing a fluxing agent or a fluxing precursor, is disposed between the first encapsulant layer and the prescribed surface of the second electronic component. Embedded within the first and second encapsulant layers and traversing therethrough are the solder joints.

This method combines the convenience of a no-flow fluxing adhesive with the reliability of a low-CTE encapsulant material. In addition, the use of fluxing encapsulant that is in a liquid form during the application step ensures that no additional holding pressure is required to maintain good contact between the bumps and the terminals of the prescribed surface during the reflow process. As a result, the method is SMT-compatible, while improving on overall packaging time and reliability. Furthermore, the process is easily adapted for wafer-level packaging, making this type of packaging one step further towards a manufacturing reality.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A to 1D are schematic drawings to illustrate the method according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention combines two important properties of a good encapsulant i.e. low CTE and processing convenience, by making use of two separate encapsulants, each providing one of the two desired properties, within the same packaging process. In the following description and in the claims, the terms "including', "comprising", and "containing" are used in an open-ended fashion, and thus should be interpreted to mean "including but not limited to.....". The term "bumps" refers to structures that can be reflowed to form electrical interconnections between electronic components. Examples of bumps include, but are not limited to, tin and lead solder bumps, and joints made from a combination of solder and other material, e.g. electroplated material.

The low-CTE encapsulant has a CTE close to that of the solder material and typically contains an adhesive and a CTE-reducing filler. An example is an epoxy adhesive containing silica as a filler. Another example is an epoxy adhesive with aluminum nitrite or boron nitrite as filler. As further non-limiting examples, a low-CTE encapsulant for semi-conductor chip packaging has a CTE of 10-50ppm/degree Celsius. Another non-limiting example is a low-CTE encapsulant with a CTE of 20-45ppm/degree Celsius

The fluxing adhesive contains an adhesive and a agent that gives a fluxing ability under reflow conditions. The adhesive may be, for example epoxy, silicone or thermoplastic. The agent may be, for example, a fluxing agent or a fluxing precursor. Examples of fluxing agents include organic acids that have the ability to remove oxide coatings, as described in PCT application WO 99/03597, and US patent no. 5128746, which are incorporated herein by reference. Example of a fluxing precursor is an alcohol added together with an anhydride. According to the preferred embodiment of the present invention, the fluxing adhesive is in a liquid form when applied onto the prescribed substrate surface. Examples of substrates include, but are not limited to, second level packaging substrates and printed circuit boards.

Tables 1 and 2 show example of low-CTE adhesives and fluxing adhesive respectively.

Component	Amount (g)	
	EXAMPLE 1	EXAMPLE 2
Epikote 828	20	35
Tetrahydrophthalic anhydride	15	0
2E4MZ	0.3	1.7
Methyl ethyl ketone	8	5
Fused Silica	70	65

TABLE 1 : LOW-CTE ADHESIVES

COMPONENT	Amount (g)
EPON 8281	30
ERL 4221	70
Hexahydro-4-methylphthalic anhydride	80
Co (II) acetylacetonate (ACAC)	0.72
Glycerol	4.5

TABLE 2 : FLUXING ADHESIVE

The method according to the present invention may be performed on a wafer **20** with solder bumps **22** on the bumped surface **23**. In the final product, the bumps have one end soldered onto the I/O pads of the chip **20a**, and a free end for soldering onto the prescribed surface **25** of a substrate **28** during packaging or assembly. Referring to Fig.1A to 1D, the low-CTE encapsulant material **24** is applied onto the bumped surface **23** of the wafer **20** (Fig.1A and 1B). One technique that can be used is spin coating of a liquid low-CTE encapsulant, followed by curing (either completely or partially), before any excess encapsulant is removed. Curing may be through heating or chemical means. The cured low-CTE encapsulant is preferably of a thickness lower than the bumps, such that part of the bumps are exposed, as shown in Fig. 1B. Another technique that can be used is by molding, e.g. of semi-solid or solid (resin). If there is excess encapsulant, i.e. the free end(s) of one or more bumps are covered by the cured low-CTE encapsulant, cleaning of the free ends is performed, for example using plasma etching or laser technology. Thereafter, the wafer may be singulated to obtain individual chips. For ease of illustration, details of only one portion of the wafer is shown in Figures 1A and 1B. The remaining portions of the wafer are only depicted as dotted lines, and the location of cutting shown by dotted arrows **30** by which singulated chip **20a** is obtained. Fluxing adhesive **26** is then applied to the prescribed surface **25** of the substrate **28** on which terminals for interconnection with the bumps are found (Fig.1C). The fluxing adhesive is preferably applied as a thin liquid layer with the prescribed surface of the substrate facing upwards. Conventional methods of application, such as dispensing, printing or dipping, may be used. The chip **20** with the low-CTE encapsulant is then placed onto the

substrate such that the bumps **22** are in contact with the corresponding terminals of the substrate **28** (Fig.1D). This may be performed by conventional pick and place systems. The chip/substrate assembly is then transferred to a reflow oven for reflowing. Depending on the type of encapsulant material used, a post-curing step, for example of heating at lower temperatures e.g. 150°C for 30 minutes, may be required to completely cure the adhesives.

While the present invention has been described particularly with references to Figs 1A to 1E , it should be understood that the figures are for illustration only and should not be taken as limitation on the invention. In addition it is clear that the method of the present invention has utility in many applications where no-flow underfill and other types of surface mounting components are used. It is contemplated that many changes and modifications may be made by one of ordinary skill in the art without departing from the spirit and the scope of the invention described.

CLAIMS

1. A method of packaging a semi-conductor chip, said chip derived from a semi-conductor wafer, said wafer having at least one surface containing solder bumps, said bumps having one free end for electrical connection to a substrate, said substrate having a prescribed surface with metallic terminals provided for electrical connection with said bumps, said method comprising :

   a) applying a low-CTE encapsulant onto the bumped surface of said wafer;

   b) curing said low-CTE encapsulant;

   c) exposing said free end of said bumps;

   d) singulating said wafer to obtain a plurality of low-CTE encapsulated chips;

   e) applying a fluxing encapsulant onto the prescribed surface of said substrate;

   f) placing said singulated chip onto said substrate such that said bumps are in contact with said terminals of said prescribed surface;

   g) reflowing said bumps such that said bumps are soldered onto said terminals.

2. A method according to claim 1 wherein said exposing step comprises laser ablation or plasma etching.

3. A method according to claim 1 wherein said applying step uses molding technology.

4. A method according to claim 1 wherein said applying step uses spin coating technology

5. A method according to claim 1 wherein said curing step causes complete curing or partial curing of said low-CTE adhesive.

6. (Canceled)

7. An electronic package according to claim 6 wherein said first encapsulant layer has a coefficient of thermal expansion of 10-50ppm/degree celsius.

8. An electronic package according to claim 6 wherein said first encapsulant layer contains silica filler and said second encapsulant layer contains a fluxing additive.

9. An electronic package according to claim 6 wherein said second adhesive layer containing an agent that is capable of removing oxides during solder reflow before said second adhesive is cured.

10. An electronic package according to claim 6 wherein said first component is a semi-conductor chip.

11. An electronic package according to claim 6 wherein said first adhesive layer comprises an epoxy resin and a silica filler.

12. An electronic package according to claim 4 wherein said second adhesive layer comprises an epoxy resin and a fluxing agent.

13. An electronic package according to claim 4 wherein said second adhesive layer comprises an epoxy resin and an organic acid.

14. An electronic package according to claim 4 wherein said second adhesive layer comprises an epoxy resin, a hydroxyl-containing fluxing precursor and an anhydride.