WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

an epitaxial group III-V channel layer;

an epitaxial Group III-V barrier layer disposed over the channel layer;

a source recess region and drain recess region extending vertically through the barrier layer and into the channel layer;

a doped Group III-V ohmic contact layer disposed directly on bottom and inner sidewalls of the source recess and the drain recess, the doped ohmic contact layer being of the same material as the channel layer, the doped ohmic contact layer having a portion extending horizontally on the barrier layer and having a gap therein between the source recess and the drain recess;

a gate electrode disposed in the gap and on the barrier layer, the gate electrode having a lower, vertically extending stem portion; and

a dielectric structure disposed over the ohmic contact layer and over the barrier layer and extending continuously from a region over the source recess to one side of the stem portion and then extending continuously from an opposite side of the stem portion to a region over the drain recess, a first portion of the dielectric structure being in contact with the stem portion and the barrier layer, a second portion of the dielectric structure within the source recess and the drain recess.

2. The semiconductor device recited in claim 1 wherein the dielectric structure includes: a first dielectric layer disposed on and extending over the horizontally extending ohmic contact layer and being in contact with the stem portion; and a second dielectric layer disposed on the first dielectric layer and of a material different from the first dielectric layer and in contact with the stem portion and the bottom of a horizontal portion of the gate electrode.

3. The semiconductor device recited in claim 1 wherein the dielectric structure comprises:

a first dielectric layer;

a second dielectric layer; and

a third dielectric layer,

wherein the first dielectric layer is disposed on and extends over the horizontally extending ohmic contact layer and is in contact with the third dielectric layer, wherein the third dielectric layer is in contact with the stem portion, and

wherein the second dielectric layer is disposed on the first and third dielectric layers and has a material different from the first dielectric layer and is in contact with the stem portion and the bottom of the horizontal portion of the gate electrode.

4. The semiconductor device recited in claim 1 wherein the dielectric structure is disposed on the barrier layer and is in contact with sides of the stem portion and under, and in contact with a bottom portion of a horizontal portion, the bottom portion of the horizontal portion being at a vertical elevation higher than a top surface of the horizontally extending portion of the ohmic contact layer.

5. The semiconductor device recited in claim 1 wherein the doped Group III-V ohmic contact layer in contact with the source and drain recesses and the barrier layer and a field region is single crystal material.

6. The semiconductor device recited in claim 1 wherein, a portion of the doped Group III-V ohmic contact layer in direct contact with a portion of the dielectric structure is polycrystal while a portion of the group III-V ohmic contact layer in the source and drain recesses is single crystal.

7. The semiconductor device recited in claim 1 wherein the channel layer and the doped Group III-V ohmic contact layer comprise GaN.

8. The semiconductor device recited in claim 2 wherein the barrier layer comprises $Al_xGa_{1-x}N$ where x is between 0 and 1.

9. The semiconductor device recited in claim 2 wherein the barrier layer comprises $Sc_yAl_{1-y}N$ where y is between 0 and 0.5.

10. The semiconductor device recited in claim 1 wherein, a portion of the doped Group III-V ohmic contact layer in direct contact with a portion of the dielectric structure and in the source and drain regions is polycrystal.

11. The semiconductor device recited in claim 1 wherein the doped Group III-V ohmic contact layer comprises AlN.

12. The semiconductor device recited in claim 1 wherein the doped Group III-V ohmic contact layer comprises InN.

13. The semiconductor device recited in claim 1 wherein the barrier layer comprises $Al_xGa_{1-x}N$ where x is between 0 and 1.

14. The semiconductor device recited in claim 1 wherein the barrier layer comprises $Sc_yAl_{1-y}N$.

15. The semiconductor device recited in claim 1 wherein the barrier layer comprises $B_xAl_{1-x}N$.

16. The semiconductor device recited in claim 1 wherein the barrier layer comprises $Sc_yAl_{1-y}N$, where y is ≥ 0.18.