(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
25 September 2025 (25.09.2025)

WIPO | PCT

(10) International Publication Number
WO 2025/199297 A1

(51) International Patent Classification:
G06F 9/30 (2018.01) *G06F 12/0806* (2016.01)
G06F 15/76 (2006.01) *G06F 15/00* (2006.01)
G06F 9/46 (2006.01)

(21) International Application Number:
PCT/US2025/020669

(22) International Filing Date:
20 March 2025 (20.03.2025)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
18/610,302 20 March 2024 (20.03.2024) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UY, UZ, VC, VN, WS, ZA, ZM, ZW.

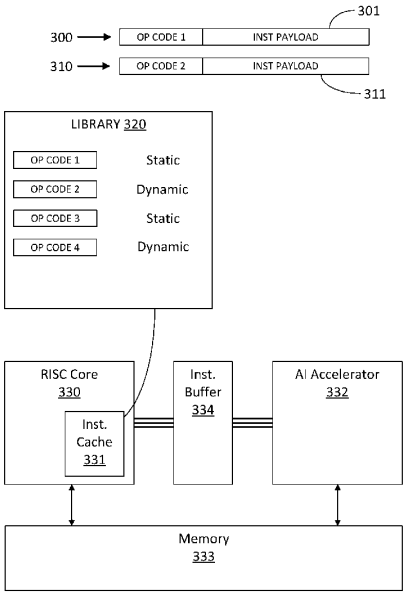
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

WO 2025/199297 A1

(54) Title: STATIC INSTRUCTION CACHING IN A COPROCESSOR ARCHITECTURE

FIG. 3



(57) Abstract: Methods and systems relating to improved coprocessing architectures with static instruction caching are disclosed herein. A disclosed coprocessor architecture includes a processor, a coprocessor defined by an instruction set, a cache of static instruction blocks, and an instruction cache. The instruction set includes at least one static instruction. The instruction cache is configured to identify instructions in a series of instructions as either static instructions or dynamic instructions. The instruction cache is configured to, in response to identifying two or more sequential instructions in the series of instructions as static instructions, cache the two or more sequential instructions in the cache of static instruction blocks as an instruction block and store a program counter value of a program counter. The instruction cache is configured to provide the instruction block to the coprocessor from the cache of static instruction blocks when the program counter returns to the program counter value.