

Fig 1A
(Prior art)



Fig. 1B
(Prior art)

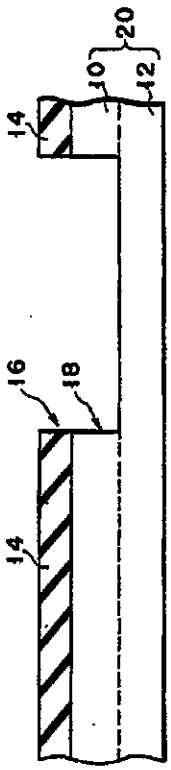


Fig. 1C
(Prior art)

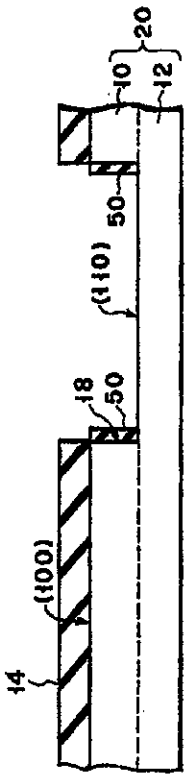


Fig. 1D
(Prior art)

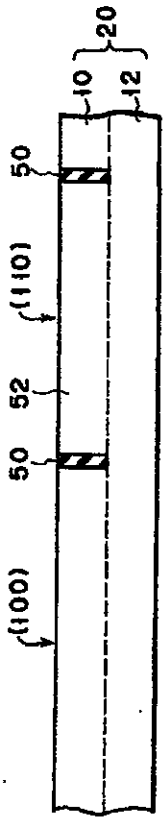


Fig. 1E
(Prior art)

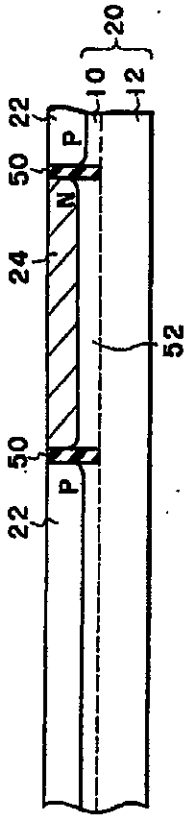


Fig. 1F
(Prior art)

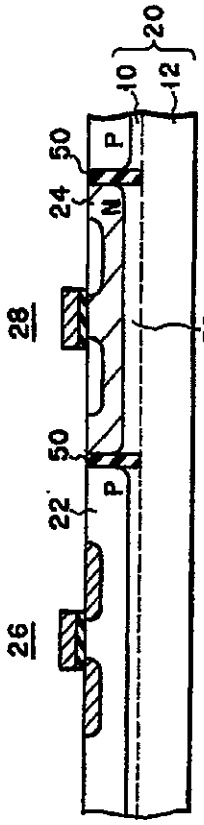


Fig. 1G
(Prior art)

Fig. 2a

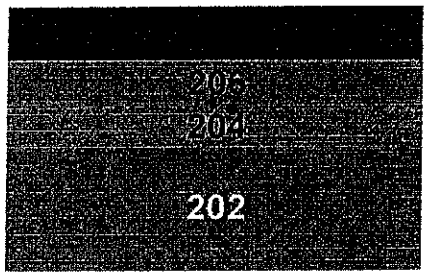


Fig. 2b

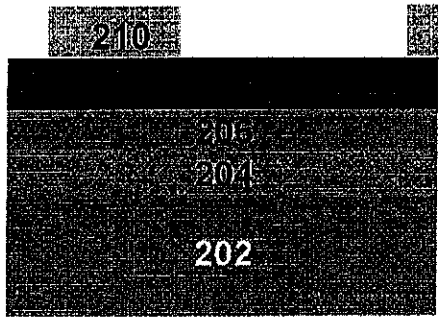


Fig. 2c

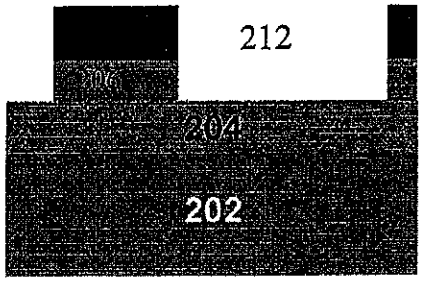
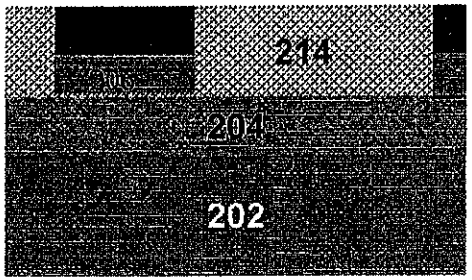


Fig. 2d



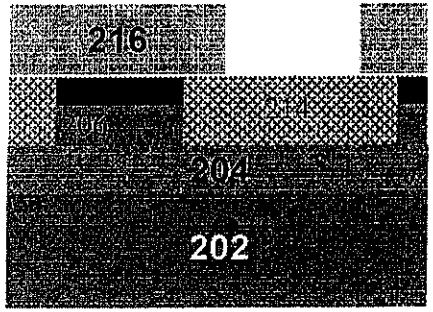


Fig. 2e

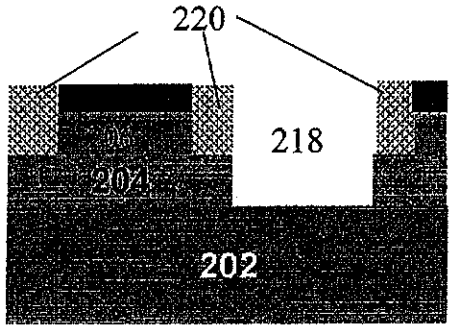


Fig. 2f

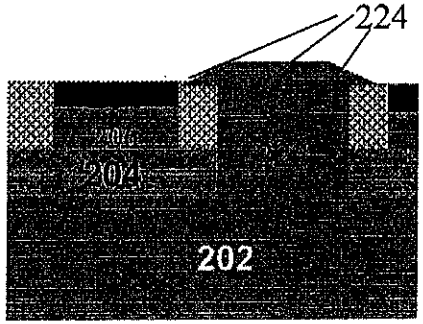


Fig. 2g

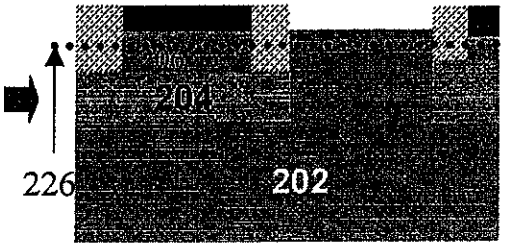


Fig. 2h

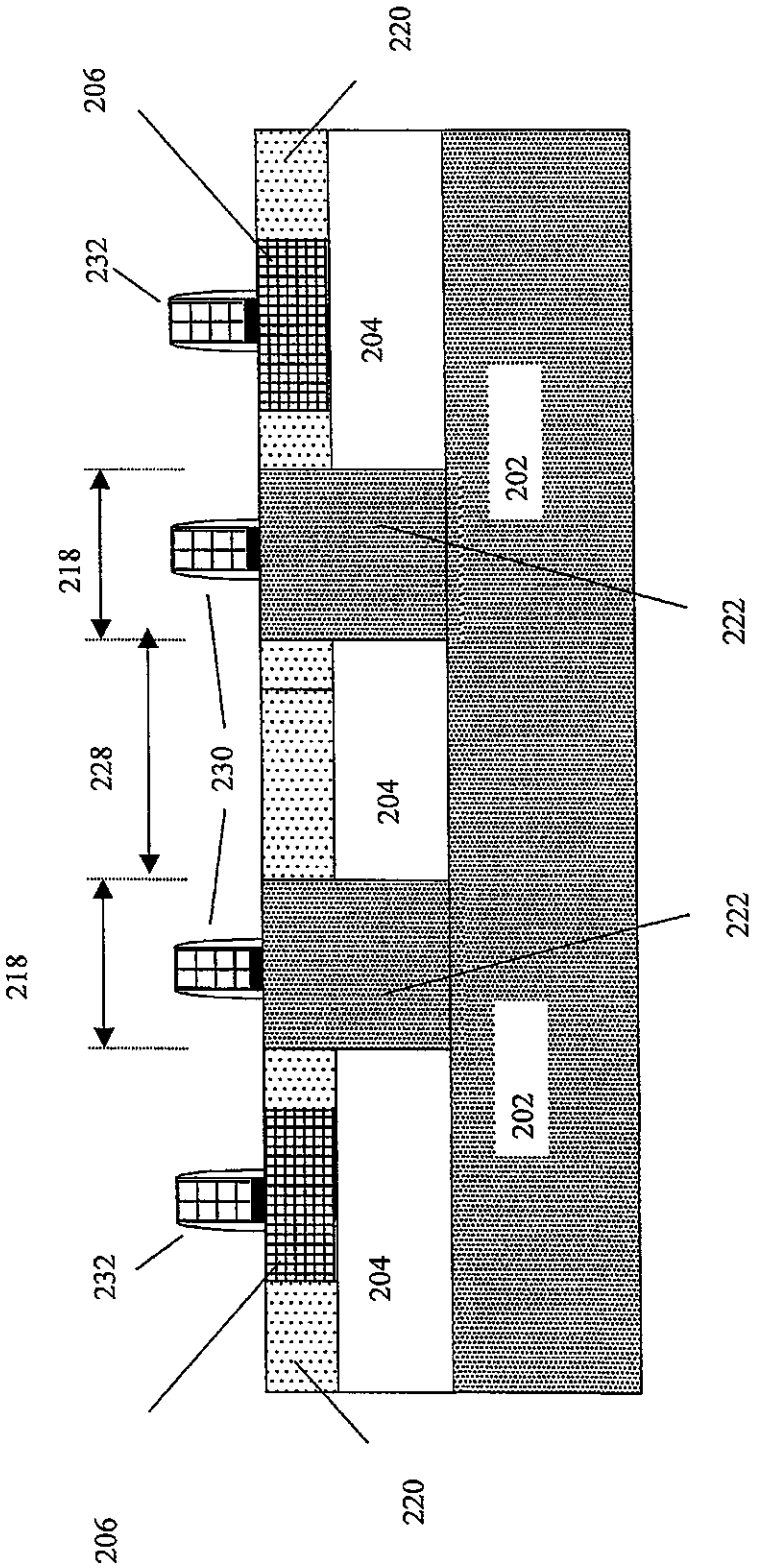

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Fig. 3

Fig. 4b

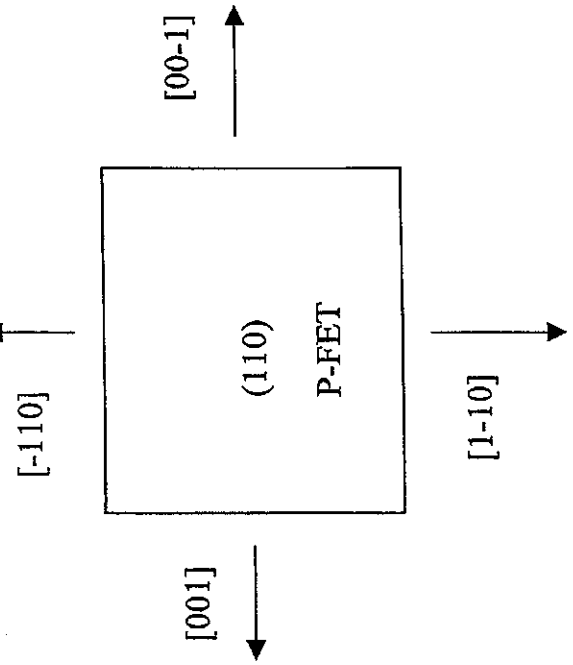


Fig. 4b

Fig. 4a

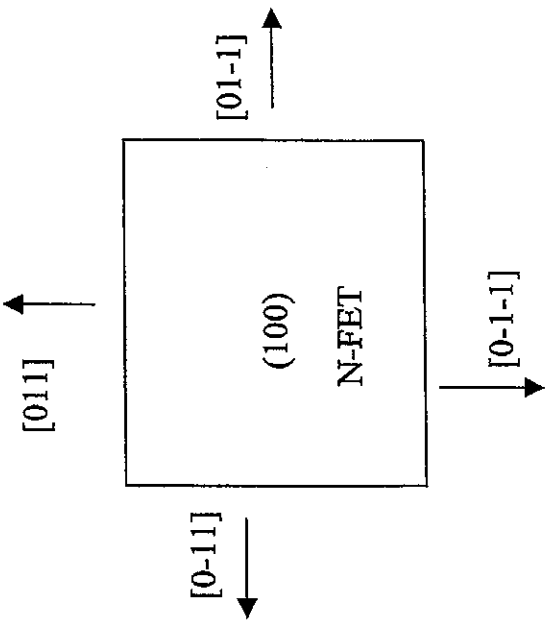


Fig. 4a

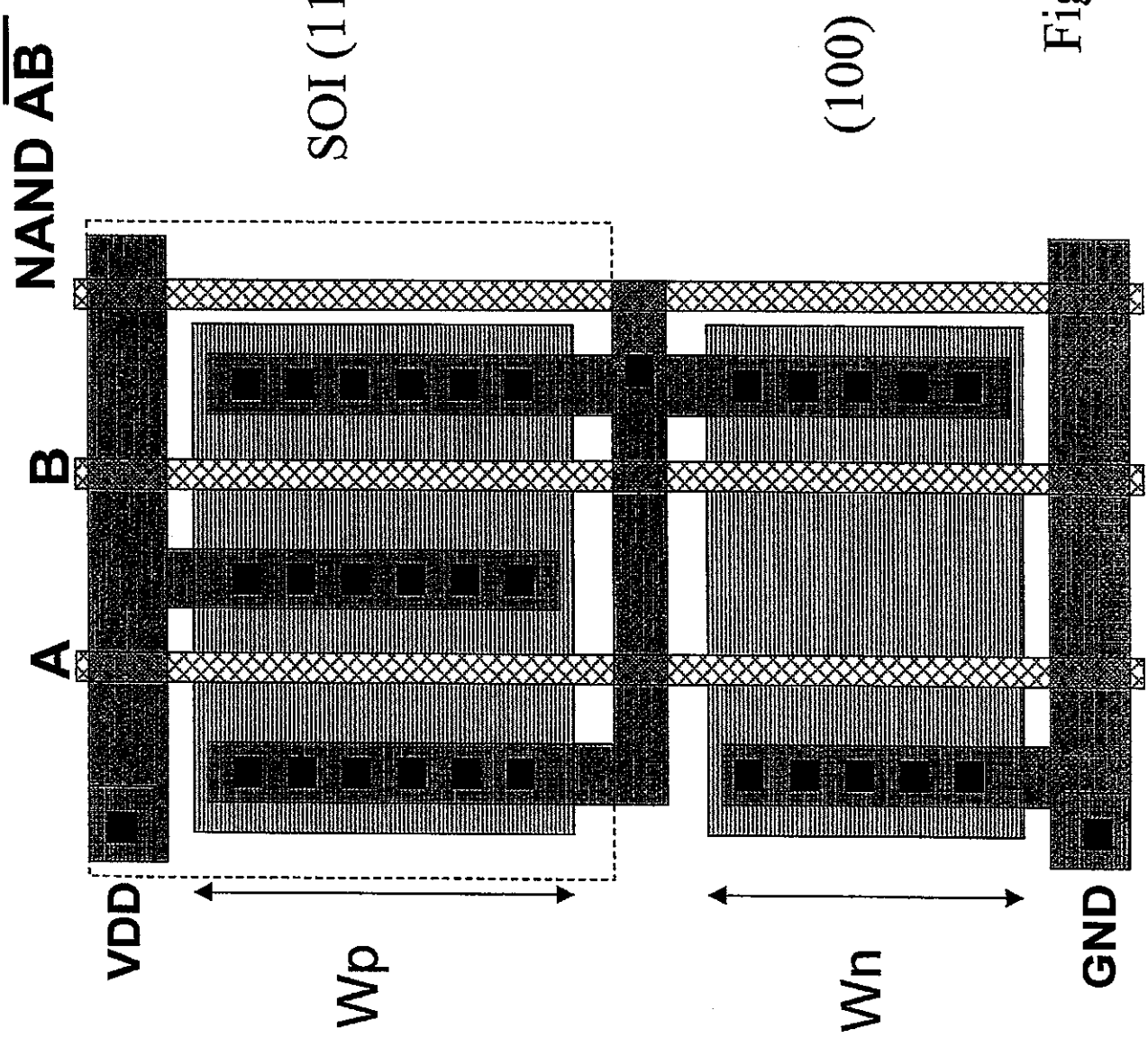


Fig. 5a

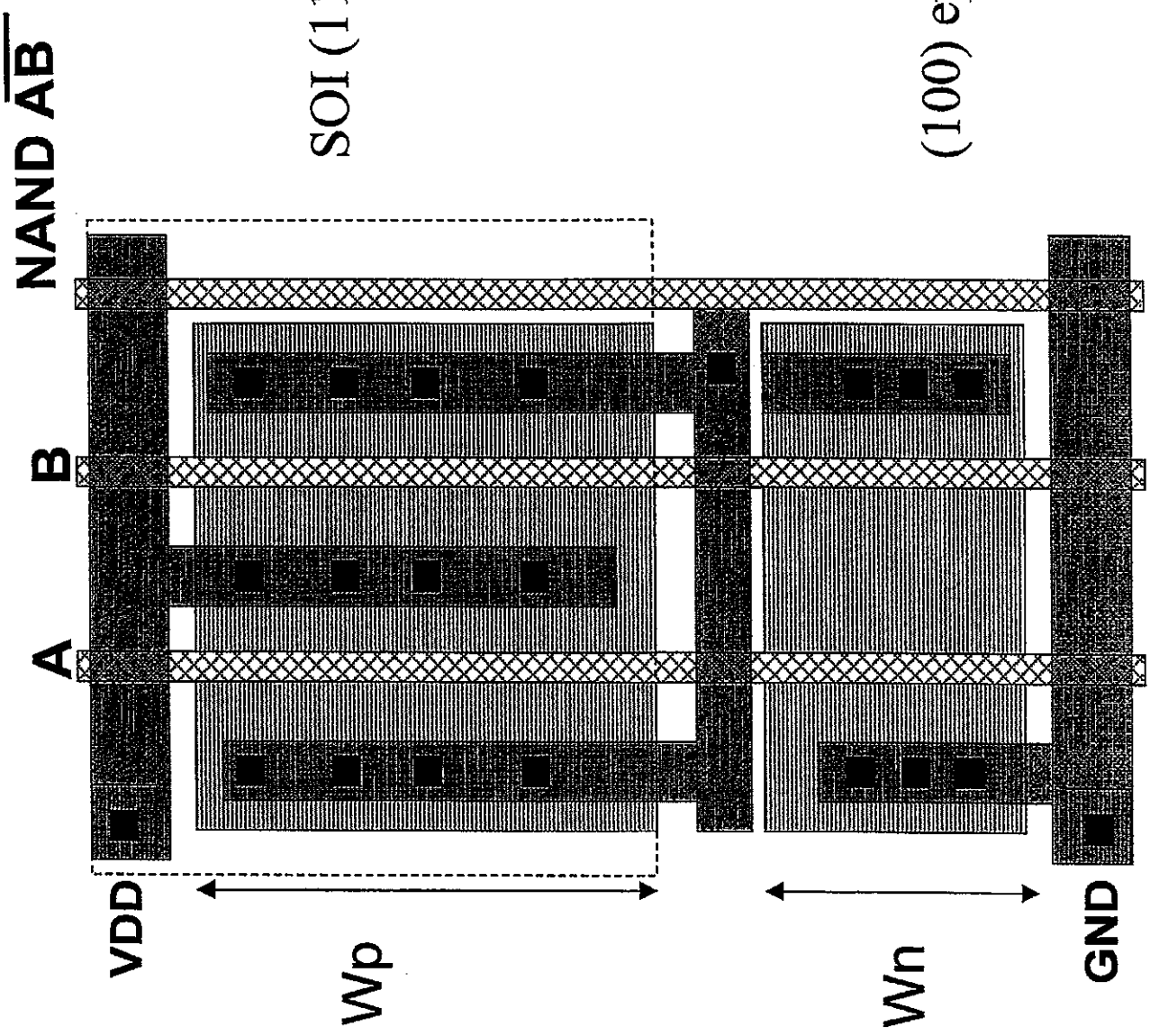


Fig. 5b

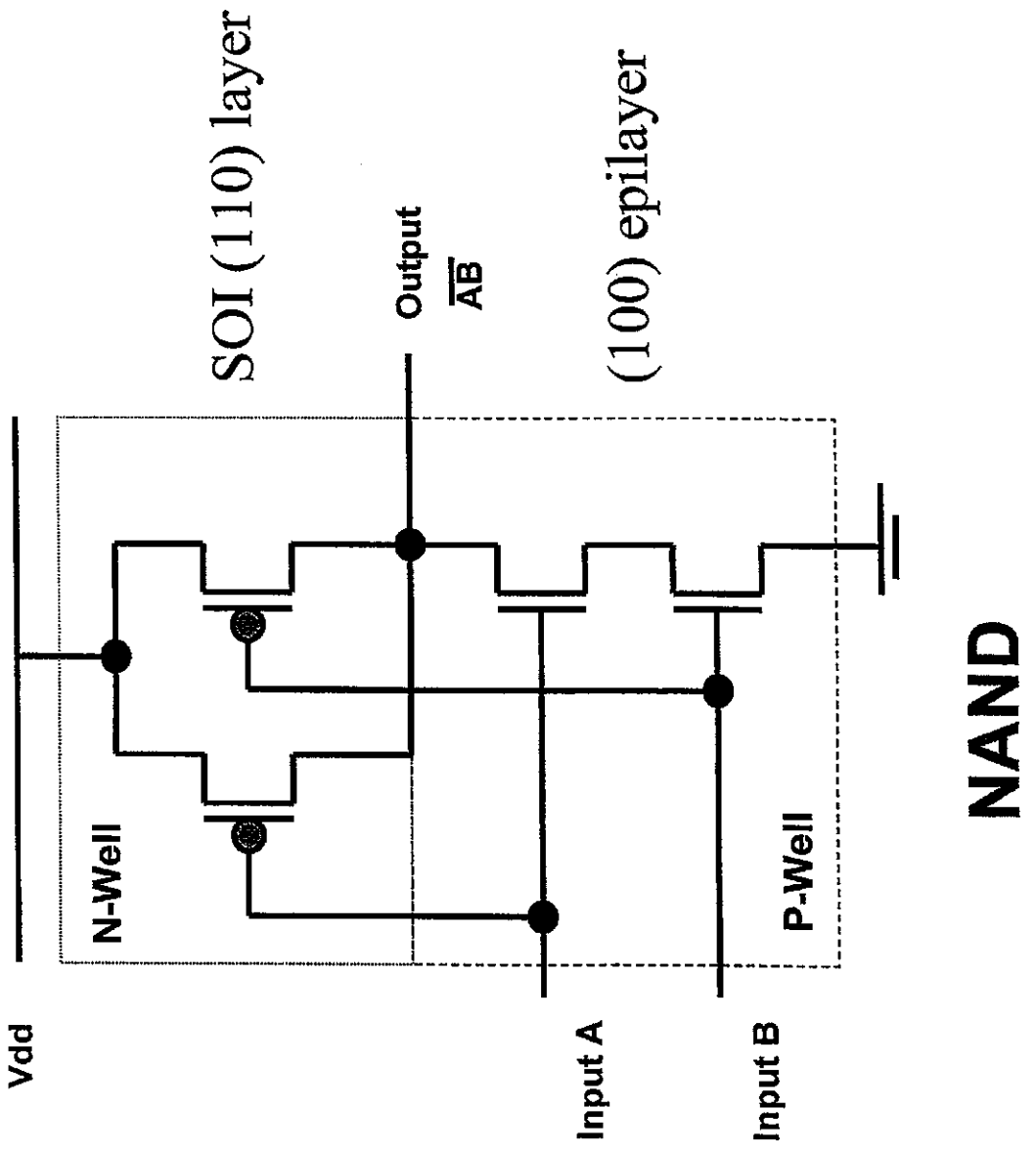

SOI (110) layer
(100) epilayer
Output
$\overline{AB}$
Vdd
N-Well
P-Well
Input A
Input B
NAND

Fig. 6

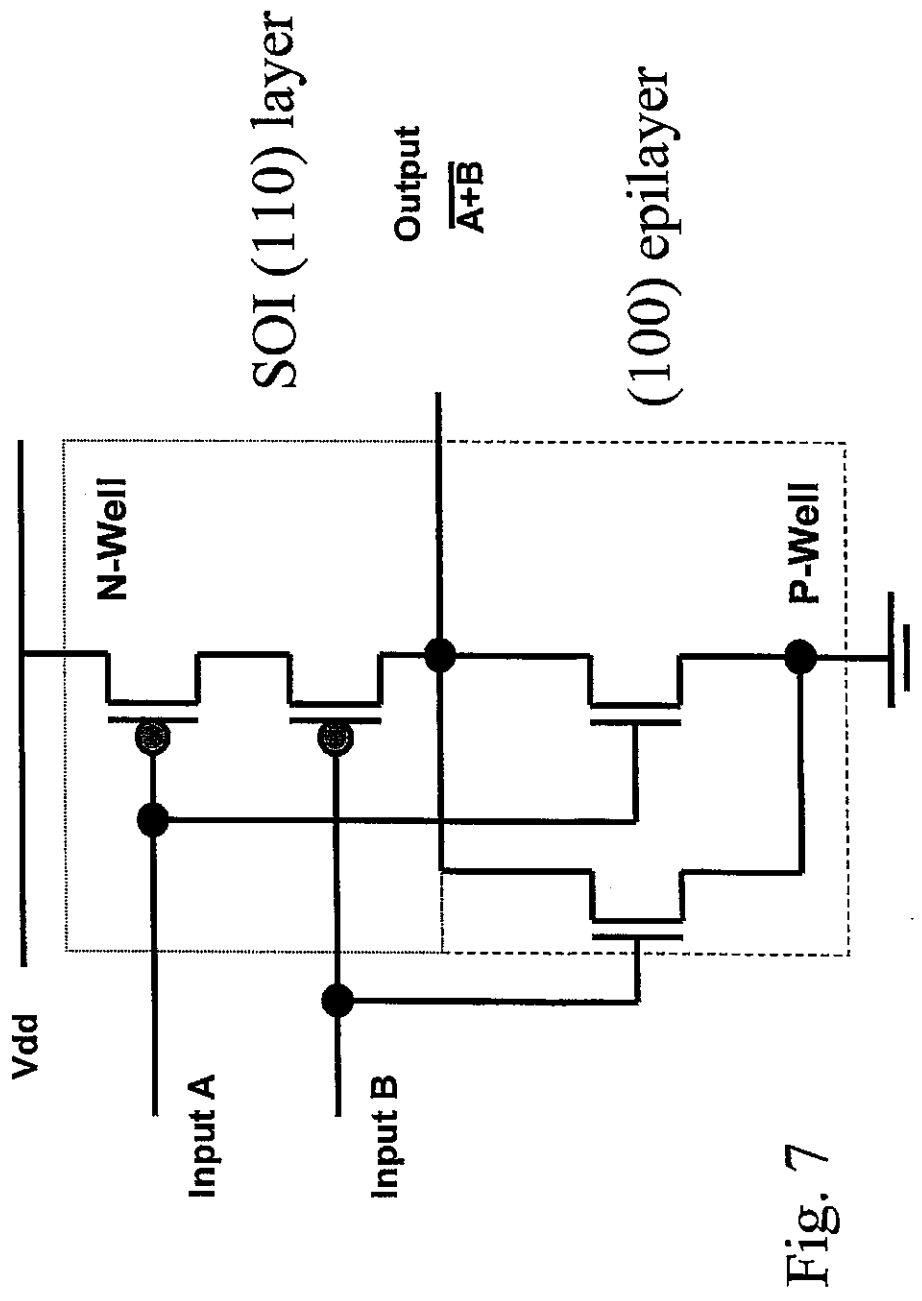

SOI (110) layer
Output
$\overline{A+B}$
(100) epilayer
N-Well
P-Well
Vdd
Input A
Input B
NOR

Fig. 7

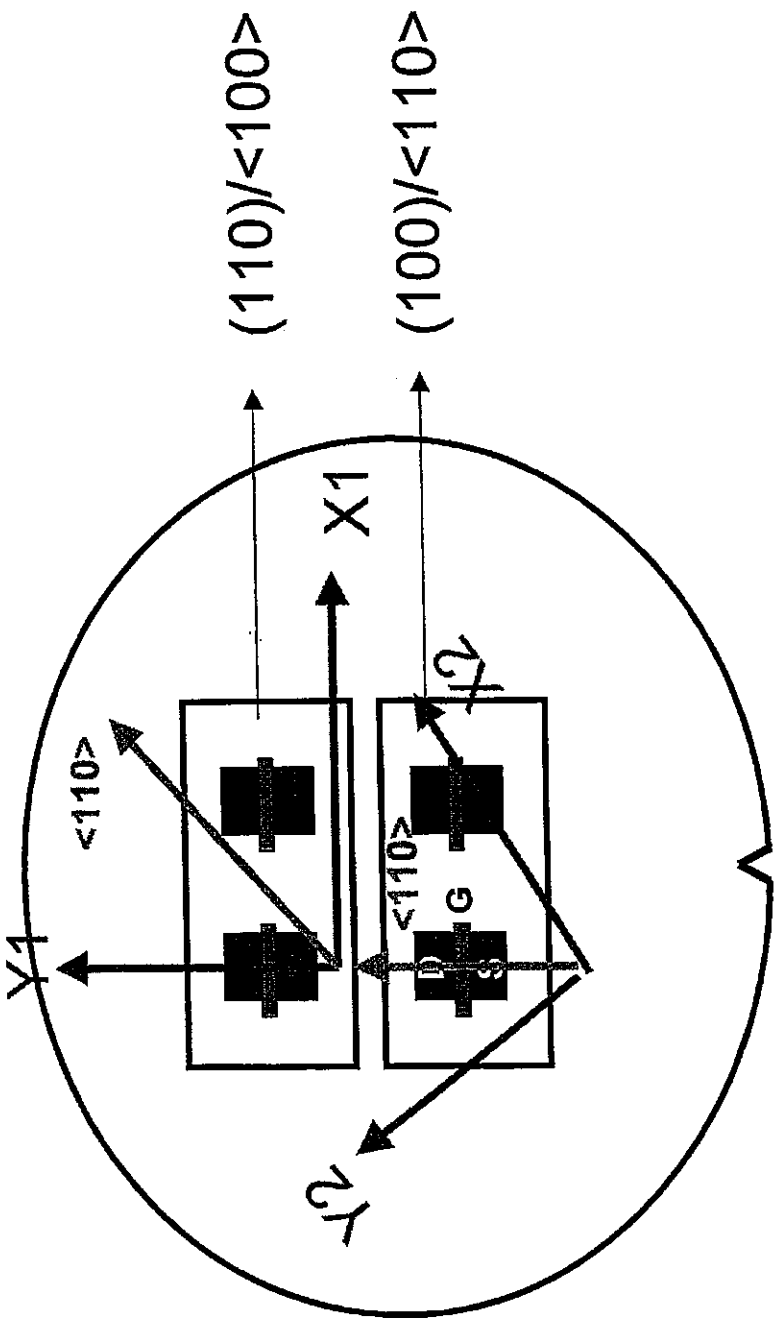


Fig. 8