

Description

The present invention relates to digital decimation and filtering devices and more particularly to a decimation filter for converting a train of sigma-delta pulses into a corresponding train of Pulse Code Modulation samples. Digital filtering as it is addressed here is known from EP-A-0 356 598.

The sigma-delta technology is of great interest for realizing linear, accurate and simple analog-to-digital converters. Sigma-delta coders and decoders generally require the use of decimation circuits requiring a great number of electronic components. For that reason, decimation circuits are embodied by means of Very Large Scale Technology (VLSI) components.

Figure 1 shows the traditional basic structure of an analog-to-digital converter which uses a sigma-delta converter (101) for converting an analog input signal existing on lead 110 to a train of sigma-delta pulses on a lead 120. The train of sigma-delta pulses comprising a high level of out-of-band quantization noise is then entered into a decimation circuit 104 in order to convert the sigma-delta pulses into a sequence of Pulse Code Modulation (PCM) samples on lead 140. For that purpose, decimation circuit 104 includes a low-pass digital filter 102 for suppressing the out-of-band quantization noise mentioned above and for avoiding in-band aliasing during the decimation process. Decimation circuit 104 also includes the specific decimation element which samples down the output signal of low-pass filter. This is simply achieved by taking one sample over N samples. N is called the decimation factor of the decimation process.

Figure 2 illustrates the different spectra which are involved in the sigma-delta conversion and decimation processes. Figure 2a shows a spectrum of a typical band-limited analog input signal which is carried by lead 110 and which is to be coded. Figure 2b shows the spectrum of the corresponding train of sigma-delta pulses existing on lead 120 and resulting from the sigma-delta conversion process. As mentioned above, the sigma-delta bit stream has a high level of out-of-band quantization noise which periodically extends over the whole band with a period f_s which is equal to the value of the sigma-delta modulation frequency. The dotted lines in figure 2c illustrate the frequency response of the low-pass filter and the resulting filtered signal has a spectrum which is shown in figure 2d. Figure 2e illustrates the spectrum of the PCM signal which exists at the output of decimation circuit 104. The PCM words are generated at a frequency of f_s/N .

Generally speaking, the value of the decimation factor N is chosen by considering first the signal/noise ratio which is required and also the band width of the input signal. Since sigma-delta coders and decoders are likely to be used in a wide variety of different applications, it is highly desirable to have a sigma-delta coder having a variable and programmable decimation factor as will be shown in the following examples which have been chosen in the telecommunication field. A first example can be found by considering a V32 modem or DCE. The echo estimation and cancellation techniques involved in such modems require a signal-to-noise ratio which is equal to at least 80 dB. Figure 3 shows a table indicating approximate theoretical values of the signal-to-noise ratio as a function of the band width of the input signal f_b and also the oversampling frequency f_s . It appears in the table that a signal-to-noise ratio of 80 dB is provided in the cases where the ratio f_s/f_b -i.e. the oversampling factor) is equal to at least 300. Since the band-width of such modems is about 3 kHz, the oversampling frequency must be equal to at least 900 kHz. If the V32 modem uses four samples per bit time, the decimation factor appears to be equal to $300/4 = 75$. Conversely, when considering a base-band modem which is intended to be connected to a digital network, the band-width should be at least equal to 72kHz. It results that the preceding oversampling ratio (300) would lead to an oversampling frequency of at least 20 MHz ($300 \times 72\text{kHz}$) which is practically unattainable. However, since such a base-band modem does not involve the highly sophisticated echo-cancellation techniques, a signal-to-noise ratio of 60 dB appears to be sufficient. Figure 3 shows that a signal-to-noise ratio of 60 dB corresponds to an oversampling ratio of at least 64 which results in a decimation factor of $64/2 = 32$ (assuming that the modem is embodied with a sigma-delta coders using two samples per bit time).

Therefore, since the oversampling frequency is compelled to be limited by the actual technology and since the value f_b is likely to vary in a large extent when considering different applications (modems, voice processing system, audio etc...) it is highly desirable to carry out a sigma-delta coder which has a decimation factor variable and adjustable by the user. Since the sigma-delta converter is intended to be embodied in costly, highly sophisticated VLSI technology, it is also desirable that the same chip be able to satisfy a wide variety of users.

The problem to be solved by the present invention is to provide a decimation filter and an analog-to-digital converter having a decimation filter by which it is possible to simply vary the decimation factor N without requiring the use of complex tables in which the different coefficients of the decimation filter are stored for any value of the decimation factor.

This problem is solved by the decimation filter for converting a train of sigma-delta pulses $S(i)$ in synchronism with a sigma-delta clock into a train of PCM samples in accordance with the present invention. The decimation filter has computing means including counting means which is driven by the sigma-delta clock and con-

tinuously incremented by one during N sigma-delta clock pulses, then decremented by two during N following sigma-delta clock pulses and then incremented again by one during N following sigma-delta clock pulses in order to provide a sequence of incrementation parameters DELTA(n). The computing means further includes storing means for storing the value of the coefficient C(n) corresponding to the decimation filter transfer function, and means driven by the sigma-delta clock for incrementing the storing means with the incrementation parameter DELTA(n). The computing means includes means for deriving from the contents C(n) of said storing means and from the train of input sigma-delta samples S(i+n) one Pulse Code Modulation (PCM) sample every 3xN input sigma-delta samples according to the formula:

$$\sum_{n=0}^{3N-1} C_n S_{i+n}$$

Since the coefficients C(n) are directly and on-line computed with the reception of the sigma-delta pulses, the decimation filter can operate for any value of the decimation parameter without requiring the use of further substantial digital processing resources. The decimation filter according to the present invention, which can be embodied into one Very Large Scale Integrated chip, can be used for a wide variety of different applications requiring different decimation factors.

More particularly, the invention is recited in claim 1.

In a preferred embodiment of the invention, the decimation filter includes three computing means respectively driven by a set of three phase-delayed clocks derived from said sigma-delta clock, each of said computing means computing one PCM sample from a sequence of 3xN consecutive input sigma-delta pulses. Therefore, the filter only requires the provision of the PCM clock, the sigma-delta clock and the train of sigma-delta pulses to provide a multipurpose decimation process.

In a more preferred embodiment of the invention, each of the three computing means includes counting means having a control lead and performing an incrementation by one when said control lead is at a first logical level and conversely for performing a decrementation by two when said control lead is at a second logical level. Each of the three computing means further includes a first register for storing the value C(n) of the coefficient to be multiplied by the next sigma-delta input sample S(i+n), adding means active every sigma-delta clock period for adding the contents of said counting means with the contents of said first register in order to compute the following coefficient C(n+1) to be loaded into said first register. Each computing means further includes multiplying means which is connected to said first register and which receives the train of sigma-delta pulses for computing at every period of the sigma-delta clock (fs) the product C(n)xS(i+n), and a second register which is continuously incremented by the result of said multiplying means.

Other preferred embodiment are recited in the dependent claims.

Description of the drawings.

Figure 1 shows the basic structure of a sigma-delta converter using a decimation filter.

Figure 2 shows illustrative spectra which are involved in the sigma-delta and decimation process.

Figure 3 is a table showing the variation of the signal-to-noise ratio with the frequency of the input signal fb and the oversampling frequency fs.

Figure 4 illustrates the evolution of the coefficients of the filter included into the present invention for a decimation factor of N = 10.

Figure 5 illustrates the decoding circuit 310 providing the required clocks.

Figure 6 shows the structure of a sigma-delta converter in accordance with the present invention.

Figure 7 are timing diagrams illustrating the operating of the invention.

Figure 8a and 8b show the structure of a double-loop sigma-delta converter which can be used with the decimation filter according to the present invention in order to carry out an efficient and simple analog-to-digital converter.

Figure 9a, 9b and 9c are timing diagrams showing the operating of the double-loop sigma-delta converter.

Description of the preferred embodiment of the invention.

The decimation circuit in accordance with the present invention simultaneously performs the filtering and decimation function by computing one filtered output over N samples in accordance with the following transfer function:

$$H(f) = \left(\frac{\sin(\frac{N\pi f}{f_s})}{N \sin(\frac{\pi f}{f_s})} \right)^3$$

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which is particularly well suited for decimation purposes. The coefficients of the digital filter results from the Z transfer function:

$$\begin{aligned} H(Z) &= \left(\frac{1 - Z^{-N}}{1 - Z^{-1}} \right)^3 && \text{(relation 1)} \\ &= (1 + Z^{-1} + \dots + Z^{-(N-1)})^3 \\ &= C_0 + C_1 Z^{-1} + \dots + C_{(3N-3)} Z^{-(3N-3)} \end{aligned}$$

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The computation of one PCM sample by the digital processing system included in the apparatus according to the present invention is performed with a set of $3N$ consecutive input samples $S(i)$. The PCM output sample is equal to

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$$\sum_{n=0}^{3N-1} C_n S_{i+n} \quad \text{(relation 2)}$$

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The coefficients used for the computation are given by the following formulae derived from the above relationship (2):

- For $n = 0 \dots N-1$ (W0 Window)

$$C_n = n \frac{(n+1)}{2}$$

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- For $n = N \dots 2N-1$ (W1 Window)

$$C_n = N \frac{(N+1)}{2} + (n - N)(2N - 1 - n)$$

- For $n = 2N \dots 3N-1$ (W2 Window)

$$C_n = (3N - n - 1) \frac{(3N - n)}{2}$$

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Let us call

$$\begin{aligned} C_{l+1} &= C_l + \Delta_l \\ \Delta_{l+1} &= \Delta_l + \delta_l \end{aligned}$$

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The following relations can be written:

- for $n = 0 \dots N-1$

$$C_n = n \frac{(n+1)}{2}$$

$$C_{n+1} = (n+1) \frac{(n+2)}{2}$$

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$$\Delta_n = n + 1$$

$$\delta_n = +1$$

- for $n = N \dots 2N-1$

$$C_n = N \frac{(N+1)}{2} + (n - N)(2N - 1 - n)$$

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$$C_{n+1} = N \frac{(N+1)}{2} + (n+1 - N)(2N - n - 2)$$

$$\Delta_n = 3N - 2n - 2$$

$$\delta_n = -2$$

- for $n = 2N \dots 3N-1$

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$$C_n = (3N - n - 1) \frac{(3N - n)}{2}$$

$$C_{n+1} = (3N - n - 2) \frac{(3N - n - 1)}{2}$$

$$\Delta_n = -3N + n + 1$$

$$\delta_n = +1$$

5 Therefore, it appears that the filtering coefficients can be divided in three distinctive groups which are characterized by important proprieties: the first group (or first window w0) where the difference between 2 consecutive coefficients is incremented by one at every step from 1 to N; the second group (window w1) where the difference between 2 consecutive coefficients is decremented by two at every step from N to 2xN-1; a third group (window w2) where the difference between 2 consecutive coefficients is incremented by one at every step from 2xN to 3xN-1. It should be noticed that this is absolutely independent of the value of the decimation factor N. Figure 4 illustrates the variation of the coefficients of the filtering function involved in the decimation circuit according to the present invention.

10 Figures 5 and 6 shows the decimation circuit of the sigma-delta converter in accordance with the present invention which successively computes the values of the coefficients C(n) from the generation of the value DELTA(i) in accordance with the following relationship:

$$C(i+1) = C(i) + \text{DELTA}(i)$$

As will appear hereinafter, the computing of the coefficients by means of the generation of the sequence of parameters DELTA(i) provides any desired value of the decimation factor.

20 Figure 6 is a detailed structure of the filtering and decimation device which receives a train of sigma-delta pulses on a INPUT SPL lead 301 and which converts it into PCM words on a PCM data bus 303. To achieve this, the device also receives the oversampling frequency clock fs (C) on a lead 300 and the PCM clock on a lead 302. The computation of one PCM sample is achieved by means of three separate calculations which are respectively performed by three corresponding computation blocks 350, 360 and 370, each computation block computing one PCM sample from a set of 3xN input samples received on lead 301. The computing blocks 350, 360 and 370 are respectively driven by a set of three phase-delayed clocks R0, R1 and R2 which are generated by a decoding circuit 310 receiving the PCM clock on lead 302 as shown in figure 5. Decoding circuit 310 respectively generates the set of three phase-delayed clocks R0, R1, R2 on a set of three leads 304, 305 and 306 at a frequency being one third of the value of the frequency of the PCM clock as shown in figure 7c, 7d, 7e and 7f. The use of the three computing blocks 350, 360 and 370 allows the whole generation of one PCM sample every N input samples S(i) which eventually provides a full down-sampling process with the desired decimation factor N.

The first computing block 350 includes a COEFF0 register 320 for storing the value of the coefficients C(n) which will be used in the filtering and decimation process, the latter register having an input bus connected to a corresponding output bus of an ADDER0 adding circuit 327. Block 350 further includes an ACCU0 accumulator 322 having an input bus connected to the output bus of ADDER0 adding circuit 327. As will be explained hereinafter, ADDER0 327 is alternatively used for computing the new calculated coefficient and also the partial PCM result: C0xSi + C1xS(i+1) + C2xS(i+2) ... in accordance with relation 3 above. A counter 311 receives the PCM clock on lead 302 at its Clock input and also the R0 clock at its reset input existing on lead 304. Counter 311 generates a control signal for a INCCTR0 counter 321 which is used for continuously generating the values of DELTA(i). The update of the contents of counter 321 is performed either by an incrementation of one, or a decrementation of two according to the state of the output of counter 311. The output bus of INCCTR0 counter 321 is connected to a first input bus of a MPX0 multiplexing circuit 324 having a second input bus which is connected to the output bus of accumulator 322. MPX0 multiplexor 324 is controlled by the oversampling clock fs (c) on lead 300. MPX0 multiplexing circuit 324 has an output bus which is connected to a first input bus of an ADDER0 adding circuit 327, which circuit 327 having a second input bus connected to the output bus of a XOR circuit block 323. XOR circuit block 323 is a set of XOR circuits, each having a first input connected to the output of a AND gate 326 and a second input connected to the corresponding lead of output bus of register 320. AND gate 326 has a first input which receives the oversampling clock fs (c) on lead 300 and a second input receiving the input sample of the train of sigma-delta pulses. The output of AND Gate 326 is also connected to the "Carry in" input of the ADDER0. The output of ACCU0 accumulator 322 is connected to the input of gates 325 which transmits the computed PCM sample every 3xN sigma-delta clock pulses at a first input of a set of OR gates 314. COEFF0 circuit 320, INCCTR0 counter 321, ACCU0 accumulator 322 and gates 325 receive the first R0 clock which is generated by decoding circuit 310 of figure 5. COEFF0 circuit 320, INCCTR0 counter 321 and ACCU0 accumulator also receive the oversampling clock c existing on lead 300.

55 Similarly, the second computing block 360 includes a COEFF1 register 330 for storing the value of the coefficients C(n) of the filtering/decimation process, the latter register having its inputs connected to the corresponding outputs of a ADDER1 adding circuit 337. Block 360 further includes an ACCU1 accumulator 332 having its input bus connected to the output bus of ADDER1 adding circuit 337. As will be described hereinafter,

ADDER1 337 is alternatively used for computing the new calculated coefficient and also the result of the computed value $C0xSi + C1xS(i+1) + C2xS(i+2)$ in accordance with the relation (3) above. A counter 312 receives the PCM clock on lead 302 at its Clock input and also the R1 clock which exists on lead 305. Counter 312 generates a control signal for a INCCTR1 counter 331 which continuously generates the sequence DELTA(i) which will be needed to compute the coefficients of the second computing block 360. The update of counter 331 is performed either by an incrementation of one, or a decrementation of two according to the state of the output of counter 312. The output bus of INCCTR1 counter 331 is connected to a first input bus of a MPX1 multiplexing circuit 334 having a second input bus connected to the output bus of accumulator 332 and which is controlled by the oversampling clock f_s (c) on lead 300. MPX1 multiplexing circuit 334 has an output bus which is connected to a first input bus of an ADDER1 adding circuit 337; circuit 337 has a second input bus connected to the output bus of a XOR circuit block 333. XOR circuit block 333 is a set of XOR circuits having each a first input connected to the output of a AND gate 336 and a second input connected to the corresponding lead of the output bus of register 330. AND gate 336 has a first input which receives the oversampling clock f_s (c) on lead 300 and a second input receiving the input sample coming from the sigma-delta converter. The output of AND gate 336 is also connected to the "Carry in" input of ADDER1. The output of ACCU1 accumulator 332 is connected to the input of gates 335 which output the PCM sample computed by block 360 every $3xN$ sigma-delta clock pulses and which is transmitted to a second input bus of set of OR gates 314. As for above, COEFF1 circuit 330, INCCTR1 counter 331, ACCU1 accumulator 332 and gates 335 receive the second R1 clock which is generated by decoding circuit 310 of figure 5. The COEFF1 circuit 330, INCCTR1 counter 331 and ACCU1 accumulator also receive the oversampling clock f_s (c) existing on lead 300.

Similarly, the third computing block 370 includes a COEFF2 register 340 for storing the value of the coefficients $C(n)$ needed for the filtering/decimation process of the third serie of $3xN$ input samples which is processed by computing block 370. Register 340 has an input bus which is connected to the output bus of an ADDER2 adding circuit 347. Block 370 further includes an ACCU2 accumulator 342 having its input bus connected to the output bus of ADDER2 adding circuit 347. As will be described hereinafter, ADDER2 347 is alternatively used for computing the new calculated coefficient and also the result of the computed value $C0xSi + C1xS(i+1) + C2xS(i+2) \dots$ in accordance with relation 3 above. A counter 313 receiving the PCM clock on lead 302 at its Clock input and also the R2 clock existing on lead 306 at its reset input generates a control signal for a INCCTR2 counter 341 which continuously generates the sequence of DELTA(i) needed to process the third set of $3xN$ input samples received by block 370. As for INCCTR0 and INCCTR1 counters, the update of delta in INCCTR2 block 341 is performed either by an incrementation of one, or a decrementation of two according to the state of the output line of counter 313. The output bus of INCCTR2 counter 341 is connected to a first input bus of a MPX2 multiplexing circuit 344 having a second input bus connected to the output bus of accumulator 342 and which is controlled by the c oversampling clock on lead 300. MPX2 multiplexing circuit 344 has an output bus which is connected to a first input bus of an ADDER2 adding circuit 347; circuit 347 has a second input bus connected to the output bus of a XOR circuit block 343. XOR circuit block 343 is a set of XOR circuits having each a first input connected to the output of a AND gate 346 and a second input connected to the corresponding lead of the output bus of register 340. AND gate 346 has a first input which receives the oversampling clock f_s (c) on lead 300 and a second input receiving the input sample coming from the sigma-delta converter. The output of AND gate 346 is connected to "Carry in" input of ADDER2. The output of ACCU2 accumulator 342 is connected to the input of gates 345 which outputs the desired PCM sample every $3xN$ sigma-delta clock period and which transmits it to a third input bus of a set of OR gates 314. Similarly than above, COEFF2 circuit 340, INCCTR2 counter 341, ACCU2 accumulator 342 and gates 345 receive the third R2 clock which is generated by decoding circuit 310 of figure 5. The COEFF2 circuit 340, INCCTR2 counter 341 and ACCU2 accumulator also receive the oversampling clock f_s (c) existing on lead 300.

The operating of the filtering/decimation circuit according to the present invention is as follows: Considering the first computing block 350: at every clock period of the oversampling clock f_s (c) existing on lead 300, counter 321 generates the following element of the sequence DELTA(i) illustrated in figure 4 by means of either an incrementation of one or a decrementation of two according to the state of the output of counter 311. Then, the update of the coefficient $c(n)$ is performed in register 320. To achieve this, during the first half of the oversampling clock period f_s (c) - i.e. when the f_s clock on lead 300 is at its low level- MPX0 multiplexing circuit 324 transmits the value DELTA(i) carried by the output bus of INCCTR0 counter 321 to the first input bus of ADDER0 circuit 327. The second input bus of ADDER0 circuit 327 receives the contents of COEFF0 register 320 via XOR 323 because the output of AND gate 326 is set to a low level since the oversampling clock f_s (c) on lead 300 is also at a low level. Similarly the input Carry in of ADDER0 is at a low level. ADDER0 circuit 327 therefore performs the computation: $c(n) = c(n-1) + DELTA(n-1)$ and the result $c(n)$ is stored into COEFF0 register 320 at the rising edge of the sigma-delta clock period, that is to say at the end of the first half of the sigma-delta clock period. During the second half of the oversampling clock period - i.e. when the latter clock is at a

high level -, MPX0 multiplexing circuit 324 transmits the contents of ACCU0 accumulator 322 to the first input bus of ADDER0 adding circuit 327 while its second input bus receives the output of XOR gates 323. XOR gates 323 transmit to ADDER0 adding circuit 327 the contents of COEFF0 register 320 or its inverse according to the value of the input sample SPL which is existing on lead 301 during the second half of the oversampling clock period. In the same time, the value of the input sample SPL is presented to ADDER0 Carry in input through AND gate 326. This provides a very simple way to achieve the computation of the term referred to in relation 2 above. Therefore, during that second half of the sigma-delta clock period, the input sigma-delta sample $S(i+n)$ on lead 301 is multiplied by the value of the coefficient $C(n)$ stored into register 320 and the result $C(n) \times S(i+n)$ is added to the contents of ACCU0 accumulator 322 by ADDER0 adding circuit 327. The result of the latter addition, i.e. the partial computation of the PCM sample $C(0) \times S(i) + C(1) \times S(i+1) + C(2) \times S(i+2) \dots$ is loaded into ACCU0 accumulator 322 on the falling edge of the oversampling clock f_s , i.e. at the end of the second half of the clock period of the sigma-delta clock f_s . The INCCTR0 counter 321 is used to continuously generate the sequence $\Delta(i)$ which is needed in the computation of the PCM sample by control block 350 and is controlled by counter 311 as follows: when the output of counter 311 is set to a low level, INCCTR0 counter 321 is incremented by one when the oversampling clock f_s (c) on lead 300 switches to a high level. Conversely, when the output of counter 311 is set to a high level, INCCTR0 counter 321 is decremented by two on the rising edge of the oversampling clock period on lead 300. The structure of INCCTR0 counter 321 is well known to the skilled man and will not be detailed. Therefore, INCCTR0 counter 321 stores at every clock period, and more accurately at every half of the oversampling clock period when the latter switches to a high level, the value of Δ which will be used to update the value of the coefficient needed to compute the PCM sample in accordance with the relation $C(n) = C(n-1) + \Delta(n-1)$. The latter update of the value of the coefficient $C(n)$ occurs during the first half of the next clock period. R0 clock generated by decoding circuit 310 of figure 5 is used to reset the different registers and counters: COEFF0 register 320, INCCTR0 counter 321, and counter 311 are reset when the R0 clock on lead 304 switches to a high level. Conversely, ACCU0 accumulator 322 is reset when the latter R0 clock switches to a low level. Moreover, counter 311 switches at every rising edge of the PCM clock on lead 302. Therefore, when the R0 clock on lead 304 switches to a high level, counter 311 is reset and its output is set to a low level: the INCCTR counter 321 is then incremented by one during a set of N oversampling clock period. At the next PCM pulse on lead 302, the output of counter 311 switches to a high level and INCCTR0 counter 321 is decremented by two during a set of N oversampling clock period. Similarly, at the next pulse of the PCM clock on lead 302, the output of counter 311 switches again to a low level and INCCTR0 counter 321 is incremented again by one during a set of N oversampling clock period. It appears that the contents of INCCTR0 counter 321 fully conforms to the diagram of figure 4 illustrating the variation of the value of $\Delta(i)$. Therefore, at the end of $3 \times N$ consecutive oversampling clock period, the ACCU0 accumulator 322 is loaded with the value of one PCM sample derived from the sigma-delta pulses according to the formula:

$$\sum_{n=0}^{3N-1} C_n S_{i+n}$$

The PCM sample is transmitted to the output of gates 325 at every pulse of the R0 clock and received at the first input of OR gates 314. Since a number of $3 \times N$ input samples have been required to generate the PCM output sample which was computed by block 350, the PCM samples generated by block 350 appear at a frequency of $f_s/3N$. Computing block 360 and 370 operates similarly to computing block 350 but are only phase-delayed since block 360 (or block 370) is driven by the phase-delayed R1 clock (or R2 clock) which is generated by decoding circuit 310 on lead 305. (or 306). Briefly, computing block 360 (or 370) operates as follows: at every clock period of the oversampling clock f_s (c) existing on lead 300, counter 331 (or 341) computes the new value of Δ under control of counter 312 (or 313). For this, during the first half of the oversampling clock period f_s (c), MPX1 multiplexing circuit 334 (or the MPX2 multiplexing circuit 344) transmits the value $\Delta(n-1)$ at the output of INCCTR1 counter 331 (or 341) to the first input bus of ADDER1 337 (or of ADDER2 347). The second input bus of ADDER1 337 (or ADDER2 347) receives the contents $C(n-1)$ of COEFF1 register 330 (or COEFF2 register 340) via XOR 333 (or 343) because the output of AND gate 336 (or 346) is set to a low level. Similarly, the "Carry in" input of ADDER1 (or of ADDER2) is at a low level. The ADDER1 circuit 337 (or ADDER2 circuit 347) performs the computation $c(n) = c(n-1) + \Delta(n-1)$. The result of the latter computation is stored again into COEFF1 register 330 (or the COEFF2 register 340) on the rising edge of the oversampling clock period f_s (c), i.e. at the end of the first half of that clock period. As for above, during the second half of the clock period, MPX1 multiplexing circuit 334 (or MPX2 multiplexing circuit 344) transmits the contents of ACCU1 accumulator 332 (or ACCU2 342) - carrying the partial result of the PCM sample computation

$C(0) \times S(i+1) + C(1) \times S(i+2) + C(2) \times S(i+3) + \dots$ (resp. $C(0) \times S(i+2) + C(1) \times S(i+3) + C(2) \times S(i+4) + \dots$) -to the first input bus of ADDER1 circuit 337 (resp. ADDER2 347) while its second input bus receives the output of XOR gates 333 (or XOR 343). In the same time the value of the input sample SPL is presented to ADDER1 (or ADDER2) "Carry in" input through AND gate 336 (or 346). Therefore, during the second half of the sigma-delta clock period, the input sigma-delta sample $S(i+n)$ on lead 301 is multiplied by the value of the coefficient $C(n)$ which has been computed before and stored into register 330 (or into register 340). The product $C(n) \times S(i+n)$ is added to the contents of ACCU1 accumulator 332 (or of ACCU2 accumulator 342) by ADDER1 circuit 337 (or by ADDER2 circuit 347). The result of the latter addition, corresponding to the partial result of the PCM sample computed by block 360 (or 370), is loaded into ACCU1 accumulator 332 (or ACCU2 accumulator 342) on the falling edge of the oversampling clock f_s (c), i.e. at the end of the second half of the clock period. The INCCTR1 counter 331 (as for INCCTR2 counter 341) is used to continuously generate the sequence $\Delta(n)$ needed to compute the coefficients $C(n)$, controlled by counter 312 (or counter 313) as follows: when the output of counter 312 (or of 313) is set to a low level, INCCTR1 counter 331 (or INCCTR2 counter 341) is incremented by one on the rising edge of the oversampling clock. Conversely, when the output of counter 312 (or of 313) is set to a high level, INCCTR1 counter 331 (or INCCTR2 counter 341) is decremented by two on the rising edge of the oversampling clock on lead 300. Therefore, INCCTR1 counter 331 (or INCCTR2 counter 341) stores on every rising edge of the oversampling clock the value of $\Delta(n)$, which will be used to compute the new coefficient $C(n)$. As for above, the latter update of the value of the coefficient $C(i)$ will occur during the first half of the next clock period. The R1 (or R2) clock generated by decoding circuit 310 of figure 5 is used to reset the different registers and counters: COEFF1 register 330, INCCTR1 counter 331 and counter 312 (or COEFF2 register 340, INCCTR2 counter 341 and counter 313) are reset at the rising edge of the R1 clock (or R2). On the other hand, ACCU1 accumulator 332 (or ACCU2 accumulator 342) is reset on the falling edge of the R1 clock (or R2 clock). Moreover, counter 312 (or 313) switches at every rising edge of the PCM clock on lead 302. Therefore, when the R1 clock (or R2 clock) switches to a high level, counter 312 (or 313) is reset and its output is low: the INCCTR1 counter 331 (or the INCCTR2 counter 341) is then incremented by one during a set of N oversampling clock period. At the next PCM pulse, the output of counter 312 (or 313) switches and INCCTR1 counter 331 (or INCCTR2 counter 341) is decremented by two during a following set of N oversampling clock period etc... Therefore, at the end of $3 \times N$ consecutive oversampling clock period, a PCM pulse is available in ACCU1 accumulator 332 (or ACCU2 accumulator 342). The latter PCM sample is transmitted to the second (or third) input of OR gate 314 by means of gates 335 (or 345) which are controlled by the R1 clock (or R2 clock).

As a conclusion, the set of three computing block 350, 360 and 370, each generating one PCM sample every $3 \times N$ input sample which is transmitting to one input of OR gate 314, produces a train of PCM samples at a frequency of f_s/N . The output of OR gate 314 is connected to the input of a register 315 which provides the PCM word on a PCM data bus 303 at the desired f_s/N frequency.

Figure 7 particularly illustrates the preceding operation by showing different timing diagrams which are involved in the filtering and decimation process when the decimation factor is equal to 4. There is also illustrated the continuous update process of INCCTR0 counter 321, COEFF0 register 320, INCCTR1 counter 331, COEFF1 register 330, INCCTR2 counter 341, and COEFF2 register 340. It clearly appears that the operation of each of the computing blocks 350, 360 or 370 is similar but phase-delayed with respect to the others.

Therefore, the decimation process can be easily preset and adjusted to predetermined parameters, i.e. the over-sampling rate and the decimation factor can be easily adjusted in a wide range in order to reach the necessary resolution for the PCM signal. It should be noticed that the filtering and decimation process operates whatever the value of the decimation factor is. This is simply achieved by using registers, adders, multiplexing circuits and accumulators having the appropriate size with respect to the higher value of the decimation factor desired. For instance, if the higher decimation factor which is desired is equal to N, the registers, adders, multiplexing circuits and accumulators should respectively be able to control N^3 values. The number of bits must be chosen accordingly. The set of computing blocks 350, 360 and 370 only requires the provision of the oversampling clock on lead 300, the train of sigma-delta pulses on lead 301 and the PCM clock on lead 302 which accurately indicates the instants when the PCM word resulting from the decimation process has to be delivered. The filtering and decimation device according to the present invention is particularly suited for a wide variety of different applications. Moreover, the adjustment of the decimation factor can be easily achieved only by adjusting the clocks which are entered into the coder.

A sigma-delta converter 101 which is particularly adapted to the filtering and decimation device according to the present invention is a first order or second-order converter such as shown in figure 8a and 8b.

Figure 8A illustrates an example of a double-loop sigma-delta converter according to the present invention which is embodied with discrete off the shelf analog components and which provides an actual signal-to-noise ratio close to its theoretical ratio, and also close to that provided by the corresponding sigma-delta converter

embodied in an integrated circuit with the switched capacitors technique. With respect to figure 8A, the DC component of the analog signal to be converted is suppressed by means of a capacitor 210. The resulting signal is transmitted to a first lead of a resistor 211 having a second lead respectively connected to the inverting input of an operational amplifier (OA) 214, to a first lead of a resistor 212 and to a first lead of a capacitor 213. The output of the operational amplifier 214 is connected to a second lead of capacitor 213 and to a first lead of a resistor 217 having a second lead respectively connected to the inverting input of a second operational amplifier 220, to a first lead of a resistor 218 and to a first lead of a capacitor 219. Operational amplifier 220 has its output lead connected to a second lead of capacitor 219 and to the D-input lead of a D-type latch 222 used as a threshold device. Latch 222, being a latch of the type 7474 well known in the art, provides at its output leads a sequence of voltages being either equal to 5 Volts (or V_{cc} more generally) or 0 Volt at the rhythm of an fs clock existing at its CK input lead. An example of a circuit for generating the fs clock will be described hereinafter with reference to figure 8B. A reference potential V_{ref} being equal to half the value of the positive supply voltage of latch 222 is transmitted to the non-inverting inputs of operational amplifiers 214 and 220 via a lead 216. The non-inverted Q output lead 223 of latch 222 is connected to a first input of a NOR gate 215 of the type 7402 well known by the skilled man having its second input lead receiving the fs clock and also an output lead connected to a second lead of resistor 212. The inverted output lead of latch 222 is connected to a first input of a NOR gate 221 which has its second input lead receiving the fs clock and also an output lead connected to a second lead of resistor 218. It appears that the feedback signal appearing at the output of NOR 215 is added to the analog input AC voltage to be converted and then integrated by means of the circuit formed by OA 214, resistors 211 and 212 and capacitor 213. Similarly, the feedback signal appearing at the output of NOR 221 is added to the signal at the output of OA 214 and integrated by means of the circuit based on OA 220, resistors 217 and 218, and capacitor 219. Thus the circuit of figure 2A has a double feedback loop similar to that of the architecture shown with respect to figure 1. The output Q of latch 222 provides a train of sigma-delta pulses which can be used to drive the decimation filter which has been described above.

The figure 8B shows a preferred embodiment of the fs sigma/delta clock generator in accordance with the preferred embodiment of the invention. A NOR gate 202, connected as an inverter, has its two input leads receiving a squared wave clock signal having the desired sigma-delta frequency. The output of NOR 202 is connected to a first lead of a resistor R 204, to a first lead of a resistor 203 having its second lead connected to the voltage supply (5 Volts in the preferred embodiment), and to a first input of a NOR gate 207. Resistor R 204 has a second input which is connected to a first input of a capacitor C 206 having a second lead connected to ground, and to the two input leads of a NOR gate 205, the output of which being connected to a second input of NOR 207. The output of NOR 207 eventually provides on a lead 208 the required fs clock. NOR gate 202 is used as an inverter and permits to supply enough current to drive the electronic components being connected.

Figures 9A, 9B and 9C respectively shows timing diagrams of the voltages existing on leads 208, 223 and 215. As illustrated in the figures, fs clock appears to be a train of pulses at the oversampling frequency, the pulses being very short and largely exaggerated on Fig. 3A. That train of pulses respectively transmitted to one input of NOR gates 215 and 221 in both feedback loops of the sigma-delta converter causes a return-to-zero of the output voltage of NOR 215 and NOR gate 221 at every rising edge of the fs clock. In this way, two adjacent "1" ("ONE") in the train of sigma-delta pulse on lead 223 causes the appearance of two pulses at the output of NOR 215. Therefore, the "weight" of two adjacent "1" will be exactly twice the "weight" of one "1", which was not the case in the conventional sigma-delta converter because of the asymmetry of the rise time and fall time of the converter. The linearity of the converter and its actual signal-to-noise ratio are substantially improved and reach those obtained by integrated sigma-delta converters which traditionally use the switched capacitor technique. The fs clock introduced in both feedback loops by means of NOR gates 215 and 216 entails the appearance in the sigma-delta code of a DC component proportional to the pulse width of fs clock. The latter DC component will be easily suppressed by traditional digital handling methods well known by the skilled man or still, by choosing appropriate values of resistor 204 and capacitor 206, so that RxC becomes negligible relative to the full period of the fs clock.

It should be noticed that the man skilled in the art will easily and straight forwardly embody the invention with a circuit in the feedback loops which generates a return-to-one at every raising edge of the fs clock.

It can be advantageous in some cases to choose a RxC value leading to a non-negligible pulse width in the fs clock. It has been discovered that if the latter width is not negligible the sigma-delta converter introduces an amplification step in the conversion process, the amplification being determined by the width of every pulse in fs clock. The width can be controlled by means of an adjustable resistor 204 or still by means of a digital circuit providing numerous clocks having the desired duty cycle form and associated with a switch (not shown) for selecting the appropriate clock. In the preferred embodiment of the invention, the sigma-delta converter is not associated with an amplification step. For that purpose, resistance R and capacitor C are chosen so that

the product RxC is negligible with respect to the full period of the f_s clock, according to the technology used.

However, it should be noticed that the filtering and decimation device according to the present invention could be used in any apparatus requiring a decimation and filtering process in accordance with relation 1 with a variable decimation factor, such as for instance spectrum analyzing devices having Fast Fourier Transformation (FFT) zoom capabilities.

Claims

1. Decimation filter for converting a train of sigma-delta pulses $S(i)$ in synchronism with a sigma-delta clock (f_s) into a train of Pulse Code Modulation (PCM) samples in accordance with the formula

$$\sum_{n=0}^{3N-1} C_n S_{i+n}$$

where C_n is the sequence of the coefficients of the decimation filter which corresponds to a determined decimation factor N ,

characterized in that it includes: computing means (350, 360, 370) further including:

- counting means (321, 331, 341) driven by said sigma-delta clock (f_s) and which is continuously incremented by one during N sigma-delta clock pulses, then decremented by two during N following sigma-delta clock pulses and then incremented again by one during N following sigma-delta clock pulses for generating an incrementation parameter ($\Delta(n)$),
- storing means (320, 330, 340) for storing the value of the coefficient $C(n)$ of said decimation filter to be multiplied by the next input sample $S(i+n)$ to be processed,
- means (327, 337, 347) active every sigma-delta clock period for incrementing said storing means (320, 330, 340) with said incrementation parameter ($\Delta(n)$),
- means (323, 327) for deriving from the contents $C(n)$ of said storing means (320, 330, 340) and from the train of input sigma-delta samples $S(i+n)$ one Pulse Code Modulation (PCM) sample every $3xN$ input sigma-delta samples.

2. Filtering and decimation device according to claim 1 characterized in that it includes three computing means (350, 360, 370) respectively driven by a set of three phase-delayed clocks derived from said sigma-delta clock (f_s), each of said computing means (350, 360, 370) computing one PCM sample from a sequence of $3xN$ consecutive input sigma-delta pulses.

3. Filtering and decimation device according to claim 1 or 2 characterized in that

- said counting means (321, 331, 341) has a control lead and performing an incrementation by one when said control lead is at a first logical level and conversely for performing a decrementation by two when said control lead is at a second logical level, and that each of said three computing means (350, 360, 370) includes:
- a first register (320, 330, 340) for storing the value $C(n)$ of the coefficient to be multiplied by the next sigma-delta input sample $S(i+n)$,
- adding means (327, 337, 347) active every sigma-delta clock period for adding the contents of said counting means with the contents of said first register (320, 330, 340) in order to compute the following coefficient $C(n+1)$ to be loaded into said first register (320, 330, 340).

4. Filtering and decimation device according to claim 3 characterized in that each of said three computing means (350, 360, 370) further includes

- multiplying means (323, 333, 343) connected to said first register (320, 330, 340) and receiving said train of sigma-delta pulses for computing at every period of the sigma-delta clock (f_s) the product $C(n) \times S(i+n)$,
- a second register (322, 332, 342) continuously incremented by the result of said multiplying means.

5. Filtering and decimation device according to claim 4 characterized in that in each of said three computing means (350, 360, 370), said adding means (327, 337, 347) is also used for computing the new coefficient $C(n+1)$ stored into said first register (320, 330, 340) and for incrementing said second register (322, 332,



the product RxC is negligible with respect to the full period of the f_s clock, according to the technology used.

However, it should be noticed that the filtering and decimation device according to the present invention could be used in any apparatus requiring a decimation and filtering process in accordance with relation 1 with a variable decimation factor, such as for instance spectrum analyzing devices having Fast Fourier Transformation (FFT) zoom capabilities.

Claims

1. Decimation filter for converting a train of sigma-delta pulses $S(i)$ in synchronism with a sigma-delta clock (f_s) into a train of Pulse Code Modulation (PCM) samples in accordance with the formula

$$\sum_{n=0}^{3N-1} C_n S_{i+n}$$

where C_n is the sequence of the coefficients of the decimation filter which corresponds to a determined decimation factor N ,

characterized in that it includes: computing means (350, 360, 370) further including:

- counting means (321, 331, 341) driven by said sigma-delta clock (f_s) and which is continuously incremented by one during N sigma-delta clock pulses, then decremented by two during N following sigma-delta clock pulses and then incremented again by one during N following sigma-delta clock pulses for generating a incrementation parameter ($\Delta(n)$),
- storing means (320, 330, 340) for storing the value of the coefficient $C(n)$ of said decimation filter to be multiplied by the next input sample $S(i+n)$ to be processed,
- means (327, 337, 347) active every sigma-delta clock period for incrementing said storing means (320, 330, 340) with said incrementation parameter ($\Delta(n)$),
- means (323, 327) for deriving from the contents $C(n)$ of said storing means (320, 330, 340) and from the train of input sigma-delta samples $S(i+n)$ one Pulse Code Modulation (PCM) sample every $3xN$ input sigma-delta samples.

2. Filtering and decimation device according to claim 1 characterized in that it includes three computing means (350, 360, 370) respectively driven by a set of three phase-delayed clocks derived from said sigma-delta clock (f_s), each of said computing means (350, 360, 370) computing one PCM sample from a sequence of $3xN$ consecutive input sigma-delta pulses.

3. Filtering and decimation device according to claim 1 or 2 characterized in that

- said counting means (321, 331, 341) has a control lead and performing a incrementation by one when said control lead is at a first logical level and conversely for performing a decrementation by two when said control lead is at a second logical level, and that each of said three computing means (350, 360, 370) includes:
- a first register (320, 330, 340) for storing the value $C(n)$ of the coefficient to be multiplied by the next sigma-delta input sample $S(i+n)$,
- adding means (327, 337, 347) active every sigma-delta clock period for adding the contents of said counting means with the contents of said first register (320, 330, 340) in order to compute the following coefficient $C(n+1)$ to be loaded into said first register (320, 330, 340).

4. Filtering and decimation device according to claim 3 characterized in that each of said three computing means (350, 360, 370) further includes

- multiplying means (323, 333, 343) connected to said first register (320, 330, 340) and receiving said train of sigma-delta pulses for computing at every period of the sigma-delta clock (f_s) the product $C(n) \times S(i+n)$,
- a second register (322, 332, 342) continuously incremented by the result of said multiplying means.

5. Filtering and decimation device according to claim 4 characterized in that in each of said three computing means (350, 360, 370), said adding means (327, 337, 347) is also used for computing the new coefficient $C(n+1)$ stored into said first register (320, 330, 340) and for incrementing said second register (322, 332,



342).

6. Filtering and decimation device according to claim 5 characterized in that each of said three computing means (350, 360, 370) further includes

- 5 - multiplexing means (324, 334, 344) having a first input bus connected to the output bus of said second register (322, 332, 342) and a second input bus connected to the output of said counting means (321, 331, 341), said multiplexing means being controlled by said sigma-delta clock,
- 10 - XOR gating means (323, 333, 343) having one input connected to the output of a AND gate (326, 336, 346) receiving the input train of sigma-delta pulses and also the sigma-delta clock, said XOR gating means (323, 333, 343) having a second input bus connected to the output bus of said first register (320, 330, 340),
and that said adding means (327, 337, 347) has a first input bus connected to the output of said multiplexing means and a second input bus connected to the output of said XOR gating means (323, 333, 343), the output bus of said adding means being connected to the input of said first and said
15 second register,
whereby said adding means performs the computation of $c(n) + \Delta(i)$ during one half of said sigma-delta clock period and the update of said second register during the second half of said sigma-delta clock period.

- 20 7. Analog-to-digital converter including a sigma-delta converter (101) of the first or second order characterized by the filtering and decimation device of claims 1-6

8. Analog-to-digital converter according to claim 7 characterized in that said sigma-delta converter includes

- 25 - a threshold device (222) for generating an output and feedback signal,
- a filter (214, 220) receiving the analog input signal to be converted and said output and feedback signal by means of at least one feedback loop,
- means (215, 221) located in said at least one feedback loop for performing a return-to-specified-logical-state of the sigma-delta code generated by said threshold device at every period of the sigma-delta clock thereby making the sigma-delta converter insensitive to the rise and fall time of the threshold device.

9. Analog-to-digital converter according to claim 8 characterized in that said sigma-delta converter further includes:

- 35 - a first integrator (214, 213, 211, 212) receiving said analog input signal to be converted and a first feedback signal coming from a first feedback loop,
- a second integrator (220, 217, 218, 219) receiving the analog output of said first integrator and a second feedback signal coming from a second feedback loop and having an output lead connected to said threshold device,
- 40 - first means (215, 208) for performing a return-to-zero of the feedback signal conveyed through said first feedback loop to said first integrator,
- second means (221, 208) for performing a return-to-zero of the feedback signal conveyed through said second feedback loop to said second integrator.

- 45 10. Data circuit terminating equipment (DCE) characterized by the analog-to-digital converter according to claims 7, 8 or 9.

Patentansprüche

- 50 1. Dezimationsfilter zum Konvertieren einer Folge von Sigma-Delta-Impulsen $S(i)$ synchron mit einem Sigma-Delta-Takt (f_s) in eine Folge von Impulsen mit Pulsmodulation (PCM) gemäß der Formel

55
$$\sum_{n=0}^{3N-1} C_n S_{i+n}$$

wobei C_n die Koeffizientenfolge des Dezimationsfilters ist, die einem vorherbestimmten Dezimationsfak-



tor N entspricht,

dadurch gekennzeichnet, daß es folgendes umfaßt:

Berechnungsmittel (350, 360, 370), das weiterhin folgendes umfaßt:

- 5 - Zählmittel (321, 331, 341), das durch den Sigma-Delta-Takt (f_s) getrieben und während N Impulsen des Sigma-Delta-Taktes fortlaufend um eins erhöht wird, dann während N folgenden Impulsen des Sigma-Delta-Taktes um zwei vermindert wird und dann wieder während N folgenden Impulsen des Sigma-Delta-Taktes um eins erhöht wird, um einen Inkrementierungsparameter ($\Delta(n)$) zu erzeugen,
- 10 - Speichermittel (320, 330, 340) zum Speichern des Wertes des Koeffizienten $C(n)$ des Dezimationsfilters, der mit dem nächsten Eingangsimpuls $S(i+n)$ zu multiplizieren ist, um verarbeitet zu werden,
- 15 - Mittel (327, 337, 347), das zu jeder Periode des Sigma-Delta-Taktes aktiv ist, um das Speichermittel (320, 330, 340) um den Inkrementierungsparameter ($\Delta(n)$) zu erhöhen,
- Mittel (323, 327), um alle $3 \times N$ Sigma-Delta-Eingangsimpulse einen Pulsmodulations(PCM)-Impuls aus dem Inhalt $C(n)$ des Speichermittels (320, 330, 340) und aus der Folge von Sigma-Delta-Eingangsimpulsen $S(i+n)$ abzuleiten.

2. Filter- und Dezimationseinheit gemäß Anspruch 1, dadurch gekennzeichnet, daß sie drei Berechnungsmittel (350, 360, 370) umfaßt, die jeweils durch einen Satz von drei phasenverzögerten Takten getrieben werden, die von dem Sigma-Delta-Takt (f_s) abgeleitet werden, wobei jedes der Berechnungsmittel (350, 360, 370) einen PCM-Impuls aus einer Folge von $3 \times N$ aufeinanderfolgenden Sigma-Delta-Eingangsimpulsen berechnet.

3. Filter- und Dezimationseinheit gemäß Anspruch 1 oder 2, dadurch gekennzeichnet, daß
- 25 - das Zählmittel (321, 331, 341) eine Steuerführung aufweist und eine Inkrementierung um eins ausführt, wenn sich die Steuerführung auf einer ersten logischen Stufe befindet, und umgekehrt eine Dekrementierung um zwei ausführt, wenn sich die Steuerführung auf einer zweiten logischen Stufe befindet, und daß jedes der drei Berechnungsmittel (350, 360, 370) folgendes umfaßt:
 - 30 - ein erstes Register (320, 330, 340) zum Speichern des Wertes $C(n)$ des Koeffizienten, der mit dem nächsten Sigma-Delta-Eingangsimpuls $S(i+n)$ zu multiplizieren ist,
 - Additionsmittel (327, 337, 347), das zu jeder Periode des Sigma-Delta-Taktes aktiv ist, um den Inhalt des Zählmittels zu dem Inhalt des ersten Registers (320, 330, 340) zu addieren, um den folgenden Koeffizienten $C(n+1)$ zu berechnen, der in das erste Register (320, 330, 340) zu laden ist.

4. Filter- und Dezimationseinheit gemäß Anspruch 3, dadurch gekennzeichnet, daß jedes der drei Berechnungsmittel (350, 360, 370) weiterhin folgendes umfaßt:
- 35 - Multiplikationsmittel (323, 333, 343), das mit dem ersten Register (320, 330, 340) verbunden ist und die Folge von Sigma-Delta-Impulsen empfängt, um zu jeder Periode des Sigma-Delta-Taktes (f_s) das Produkt $C(n) \times S(i+n)$ zu berechnen,
 - 40 - ein zweites Register (322, 332, 342), das fortlaufend um das Ergebnis des Multiplikationsmittels erhöht wird.

5. Filter- und Dezimationseinheit gemäß Anspruch 4, dadurch gekennzeichnet, daß in jedem der drei Berechnungsmittel (350, 360, 370) das Additionsmittel (327, 337, 347) auch für das Berechnen des neuen Koeffizienten $C(n+1)$, der in dem ersten Register (320, 330, 340) gespeichert wird, und für das Inkrementieren des zweiten Registers (322, 332, 342) verwendet wird.

6. Filter- und Dezimationseinheit gemäß Anspruch 5, dadurch gekennzeichnet, daß jedes der drei Berechnungsmittel (350, 360, 370) weiterhin folgendes umfaßt:
- 50 - Multiplexmittel (324, 334, 344), das einen ersten Eingangsbus aufweist, der mit dem Ausgangsbus des zweiten Registers (322, 332, 342) verbunden ist, und einen zweiten Eingangsbus, der mit dem Ausgang des Zählmittels (321, 331, 341) verbunden ist, wobei das Multiplexmittel durch den Sigma-Delta-Takt gesteuert wird,
 - 55 - XOR-Verknüpfungsmittel (323, 333, 343), das einen Eingang aufweist, der mit dem Ausgang eines UND-Gatters (326, 336, 346) verbunden ist, welches die Eingangsfolge der Sigma-Delta-Impulse sowie des Sigma-Delta-Taktes empfängt, wobei das XOR-Verknüpfungsmittel (323, 333, 343) einen zweiten Eingangsbus aufweist, der mit dem Ausgangsbus des ersten Registers (320, 330, 340) verbunden ist, und daß das Additionsmittel (327, 337, 347) einen ersten Eingangsbus aufweist, der mit dem Aus-



gang des Multiplexmittels verbunden ist, und einen zweiten Eingangsbus, der mit dem Ausgang des XOR-Verknüpfungsmittels (323, 333, 343) verbunden ist, wobei der Ausgangsbus des Additionsmittels mit dem Eingang des ersten und des zweiten Registers verbunden ist, wobei das Additionsmittel die Berechnung von $c(n) + \text{DELTA}(i)$ während einer Hälfte der Periode des Sigma-Delta-Taktes und die Aktualisierung des zweiten Registers während der zweiten Hälfte der Periode des Sigma-Delta-Taktes ausführt.

7. Analog-Digital-Konverter, der einen Sigma-Delta-Konverter (101) erster oder zweiter Ordnung enthält, gekennzeichnet durch die Filter- und Dezimationseinheit der Ansprüche 1 bis 6.
8. Analog-Digital-Konverter gemäß Anspruch 7, dadurch gekennzeichnet, daß der Sigma-Delta-Konverter folgendes umfaßt:
 - eine Schwelleneinheit (222) zur Erzeugung eines Ausgangs- und Rückkopplungssignals,
 - ein Filter (214, 220), welches das zu konvertierende analoge Eingangssignal und das Ausgangs- und Rückkopplungssignal mittels zumindest einer Rückkopplungsschleife empfängt,
 - Mittel (215, 221), das in der zumindest einen Rückkopplungsschleife angeordnet ist, um eine "Rückkehr zum vorgegebenen logischen Status" des Sigma-Delta-Codes auszuführen, der von der Schwelleneinheit zu jeder Periode des Sigma-Delta-Taktes erzeugt wird, wodurch der Sigma-Delta-Konverter unempfindlich gegen die Anstiegs- und Abfallzeit der Schwelleneinheit gemacht wird.
9. Analog-Digital-Konverter gemäß Anspruch 8, dadurch gekennzeichnet, daß der Sigma-Delta-Konverter weiterhin folgendes umfaßt:
 - ein erstes Integrierglied (214, 213, 211, 212), welches das umzuwandelnde analoge Eingangssignal und ein erstes Rückkopplungssignal empfängt, das von einer ersten Rückkopplungsschleife kommt,
 - ein zweites Integrierglied (220, 217, 218, 219), welches das analoge Ausgangssignal des ersten Integriergliedes und ein zweites Rückkopplungssignal, das von einer zweiten Rückkopplungsschleife kommt, empfängt, und eine Ausgangsleitung aufweist, die mit der Schwelleneinheit verbunden ist,
 - erstes Mittel (215, 208) zum Ausführen einer Rückkehr-zu-Null des Rückkopplungssignals, das durch die erste Rückkopplungsschleife zu dem ersten Integrierglied übertragen wird,
 - zweites Mittel (221, 208) zum Ausführen einer Rückkehr-zu-Null des Rückkopplungssignals, das durch die zweite Rückkopplungsschleife zu dem zweiten Integrierglied übertragen wird.
10. Datenübertragungseinrichtung (DÜE), gekennzeichnet durch den Analog-Digital-Konverter gemäß der Ansprüche 7, 8 oder 9.

Revendications

1. Filtre de décimation pour convertir un train d'impulsions sigma-delta $S(i)$ en synchronisme avec une horloge sigma-delta (f_s) en un train d'échantillons à modulation par impulsions codées (PCM) en fonction de la formule

$$\sum_{n=0}^{3N-1} C_n S_{i+n}$$

où C_n est la séquence des coefficients du filtre de décimation qui correspond à un facteur de décimation déterminé N ,

- caractérisé en ce qu'il comporte: un moyen de calcul (350, 360, 370) comportant en outre:
- un moyen de comptage (321, 331, 341) entraîné par ladite horloge sigma-delta (f_s) et qui est incrémenté en continu de un au cours de N impulsions d'horloge sigma-delta, puis décrétementé de deux au cours des N impulsions d'horloge suivantes sigma-delta puis incrémenté à nouveau de un au cours des N impulsions d'horloge suivantes sigma-delta pour générer un paramètre d'incrémentatation ($\text{DELTA}(n)$),
 - un moyen de stockage (320, 330, 340) pour stocker la valeur du coefficient $C(n)$ dudit filtre de décimation pour le multiplier par l'échantillon d'entrée suivant $S(i+n)$ à traiter,
 - un moyen (327, 337, 347) actif à chaque période d'horloge sigma-delta pour incrémenter ledit moyen



de stockage (320, 330, 340) avec ledit paramètre d'incrémentation ($\Delta(n)$),

- un moyen (323, 327) pour obtenir à partir du contenu $C(n)$ dudit moyen de stockage (320, 330, 340) et à partir du train d'échantillons d'entrée sigma-delta $S(i+n)$ un échantillon à modulation par impulsions codées (PCM) à chaque $3 \times N$ échantillon d'entrée sigma-delta.

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2. Dispositif de filtrage et de décimation selon la revendication 1 caractérisé en ce qu'il comporte trois moyens de calcul (350, 360, 370) respectivement entraînés par une série de trois horloges à retard de phase obtenues à partir de ladite horloge sigma-delta (f_s), chacun desdits moyens de calcul (350, 360, 370) calculant un échantillon PCM à partir d'une séquence de $3 \times N$ impulsions sigma-delta d'entrée consécutives.

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3. Dispositif de filtrage et de décimation selon la revendication 1 ou 2 caractérisé en ce que
 - ledit moyen de comptage (321, 331, 341) comporte un conducteur de commande et effectuant une incrémentation de un lorsque ledit conducteur de commande est à un premier niveau logique et inversement pour effectuer une décrémentation de deux lorsque ledit conducteur de commande est à un second niveau logique, et en ce que chacun desdits moyens de calcul (350, 360, 370) comporte:
 - un premier registre (320, 330, 340) pour stocker la valeur $C(n)$ du coefficient à multiplier par l'échantillon suivant sigma-delta d'entrée $S(i+n)$,
 - un moyen d'addition (327, 337, 347) actif à chaque période d'horloge sigma-delta pour ajouter les contenus dudit moyen de comptage avec les contenus dudit premier registre (320, 330, 340) afin de calculer le coefficient suivant $C(n+1)$ à charger dans ledit premier registre (320, 330, 340).

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4. Dispositif de filtrage et de décimation selon la revendication 3, caractérisé en ce que chacun desdits trois moyens de calcul (350, 360, 370) comporte en outre
 - un moyen de multiplication (323, 333, 343) connecté audit premier registre (320, 330, 340) et recevant ledit train d'impulsions sigma-delta et calculant à chaque période de l'horloge sigma-delta (f_s) le produit $C(n) \times S(i+n)$,
 - un second registre (322, 332, 342) incrémenté en continu par le résultat dudit moyen de multiplication.

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5. Dispositif de filtrage et de décimation selon la revendication 4, caractérisé en ce que chacun desdits trois moyens de calcul (350, 360, 370), ledit moyen d'addition (327, 337, 347) est aussi utilisé pour calculer le nouveau coefficient $C(n+1)$ stocké dans ledit premier registre (320, 330, 340) et pour incrémenter ledit second registre (322, 332, 342).

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6. Dispositif de filtrage et de décimation selon la revendication 5 caractérisé en ce que chacun desdits trois moyens de calcul (350, 360, 370) comporte en outre
 - un moyen de multiplexage (324, 334, 344) ayant un premier bus d'entrée connecté au bus de sortie dudit second registre (322, 332, 342) et un second bus d'entrée connecté à la sortie dudit moyen de comptage (321, 331, 341), ledit moyen de multiplexage étant commandé par ladite horloge sigma-delta,
 - un moyen à porte OU exclusive (323, 333, 343) ayant une entrée connectée à la sortie d'une porte ET (326, 336, 346) recevant le train d'entrée des impulsions sigma-delta et aussi l'horloge sigma-delta, ledit moyen à porte OU exclusive (323, 333, 343) ayant un second bus d'entrée connecté au bus de sortie dudit premier registre (320, 330, 340),
 - et en ce que ledit moyen d'addition (327, 337, 347) a un premier bus d'entrée connecté à la sortie dudit moyen de multiplexage et un second bus d'entrée connecté à la sortie dudit moyen à porte OU exclusive (323, 333, 343), le bus de sortie dudit moyen d'addition étant connecté à l'entrée desdits premier et second registres,
 - grâce à quoi ledit moyen d'addition effectue le calcul de $c(n) + \Delta(i)$ au cours de la moitié de la période d'horloge sigma-delta et la mise à jour dudit second registre au cours de la seconde moitié de ladite période d'horloge sigma-delta.

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7. Convertisseur analogique-numérique comportant un convertisseur sigma-delta (101) du premier ou du second ordre caractérisé par le dispositif de filtrage et de décimation des revendications 1-6.
8. Convertisseur analogique-numérique selon la revendication 7 caractérisé en ce que ledit convertisseur sigma-delta comporte



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- un dispositif à seuil (222) pour générer une sortie et un signal de contre-réaction,
 - un filtre (214, 220) recevant le signal d'entrée analogique à convertir et ledit signal de sortie et de contre-réaction au moyen d'au moins une boucle de contre-réaction,
 - un moyen (215, 221) situé dans ladite au moins une boucle de contre-réaction pour effectuer un retour à l'état logique spécifié du code sigma-delta généré par ledit dispositif à seuil à chaque période de l'horloge sigma-delta afin de rendre le convertisseur sigma-delta insensible au temps de montée et de descente du dispositif à seuil.

10 9. Convertisseur analogique-numérique selon la revendication 8 caractérisé en ce que ledit convertisseur sigma-delta comporte en outre:

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- un premier intégrateur (214, 213, 211, 212) recevant ledit signal d'entrée analogique à convertir et un premier signal de contre-réaction en provenance d'une première boucle de contre-réaction,
 - un second intégrateur (220, 217, 218, 219) recevant la sortie analogique dudit premier intégrateur et un second signal de contre-réaction en provenance d'une seconde boucle de contre-réaction et ayant un conducteur de sortie connecté audit dispositif à seuil,
 - un premier moyen (215, 208) pour effectuer un retour à zéro du signal de contre-réaction transporté par l'intermédiaire de ladite première boucle de contre-réaction vers ledit premier intégrateur,
 - un second moyen (221, 208) pour effectuer un retour à zéro du signal de contre-réaction transporté par l'intermédiaire de ladite seconde boucle de contre-réaction vers ledit second intégrateur.
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10. Equipement terminal à circuit de données (DCE) caractérisé par le convertisseur analogique-numérique selon les revendications 7, 8 ou 9.

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