What is Claimed is:

1. A semiconductor device, comprising:

a substrate;

a first conductive type first doping area formed in a first conductive type well region in the substrate;

a second conductive type second doping area formed in the first conductive type well region in the substrate and spaced apart from the first conductive type first doping area;

a second conductive type deep well region formed below the first conductive type first doping area; and

a second conductive type highly-doped area formed in the second conductive type deep well region;

a source region formed in the first conductive type first doping area;

a drain region formed in the second conductive type second doping area;

a gate insulating film formed between the source region and the drain region, comprising:

a thin gate insulating film formed closer to the source region than the drain region;

a thick gate insulating film formed to closer to the drain region than the source region; and

a connecting insulating film disposed between the thin gate insulating film and the thick gate insulating film, and a thickness of the connecting insulating film being varied from a thickness of the thin gate insulating film and to a thickness of the thick gate insulating film; and

a gate electrode formed on the gate insulating film,

wherein a lower surface of the thin gate insulating film and a lower surface of the thick gate insulating film are coplanar, and the gate electrode covers more than half a length of the thick gate insulating film.

2. The semiconductor device according to claim 1, wherein an upper surface of the connecting insulating film has a slope, and each upper side of the thin gate insulating film and the thick gate insulating film is coplanar.

3. The semiconductor device according to claim 1, wherein the first conductive type first doping area is formed extended to a partial area of the thin gate insulating film in a direction of the source region to the drain region.

4. The semiconductor device according to claim 1, wherein the second conductive type second doping area is formed extended to a partial area of the thin gate insulating film in a direction of the drain region to the source region.

5. The semiconductor device according to claim 1, wherein the second conductive type second doping area is formed extended only to a partial area of the thick gate insulating film in a direction of the drain region to the source region.

6. The semiconductor device according to claim 1, wherein the second conductive type second doping area passes through the thick gate insulating film to extend to a partial area of the connecting insulating film in a direction of the drain region to the source region.

7. The semiconductor device according to claim 1, wherein the connecting insulating film connects the thin gate insulating film and the thick gate insulating film to each other.

8. The semiconductor device according to claim 1, wherein the drain region is spaced apart from the thick gate insulating film.

9. The semiconductor device according to claim 1, further comprising:

a silicide formed on the gate electrode, the source region, and the drain region.

10. The semiconductor device according to claim 1, further comprising an isolation region formed in the substrate and having a deeper depth from an upper surface of the substrate than the first conductivity type first doping area.

11. The semiconductor device according to claim 1, wherein the first conductivity type first doping area has a depth equal to a depth of the second conductivity type second doping area when measured from an upper surface of the substrate.

12. The semiconductor device according to claim 1, further comprising:

a silicide blocking insulating film disposed between the drain region and the thick gate insulating film,

wherein the silicide blocking insulating film contacts an upper side of the substrate.

13. The semiconductor device according to claim 12, wherein the second conductive type second doping area contacts the silicide blocking insulating film.

14. A method of manufacturing a semiconductor device, the method comprising:

forming a first conductive type first well region in a substrate;

forming a first gate insulating film on the first conductive type first well region, the first gate insulating film comprising a thin gate insulating film, a thick gate insulating film and a connecting insulating film connecting the thin gate insulating film and the thick gate insulating film, wherein a lower surface of the thin gate insulating film and a lower surface of the thick gate insulating film are coplanar to each other;

forming a first gate electrode on the first gate insulating film;

forming a source region and a drain region in the substrate,

forming a first conductive type second well region to be spaced apart from the first conductive type first well region;

forming a second conductive type first drift region in the first conductive type second well region; and

forming a second gate insulating film on the first conductive type second well region having similar thickness to the thickness of the thick gate insulating film,

wherein the thin gate insulating film is formed closer to the source region than the drain region, the thick gate insulating film is formed closer to the drain region than the source region, and the connecting insulating film is disposed between the thin gate insulating film and the thick gate insulating film, and

wherein a thickness of the connecting insulating film varies from a thickness of the thin gate insulating film and to a thickness of the thick gate insulating film.

15. The method of manufacturing the semiconductor device of claim 14, further comprising:

forming a first conductive type third well region to be spaced apart from the first conductive type first well region; and

forming a third gate insulating film in the first conductive type third well region having similar thickness to the thickness of the thin gate insulating film.

16. The method of claim 14, wherein the forming of the first conductive type first well region and the forming of the first conductive type second well region are simultaneously performed, and

wherein the forming of the thick gate insulating film of the first gate insulating film

and the forming of the second gate insulating film are simultaneously performed.

17. The method of claim 14, further comprising:

simultaneously forming a second conductive type second drift region in the first conductive type second well region while forming the second conductivity type first drift region; and

simultaneously forming a second gate electrode on the second gate insulating film while forming the first gate electrode.

18. The method of claim 14, further comprising:

forming a second conductive type deep well region formed in the substrate; and

forming a second conductive type highly-doped area formed in the second conductive type deep well region.

19. The method of claim 14, further comprising forming a first conductive type first doping area and a second conductive type second doping area in the first conductive type first well region.

20. The method of claim 19, wherein the source region and the drain region are formed in the first conductive type first doping area and the second conductive type second doping area, respectively.

21. A semiconductor device, comprising:

a first conductive type first well region in a substrate;

a first gate insulating film on the first conductive type first well region, the first gate insulating film comprising a thin gate insulating film, a thick gate insulating film and a connecting insulating film connecting the thin gate insulating film and the thick gate insulating film, wherein a lower surface of the thin gate insulating film and a lower surface of the thick gate insulating film are coplanar to each other;

a first gate electrode on the first gate insulating film;

a source region and a drain region in the substrate;

a first conductive type second well region spaced apart from the first conductive type first well region;

a second conductive type first drift region in the first conductive type second well region; and

a second gate insulating film on the first conductive type second well region having

a thickness similar to that of the thick gate insulating film,

wherein the thin gate insulating film is formed closer to the source region than the drain region, the thick gate insulating film is formed closer to the drain region than the source region, and the connecting insulating film is disposed between the thin gate insulating film and the thick gate insulating film, and

wherein a thickness of the connecting insulating film varies from a thickness of the thin gate insulating film and to a thickness of the thick gate insulating film.

22. The semiconductor device of claim 21, further comprising:

a second conductive type deep well region formed below the first conductive type first well region; and

a second conductive type highly-doped area formed in the second conductive type deep well region.

23. The semiconductor device of claim 21, further comprising:

a first conductive type third well region spaced apart from the first conductive type first well region; and

a third gate insulating film formed on the first conductive type third well region having a thickness similar to that of the thin gate insulating film.

24. The semiconductor device of claim 21, further comprising:

a second conductive type second drift region formed in the first conductive type second well region; and

a second gate electrode formed on the second gate insulating film.

25. The semiconductor device of claim 21, further comprising a first conductive type first doping area and a second conductive type second doping area formed in the first conductive type first well region.

26. The semiconductor device of claim 25, wherein the source region and the drain region are formed in the first conductive type first doping area and the second conductive type second doping area, respectively.