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SEMICONDUCTOR DEVICES INCLUDING STAIR STEP STRUCTURES,  
AND RELATED METHODS

PRIORITY CLAIM

5           This application claims the benefit of the filing date of United States Patent Application Serial Number 13/932,551, filed July 1, 2013, for “SEMICONDUCTOR DEVICES INCLUDING STAIR STEP STRUCTURES, AND RELATED METHODS.”

## 10 TECHNICAL FIELD

Embodiments of the present disclosure relate to apparatuses such as three-dimensional semiconductor devices that include stair step structures defining contact regions, and related methods of forming and of operating such semiconductor devices.

15 BACKGROUND

The semiconductor industry has continually sought ways to produce memory devices with an increased number of memory cells per memory die. In non-volatile memory (e.g., NAND flash memory), one way to increase memory density is by using a vertical memory array, which is also referred to as a three-dimensional (3-D) memory array. One type of vertical memory array includes semiconductor pillars that extend through openings (e.g., holes) in tiers (e.g., layers, plates) of conductive material (e.g., word line plates, control gate plates), with dielectric materials at each junction of the semiconductor pillars and the conductive materials. Thus, multiple transistors can be formed along each pillar. Vertical memory array structures enable a greater number of transistors to be located in a unit of die area by building the array upwards (e.g., vertically) on a die, as compared to structures with conventional planar (e.g., two-dimensional) arrangements of transistors.

Vertical memory arrays and methods of forming them are described in, for  
30 example, U.S. Patent Application Publication No. 2007/0252201 of Kito et al.;  
Tanaka et al., “Bit Cost Scalable Technology with Punch and Plug Process for Ultra  
High Density Flash Memory,” Symposium on VLSI Technology Digest of  
Technical Papers, pp. 14-15 (2007); Fukuzumi et al., “Optimal Integration and

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Characteristics of Vertical Array Devices for Ultra-High Density, Bit-Cost Scalable Flash Memory,” IEDM Technical Digest, pp. 449-52 (2007); and Endoh et al., “Novel Ultrahigh-Density Flash Memory with a Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell,” IEEE Transactions on Electron Devices, 5 vol. 50, no. 4, pp. 945-951 (Apr., 2003).

Conventional vertical memory arrays include an electrical connection between the conductive materials (e.g., word line plates) and access lines (e.g., word lines) so that memory cells in the 3-D array may be uniquely selected for writing, reading, or erasing operations. One method of forming an electrical connection 10 includes forming a so-called “stair step” structure at an edge of the conductive materials. The stair step structure includes individual “steps” that define contact regions over which a vertical conductor is formed to provide electrical access to the respective conductive materials.

Further improvements and reductions in cost in the manufacturing of such 15 structures, as well as alternative structures and methods for reducing an area covered by the stair step vertical memory arrays, are desired. In addition, improvements in the formation of structures including a higher number of memory cells and conductive tiers are desired.

## 20 BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a partially cutaway perspective view of a semiconductor device structure that includes a conventional stair step structure.

FIG. 2 illustrates a top view of a portion of a semiconductor device structure showing two elongated memory array blocks and a conventional stair step structure at a 25 longitudinal end of each of the elongated memory array blocks.

FIGS. 3 through 5 illustrate different views of a memory array block of a semiconductor device structure according to an embodiment of the present disclosure.

FIG. 3 illustrates a perspective view of the memory array block including four stair step structures according to an embodiment of the present disclosure.

30 FIG. 4 illustrates a perspective view of a portion of the memory array block of FIG. 3 indicated by phantom line A.

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FIG. 5 illustrates a top view of the portion of the memory array block of FIG. 3 indicated by phantom line A.

#### MODE(S) FOR CARRYING OUT THE INVENTION

5           The following description provides specific details, such as material types, material thicknesses, and processing conditions in order to provide a thorough description of embodiments of the present disclosure. However, a person of ordinary skill in the art will understand that the embodiments of the present disclosure may be practiced without employing these specific details. Indeed, the embodiments of the present disclosure may be practiced in conjunction with conventional fabrication techniques employed in the industry.

          In the following detailed description, reference is made to the accompanying drawings, which form a part hereof, and in which are shown, by way of illustration, specific embodiments in which the present disclosure may be practiced. These  
15       embodiments are described in sufficient detail to enable a person of ordinary skill in the art to practice the present disclosure. However, other embodiments may be utilized, and structural, logical, and electrical changes may be made without departing from the scope of the disclosure. The illustrations presented herein are not meant to be actual views of any particular system, device, or structure, but are merely  
20       idealized representations that are employed to describe the embodiments of the present disclosure. The drawings presented herein are not necessarily drawn to scale. Similar structures or components in the various drawings may retain the same or similar numbering for the convenience of the reader; however, the similarity in numbering does not mean that the structures or components are necessarily identical in size,  
25       composition, configuration, or any other property.

          The materials described herein may be formed by any suitable technique including, but not limited to, spin coating, blanket coating, chemical vapor deposition (CVD), atomic layer deposition (ALD), plasma enhanced ALD, or physical vapor deposition (PVD), unless otherwise specified. Depending on the specific material to be  
30       formed, the technique for depositing or growing the material may be selected by a person of ordinary skill in the art. While the materials described and illustrated herein

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may be formed as layers, the materials are not limited thereto and may be formed in other three-dimensional configurations.

As used herein, the term “substantially” in reference to a given parameter, property, or condition means and includes to a degree that one of ordinary skill in the art would understand that the given parameter, property, or condition is met with a small degree of variance, such as within acceptable manufacturing tolerances. By way of example, depending on the particular parameter, property, or condition that is substantially met, the parameter, property, or condition may be at least 90% met, at least 95% met, or even at least 99% met.

As used herein, the phrase “semiconductor device structure” means and includes a structure, device, or system used in the formation of a semiconductor device and which may or may not be present in the semiconductor device in its final form. For example, a semiconductor device structure may be an intermediate structure present in the formation of a semiconductor device or system or a final structure comprising at least a portion of a semiconductor device or system. “Semiconductor device structure” encompasses structures for memory, solar cells, light emitting diodes (LEDs), processors, and other devices and systems that may or may not include one or more semiconductor materials.

As used herein, any relational term, such as “first,” “second,” “over,” “under,” “on,” “underlying,” etc., is used for clarity and convenience in understanding the disclosure and accompanying drawings and does not connote or depend on any specific preference, orientation, or order, except where the context clearly indicates otherwise.

As used herein, the terms “vertical” and “horizontal” are in reference to a major plane of a substrate in or on which the structures described are formed and are not necessarily defined by earth’s gravitational field. A “horizontal” direction is a direction that is substantially parallel to the major plane of the substrate, while a “vertical” direction is a direction that is substantially perpendicular to the major plane of the substrate. The major plane of the substrate is defined by a surface of the substrate having a relatively large area compared to other surfaces of the substrate, such as by a substantially planar circular surface of a conventional semiconductor wafer substrate.

As used herein, the terms “lateral” and “laterally” refer to a direction that extends horizontally across a width of an elongated member and that is substantially

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perpendicular to a longitudinal axis of the elongated member. Unless stated otherwise, the “lateral” direction referred to herein is in reference to an elongated memory array block. For example, a lateral side surface (i.e., a surface that faces in a lateral direction) of an elongated member may extend along the elongated member between longitudinal  
5 ends of the elongated member and between vertically lower and upper surfaces of the elongated member.

As used herein, the phrase “coupled to” refers to elements operatively connected with each other, such as electrically connected through a direct ohmic connection or through an indirect connection (e.g., via another element).

10 Semiconductor devices (e.g., vertical memory devices, such as three-dimensional NAND memory devices) including stair step structures defining contact regions on conductive materials (e.g., conductive tiers, conductive layers, conductive plates) are disclosed, as are methods of forming such devices. The semiconductor devices of the present disclosure may include one or more stair step  
15 structures along a lateral side surface of the memory array block. In some embodiments, the contact regions may be positioned along the memory array block in more than one stair step structure. In some embodiments, the stair step structures may be recessed from a lateral side surface of the memory array block. In some embodiments, the stair step structures may be positioned in a longitudinal location along  
20 the memory array block between the longitudinal ends of the memory array block, such as longitudinally between vertical strings of memory cells. Since the stair step structures may be positioned internally (e.g., between longitudinal ends of the memory array block and between lateral side surfaces of the memory array block), the stair step structures may be considered “stairwells” between memory array regions of the memory  
25 array block. Positioning the contact regions along the lateral side surface of the memory array block may result in a greater number of conductive tiers used in the memory array block without adding additional lateral width (or adding a minimal lateral width) to the memory array block. In addition, access lines may be physically separated from each other at a greater distance to reduce electrical stress between adjacent access lines,  
30 without adding any lateral width (or adding a minimal lateral width) to the memory array block. While the non-volatile memory devices described herein may make

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specific reference to NAND devices, the disclosure is not so limited and may be applied to other semiconductor and memory devices.

FIGS. 1 and 2 and the accompanying description thereof in this specification are provided to enhance an understanding by one of ordinary skill in the art of  
5 embodiments of the present disclosure, and are not admitted by applicants as prior art for any purpose.

FIG. 1 illustrates a partially cutaway perspective view of a portion of a three dimensional (3-D) semiconductor device structure 100 that includes a stair step structure 120 for defining contact regions for connecting access lines 106 to conductive  
10 tiers 105 (e.g., conductive layers, conductive plates). The semiconductor device structure 100 may include, for example, a NAND Flash memory array. The semiconductor device structure 100 may include vertical strings 101 of memory cells 103 that are coupled to each other in series. The vertical strings 101 may extend vertically and orthogonal to conductive lines and tiers, such as data lines 102, a source  
15 tier 104, the conductive tiers 105, access lines 106, first select gates 108 (e.g., upper select gates, drain select gates (SGDs)), select lines 109, and a second select gate 110 (e.g., a lower select gate, a source select gate (SGS)). Vertical conductive contacts 111 may electrically couple components to each other as shown, such as the select lines 109 to the first select gates 108, the access lines 106 to the conductive tiers 105, etc. The  
20 semiconductor device structure 100 may also include a control unit 112 positioned under the memory array, which may include at least one of string driver circuitry, pass gates, circuitry for selecting gates, circuitry for selecting conductive lines (e.g., the data lines 102, the access lines 106), circuitry for amplifying signals, and circuitry for sensing signals. The control unit 112 may be electrically coupled to the data lines 102,  
25 source tier 104, access lines 106, first select gates 108, and second select gate 110, for example.

Insulating materials between the elements shown in FIG. 1 are omitted from FIG. 1 for clarity. Insulating materials may be formed of an oxide material, for example, or another dielectric material, as is known in the art. Conductive materials and  
30 structures may be formed of a metal material, a polysilicon material, or other doped or undoped electrically conductive materials, as is known in the art. In addition, some components, such as some conductive tiers 105, access lines 106, select lines 109, and

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vertical conductive contacts 111, are also omitted from FIG. 1 to more clearly show other features of the semiconductor device structure 100, such as the vertical strings 101 of the memory cells 103. For example, FIG. 1 illustrates only four conductive tiers 105, although the semiconductor device structure 100 may, in reality, include any number of  
5 conductive tiers 105, such as 16, 32, or 64 conductive tiers 105. Additionally, FIG. 1 illustrates only an end portion of a block of memory cells 103 to clearly show various components and electrical connections. In reality, the block of memory cells 103 may extend longitudinally a much greater distance to the right in the perspective of FIG. 1, as will be explained below with reference to FIG. 2.

10       The first select gates 108 may extend horizontally in a first direction  $x$  (e.g., to the left and right from the perspective of FIG. 1) and may be coupled to respective first groups of vertical strings 101 of memory cells 103 at a first end (e.g., an upper end) of the vertical strings 101. The second select gate 110 may be formed in a substantially planar configuration and may be coupled to the vertical strings 101 at a second, opposite  
15 end (e.g., a lower end) of the vertical strings 101 of memory cells 103.

      The data lines 102 (e.g., bit lines) may extend horizontally in a second direction  $y$  (e.g., up and down from the perspective of FIG. 1) that is at an angle (e.g., perpendicular) to the first direction in which the first select gates 108 extend. The data lines 102 may be coupled to respective second groups of the vertical strings 101 at the  
20 first end (e.g., the upper end) of the vertical strings 101. A first group of vertical strings 101 coupled to a respective first select gate 108 may share a particular vertical string 101 with a second group of vertical strings 101 coupled to a respective data line 102. Thus, a particular vertical string 101 may be selected at an intersection of a particular first select gate 108 and a particular data line 102.

25       The conductive tiers 105 (e.g., word line plates) may extend in respective horizontal planes. The conductive tiers 105 may be stacked vertically, such that each conductive tier 105 is coupled to all of the vertical strings 101 of memory cells 103, and the vertical strings 101 of memory cells 103 extend vertically through the stack of conductive tiers 105. The conductive tiers 105 may be coupled to or may form control  
30 gates of the memory cells 103 to which the conductive tiers 105 are coupled. Each conductive tier 105 may be coupled to one memory cell 103 of a particular vertical string 101 of memory cells 103.

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The first select gates 108 and the second select gate 110 may operate to select a particular vertical string 101 of memory cells 103 between a particular data line 102 and the source tier 104. Thus, a particular memory cell 103 may be selected and electrically coupled to a data line 102 by operation of (e.g., by selecting) the appropriate first select  
5 gate 108, second select gate 110, and conductive tier 105 that are coupled to the particular memory cell 103.

As shown in FIG. 1, the conductive tiers 105 may be configured to include the stair step structure 120 along an end of the conductive tiers 105 (e.g., along the left end of the conductive tiers 105 when viewed in the perspective of FIG. 1) to define contact  
10 regions for respectively coupling the access lines 106 (e.g., word lines) to the conductive tiers 105 with the vertical conductive contacts 111. Thus, portions of the conductive tiers 105 may be formed as respective stair steps of the stair step structure 120. The stair step structure 120 may be a structure that includes contact regions (also referred to as “stair steps”) at different vertical elevations and that extend  
15 to different distances in the horizontal direction. For example, the contact region of a conductive tier 105 relatively proximate an underlying substrate may extend horizontally beyond the contact region of a conductive tier 105 relatively more distant from the underlying substrate. A lower stair step may extend horizontally a sufficient distance beyond a next higher stair step to define a contact region on the lower stair step  
20 sufficiently large to form a vertical conductive contact 111 coupled to the contact region and electrically isolated from the next higher stair step. The stair step structure 120 may be formed at a longitudinal end of a memory array block, as will be explained below with reference to FIG. 2.

Referring to FIG. 2, a simplified semiconductor device structure 200 is  
25 illustrated that shows a top view of two memory array blocks 250 arranged laterally adjacent to each other. Each of the memory array blocks 250 may include a conventional stair step structure 220 at a longitudinal end thereof. Conventionally, many memory array blocks 250 are arranged laterally adjacent to each other in a semiconductor device structure 200. Each memory array block 250 may be similar to  
30 the structure shown in FIG. 1, except the memory array blocks 250 of FIG. 2 are shown as including fewer conductive tiers 205 than the complete structure of FIG. 1, for simplicity of explanation. As shown in FIG. 2 for illustration purposes, each memory

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array block 250 may include vertical memory strings 201 that extend through four conductive tiers 205 (e.g., word line plates). First select gates 208 (e.g., upper select gates, drain select gates (SGDs)) extending horizontally in the  $x$  direction and data lines 202 (e.g., bit lines) extending horizontally in the  $y$  direction at an angle (e.g., perpendicular) to the  $x$  direction may be coupled to upper ends of the vertical memory strings 201. The stair step structure 220 formed at a longitudinal end (e.g., a left end when viewed from the perspective of FIG. 2) of each memory array block 250 may form contact regions for coupling access lines 206 (e.g., word lines) to respective conductive tiers 205 using vertical conductive contacts 211. Each memory array block 250 has a lateral width  $W$  and a longitudinal length  $L$ , as shown in FIG. 2. By way of example and not limitation, the width  $W$  may be on the order of about  $2\text{ }\mu\text{m}$  to about  $20\text{ }\mu\text{m}$  and the length  $L$  may be on the order of about several hundreds or thousands of microns. In addition, each block 250 may include sub-blocks each corresponding to a respective first select gate 208. For example, each block 250 shown in FIG. 2 includes two first select gates 208 and, therefore, two corresponding sub-blocks.

Generally speaking, as 3-D semiconductor device technology has advanced, additional feature density (e.g., number of memory cells per unit of area) has been provided, in part, by forming blocks to a greater vertical height and having a higher number of conductive tiers (e.g., word line plates). However, greater numbers of conductive tiers per block require a corresponding greater number of contact regions and access lines. Referring to FIG. 2 for purposes of illustration, additional contact regions may be defined by forming additional stair steps in each stair step structure 220. However, forming additional stair steps may conventionally require forming each memory array block 250 at a greater width  $W$ , to provide sufficient space for the additional access lines 206. In addition, a number of first select gates 208 and corresponding sub-blocks per block 250 used to uniquely access all memory cells in each block 250 may be increased as the width  $W$  is increased. For example, if each block 250 of FIG. 2 were to include eight conductive tiers 205 and eight access lines 206 instead of the four that are shown, the width  $W$  and the number of first select gates 208 and corresponding sub-blocks per block 250 may be approximately doubled to accommodate the additional access lines 206. However, increasing the width  $W$

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and/or the number of first select gates 208 and corresponding sub-blocks per block 250 may be undesirable. Alternatively or additionally, the access lines 206 may be formed at a smaller size (e.g., pitch) to fit the additional access lines 206 into a given width W. However, reducing the size of the access lines 206 may significantly increase the cost of forming the access lines 206, such as requiring more advanced and expensive lithographic tools. In addition, reducing the size of the access lines 206 may cause performance problems, such as due to an increased electrical stress (e.g., stress across a dielectric) between adjacent access lines 206 that are formed closer to each other.

Referring to FIGS. 3 through 5, an embodiment of a semiconductor device structure 300 including at least one memory array block 350 according to the present disclosure is illustrated. The memory array block 350 may include one or more stair step structures 340A, 340B, 340C, 340D (generically referred to by reference numeral 340) positioned between longitudinal ends of the memory array block 350, rather than at a longitudinal end, such as along a lateral side surface 360 of the memory array block 350. In addition, the one or more stair step structures 340 may each be positioned between opposing lateral side surfaces 360 of the memory array block 350. Positioning the one or more stair step structures 340 in this manner may enable the use of any number of conductive tiers 305 without contributing to an increase in the lateral width W of the memory array block 350 and/or without forming access lines 306 at a smaller size (e.g., at a reduced pitch). Indeed, embodiments of the memory array block 350 according to the present disclosure may enable the lateral width W to be decreased and/or may alleviate electrical stress between adjacent access lines 306 by forming the access lines 306 at a larger size and/or with increased distance between adjacent access lines 306, as will be described below. In addition, in embodiments in which the access lines 306 are formed at a larger size, electrical resistance through the access lines 306 may be reduced.

The memory array block 350 may include substantially planar, elongated conductive tiers 305 (e.g., word line plates) arranged in a vertical stack and separated by substantially planar insulating materials (not shown for clarity). As shown in FIGS. 3 and 4, for example, the memory array block 350 may include 32 conductive tiers 305. However, the present disclosure is not limited to memory array blocks 350 having 32 conductive tiers 305. Rather, memory array blocks according to the present disclosure

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may include any number of conductive tiers 305. By way of example and not limitation, memory array blocks of the present disclosure may include 16 or more conductive tiers 305, such as 16, 32, 64, or 128 conductive tiers 305. In some embodiments, the memory array block 350 may include 32 or more conductive  
5 tiers 305, such as 64 or 128 conductive tiers 305.

As noted above, the one or more stair step structures 340 may be positioned between longitudinal ends of the memory array block 350, such as along the lateral side surface 360 and between opposing lateral side surfaces 360 of the memory array block 350. In some embodiments, the longitudinal ends of the memory array block 350  
10 may lack a stair step structure. As shown in FIG. 3, a first stair step structure 340A may define contact regions for electrically contacting a first portion of the conductive tiers 305, such as the eight conductive tiers 305 closest to an underlying substrate. A second stair step structure 340B may define contact regions for electrically contacting a second portion of the conductive tiers 305, such as the eight conductive tiers 305 next  
15 closest to the underlying substrate. A third stair step structure 340C may define contact regions for electrically contacting a third portion of the conductive tiers 305, such as the eight conductive tiers 305 next closest to the underlying substrate. A fourth stair step structure 340D may define contact regions for electrically contacting a fourth portion of the conductive tiers 305, such as the eight conductive tiers 305 most distant from the  
20 underlying substrate. The stair step structures 340 may be separated from one another by one or more structures, such as other portions of the conductive tiers 305 lacking a stair step structure 340.

Although each of the stair step structures 340 is shown in FIGS. 3 through 5 as defining contact regions for eight of the conductive tiers 305, the present disclosure is  
25 not so limited. By way of example and not limitation, each stair step structure 340 may define contact regions for 4, 8, 12, 16, or more than 16 conductive tiers 305.

Furthermore, although four stair step structures 340A through 340D are shown in FIG. 3, any number of stair step structures 340 may be used. For example, in some embodiments, the memory array block 350 may include one, two, three, four, or more  
30 than four (e.g., eight) stair step structures 340. The number of stair step structures may be selected based on manufacturing and space considerations, for example. One of ordinary skill in the art may select the number of stair step structures 340 in a given

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memory array block 350 and the number of contact regions defined by each stair step structure 340 based on, for example, complexity and cost of manufacturing, quantity of conductive tiers 305, desired lateral width W of the memory array block 350, etc.

Vertical strings 301 (FIG. 5) of memory cells may extend through the  
5 conductive tiers 305, as discussed above with reference to the vertical strings 101 of FIG. 1 and the vertical strings 201 of FIG. 2. First select gates 308 (e.g., upper select gates, drain select gates (SGDs)) may extend substantially longitudinally along the memory array block 350 in a first horizontal direction and may be coupled to ends (e.g., upper ends) of the vertical strings 301 of memory cells. The memory array block 350  
10 may include sub-blocks each corresponding to a respective first select gate 308. In addition, data lines 302 (e.g., bit lines) (FIGS. 4 and 5) may extend laterally across the memory array block 350 in a second direction at an angle (e.g., perpendicular) to the first direction and may be coupled to the ends (e.g., the upper ends) of the vertical strings 301 of memory cells, as described above with reference to the data lines 102 of  
15 FIG. 1 and the data lines 202 of FIG. 2. Although not shown in FIGS. 3 through 5 for clarity, the memory array block 350 may include a second select gate similar to the second select gate 110 of FIG. 1. Each of the first select gates 308 may, for example, be a control gate of first select transistors coupled to the data lines 302.

At least one of the one or more stair step structures 340 may be positioned  
20 between longitudinal ends of the memory array block 350. At least one of the stair step structures 340 may be between first and second portions of a memory array defined by the memory array block 350. The first portion of the memory array may include a first plurality of the first select gates 308 and the second portion of the memory array may include a second plurality of the first select gates 308. Each of the first select gates 308  
25 may extend in a particular direction (e.g., longitudinally) over the stack of conductive tiers 305. Thus, in some embodiments, at least one of the stair step structures 340 may be positioned longitudinally between (e.g., directly between) a first portion (i.e., group) of the vertical strings 301 (FIG. 5) and a second, different portion (i.e., group) of the vertical strings 301. For example, as shown in FIG. 5, the stair step structure 340C may  
30 be positioned longitudinally between a first portion of vertical strings 301 on the left of FIG. 5 and a second portion of vertical strings 301 on the right of FIG. 5. Thus, proceeding from one longitudinal end to an opposite longitudinal end of the memory

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array block 350, the memory array block 350 may be defined by alternating memory array regions 370 including first select gates 308 and stair step regions 380 lacking first select gates 308 (see FIGS. 3 through 5). The memory array regions 370 may include vertical strings 301 of memory cells and first select gates 308, while the stair step  
5 regions 380 may be free of vertical strings 301 of memory cells and free of first select gates 308.

Contact regions defined by each of the one or more stair step structures 340 may be aligned in the same direction that the first select gates 308 extend over the stack of conductive tiers 305. The first select gates 308 extending over the stack of  
10 conductive tiers 305 may have a collective lateral width (e.g., a width in a direction orthogonal to the particular direction in which the conductive tiers 305 extend). Each of the one or more stair step structures 340 may also have a lateral width (e.g., a width in a direction orthogonal to the direction in which the memory array block 350 extends), which may be less than the collective lateral width of the first select gates 308.

15 Accordingly, embodiments of the present disclosure include semiconductor device structures that include at least one memory array block defined by an elongated stack of conductive tiers. The at least one memory array block includes one or more stair step structures positioned between longitudinal ends of the memory array block. The one or more stair step structures define contact regions for electrically contacting  
20 respective conductive tiers of the elongated stack of conductive tiers. The one or more stair step structures are also positioned longitudinally between a first portion of vertical strings of memory cells and a second portion of vertical strings of memory cells.

In addition, embodiments of the present disclosure include semiconductor device structures that include elongated memory array blocks laterally adjacent to one  
25 another. Each of the memory array blocks includes a vertical stack of horizontal conductive tiers separated by electrically insulating materials and at least one stair step structure defined by portions of the conductive tiers. The at least one stair step structure is positioned along a lateral side of the memory array block and between opposing lateral side surfaces of the memory array block for providing electrical access to  
30 respective conductive tiers of the vertical stack of horizontal conductive tiers.

Access lines 306 may electrically couple respective conductive tiers 305 to one or more control units 312, which may be positioned under the memory array block 350.

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Each of the one or more control units 312 may include at least one of string driver circuitry, pass gates, circuitry for selecting gates, circuitry for selecting conductive lines (e.g., the data lines 302, the access lines 306), circuitry for amplifying signals, and circuitry for sensing signals. For example, the one or more control units 312 may  
5 include transistors (e.g., so-called “pass gates”) that are electrically coupled to access lines 306 for selecting a desired one of the conductive tiers 305, for example.

As shown in FIG. 4, in some embodiments, the access lines 306 may include lower horizontal portions 306A, upper horizontal portions 306B, laterally outer vertical portions 311A, and laterally inner vertical portions 311B. The lower horizontal  
10 portions 306A may be coupled to and extend between the one or more control units 312 and respective outer vertical portions 311A. The outer vertical portions 311A may be coupled to and extend between the lower horizontal portions 306A and the upper horizontal portions 306B. The upper horizontal portions 306B may be coupled to and extend between the outer vertical portions 311A and the inner vertical portions 311B.  
15 The inner vertical portions 311B may be coupled to and extend between the upper horizontal portions 306B and respective conductive tiers 305 of the stair step structure 340. Thus, the access lines 306 may form an electrical connection between the one or more control units 312 and respective conductive tiers 305 of the stair step structure 340, to provide electrical access to the conductive tiers 305, such as for  
20 reading, writing, or erasing data associated with memory cells of the vertical strings 301.

As shown in FIGS. 4 and 5, a lateral side surface 362 of the stair step structures 340 may be recessed from a plane defined by the lateral side surface 360 of the memory array block 350 toward a center of the memory array block 350, such as to  
25 enable the outer vertical portions 311A of the access lines 306 to be positioned along the lateral side surface 360 without adding significant, if any, width W to the memory array block 350. The outer vertical portions 311A of the access lines 306 may be aligned in a plane that is parallel to the plane defined by the lateral side surface 360 of the memory array block 350. In some embodiments, the outer vertical portions 311A of the access  
30 lines 306 may be positioned between planes defined by opposing lateral side surfaces 360 of the memory array block 350.

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Accordingly, embodiments of the present disclosure also include semiconductor device structures including at least one three-dimensional memory array block elongated in a horizontal direction. The at least one three-dimensional memory array block includes a vertical stack of conductive tiers, a lateral side surface, and at least one stair step structure. The at least one stair step structure includes contact regions of at least some of the conductive tiers of the vertical stack of conductive tiers. The at least one stair step structure is recessed from the lateral side surface of the at least one three-dimensional memory array block.

The stair step structures 340 may extend laterally across only a portion of the width W of the memory array block 350. Thus, a portion of the stair step portion 380 of the memory array block 350 laterally adjacent (i.e., in a direction laterally across the memory array block 350, up and down in the view of FIG. 5) to each stair step structure 340 may be free of the stair step structure 340 and may include all of the conductive tiers 305 of the memory array block 350. Thus, all of the respective conductive tiers 305 of the memory array regions 370 on longitudinally opposing sides of the stair step portion 380 may be continuous and in electrical communication with each other through the stair step portion 380.

As shown in FIGS. 3 and 4, two control units 312 may be associated with each stair step structure 340. A first control unit 312 may be positioned under (e.g., at least partially under) a first memory array region 370 and a second, different control unit 312 may be positioned under (e.g., at least partially under) a second memory array region 370, as shown in FIG. 3. The first control unit 312 may be electrically coupled to a first half (e.g., four) of the access lines 306 associated with the stair step structure 340 and the second, different control unit 312 may be electrically coupled to a second half (e.g., four) of the access lines associated with the stair step structure 340. Thus, only one half (e.g., four) of the lower horizontal portions 306A of the access lines 306 associated with one of the stair step structures 340 may be positioned across the width W of the memory array block 350. Accordingly, the lower horizontal portions 306A of adjacent access lines 306 may be spaced at a greater distance from each other to alleviate electrical stress and reduce manufacturing costs compared to access lines that are associated with a stair step structure positioned at a longitudinal end of a memory array block, such as the stair step structure 120 shown in FIG. 1. For example, if the

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memory array block according to FIG. 1 includes 16 conductive tiers 105, a width of the memory array block and number of first select gates 108 would need to be sufficient to accommodate at least 16 access lines 106. To form the memory array block of FIG. 1 at a relatively small width and using fewer first select gates 108, the access lines 106  
5 would be formed at a small size and relatively close to one another, as explained above. Accordingly, embodiments of the present disclosure may enable more flexibility in the design and formation of the access lines 306 and the spacing thereof.

In addition, spacing between the vertical portions 311A, 311B and the upper horizontal portions 306B of adjacent access lines 306 may be greater than spacing  
10 between adjacent access lines that are associated with a stair step structure positioned at a longitudinal end of a memory array block. As shown in FIGS. 3 through 5, the contact regions defined by each of the stair step structures 340 may be aligned substantially parallel to a longitudinal length of the memory array block 350 and substantially parallel to a plane defined by the lateral side surface 360 of the memory  
15 array block 350. The upper horizontal portions 306B of the access lines 306 associated with each of the stair step structures 340 may extend laterally from over the stair step structure 340 toward the plane defined by the lateral side surface 360 and substantially perpendicular to the plane defined by the lateral side surface 360. A length  $L_{SS}$  (FIG. 5) of the stair step structure may be adjusted as desired to provide sufficient space for  
20 forming the access lines 306 such that electrical stress and manufacturing cost is reduced or maintained at a relatively low level, without adding significant width  $W$  and/or number of first select gates 308 and corresponding sub-blocks to the memory array block 350 as a whole, or even while reducing the width  $W$  and/or number of first select gates 308 and corresponding sub-blocks of the memory array block 350. By way  
25 of example and not limitation, while conventional access lines associated with 32 conductive tiers are formed with a distance between the access lines of less than 100 nm, such as about 45 nm, adjacent access lines 306 according to the present disclosure may be separated by a distance of at least about 100 nm, such as 200 nm, 300 nm, 500 nm, or 1  $\mu\text{m}$ . Such beneficial configurations may exist regardless of the  
30 number of conductive tiers 305 included in the memory array block 350.

Although FIG. 4 illustrates two control units 312 positioned under and longitudinally adjacent to the stair step structure 340C (e.g., at least partially directly

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under respective memory array regions 370), other configurations are included in the present disclosure. For example, one or more control units 312 may be positioned directly under the stair step structure 340C (i.e., at the same longitudinal position along the length of the memory array block 350 as the stair step structure 340C). In such

5   embodiments, the lower horizontal portions 306A of the access lines 306 may extend only in a lateral direction from the one or more control units 312 to the outer vertical portions 311A. Stated another way, the lower horizontal portions 306A may not include any portion that extends longitudinally parallel to a longitudinal length of the memory array block 350. Alternatively, the lower horizontal portions 306A may be omitted and

10   the outer vertical portions 311A may be directly coupled to the one or more control units 312.

Since the stair step structures 340 are used instead of a stair step structure at a longitudinal end of the memory array block 350, an overall longitudinal length of the memory array block 350 according to the present disclosure may be the same, less than,

15   or only slightly greater than a conventional memory array block including a stair step structure at a longitudinal end, even if the length  $L_{SS}$  of each stair step structure 340 is increased to provide additional space for the access lines 306, as described above. Any such lengthening of the memory array block 350 may be insignificant relative to the benefits of reducing the width  $W$  of the memory array block 350 and/or providing

20   increased space between access lines 306 enabled by embodiments of the present disclosure.

Referring again to FIGS. 4 and 5, the first select gates 308 (e.g., upper select gates, drain select gates (SGDs)) may longitudinally extend over the stack of conductive tiers 305. In some embodiments, the first select gates 308 may extend directly over and

25   adjacent to the stack of conductive tiers 305 only over one or more portions of the memory array block 350, such as over and adjacent to the memory array portions 370 of the memory array block 350. However, the first select gates 308 may not extend over the stair step regions 380 of the memory array block 350, due to the position of one or more of the stair step structures 340 and the access lines 306. In the stair step

30   regions 380, one or more electrical lines 328 may be used to electrically couple a first portion of the first select gates 308 over a first memory array portion 370 to respective first select gates 308 of a second portion of the first select gates 308 over a second

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memory array portion 370 on longitudinally opposite sides of the stair step region 380. The one or more electrical lines 328 may be sufficiently laterally thin to be routed around the stair step structures 340 and/or the access lines 306.

As shown in FIGS. 4 and 5, the memory array block 350 may include eight first  
5 select gates 308 and corresponding sub-blocks laterally adjacent to each other. In comparison with the structure of FIG. 1, fewer first select gates 308 and corresponding sub-blocks may be used for a given number of conductive tiers 305. For example, if the structure of FIG. 1 includes 32 conductive tiers 105, a width of the stair step structure 120 may be sufficient to position at least 16 first select gates 108 and  
10 corresponding sub-blocks over the structure. However, if the same number of 32 conductive tiers 305 are used in the structure of FIGS. 4 and 5, the width W of the memory array block 350 may be sufficient for only eight or even fewer (e.g., four) first select gates 308 and corresponding sub-blocks. Accordingly, embodiments of the present disclosure include semiconductor device structures 300 including memory array  
15 blocks 350 that may have at least 32 conductive tiers and at most eight first select gates 308 and corresponding sub-blocks, such as having 64 conductive tiers 305 and eight first select gates and corresponding sub-blocks. By way of example and not limitation, the memory array blocks 350 of the present disclosure may include at least 32 conductive tiers 305 and have a lateral width W that is about 5  $\mu\text{m}$  or less, such as  
20 about 3  $\mu\text{m}$  or less. In some embodiments, the memory array blocks 350 may include 64 or more conductive tiers 305 and have a lateral width W that is about 2  $\mu\text{m}$  or less. The reduced width W of each of the memory array blocks 350 may result in fewer first select gates 308 and corresponding sub-blocks that are used to uniquely access all of the memory cells in the memory array block 350.

25 Accordingly, embodiments of the present disclosure include vertical memory devices that include at least one elongated vertical memory array block including vertical strings of memory cells and at least one stair step structure including contact regions of respective conductive tiers thereof. The at least one vertical memory array block may include at least 32 conductive tiers for selecting the memory cells and may  
30 have a lateral width of about 5  $\mu\text{m}$  or less. The vertical strings of memory cells may extend through the at least 32 conductive tiers.

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In addition, embodiments of the present disclosure include semiconductor memory devices including at least one memory array block including at least 16 conductive tiers and at least two stair step structures defining contact regions to the at least 16 conductive tiers. The at least two stair step structures are located between longitudinal ends of the at least one memory array block. At least 16 access lines are electrically coupled to respective contact regions defined by the at least two stair step structures. A portion of the at least one memory array block lacks a stair step structure and is located between the at least two stair step structures.

Additional embodiments of the present disclosure include semiconductor devices including a memory array. The memory array may include a stack of conductive tiers and a stair step structure between first and second portions of the memory array. The stair step structure may include contact regions for respective conductive tiers of the stack of conductive tiers. The first portion of the memory array may include a first plurality of select gates. Each select gate of the first plurality of select gates may extend in a particular direction over the stack of conductive tiers. The second portion of the memory array may include a second plurality of select gates. Each select gate of the second plurality of select gates may also extend in the particular direction over the stack of conductive tiers.

By way of example and not limitation, the semiconductor device structures 300 of the present disclosure may be formed using conventional semiconductor manufacturing techniques. For example, the alternating conductive tiers 305 and insulating materials may be formed using conventional material formation techniques, such as chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), spin-coating, or combinations thereof. The conductive tiers 305 may be patterned into elongated structures to ultimately define the memory array blocks 350. If desired, portions of the elongated structures may be recessed from a lateral side surface 360 thereof, to form the stair step regions 340 with a recessed lateral side surface 362, as explained above. The stair step structures 340 may be formed by covering portions of an upper conductive tier 305 of the stack of conductive tiers 305 with a first mask, which may be a so-called "hardmask." One or more apertures may be formed through the first mask at desired locations of the stair step structures 340, such as between longitudinal ends (e.g., along the lateral side surface 360) of the memory

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array blocks 350 to be formed. Each of the stair step structures 340 may be formed through the apertures in the first mask, such as by using a second mask. One or more pairs of conductive materials 305 and insulating material may be removed using the first mask and the second mask to protect portions of the structure to remain, the second  
5 mask may be horizontally recessed, and the material removal and recessing operations may be repeated until the desired number of contact regions (e.g., stair steps) are formed, as is known in the art.

Other elements of the structure (e.g., one or more control units 312, access lines 306, first select gates 308, data lines 302, vertical strings 301 of memory cells, etc.)  
10 may be formed in the locations and configurations described above using conventional semiconductor fabrication techniques.

Accordingly, the present disclosure includes methods of forming a semiconductor device structure. In accordance with such methods, a stack of alternating conductive tiers and insulating materials is formed and patterned to form at least one  
15 elongated memory array block. One or more stair step structures are formed between longitudinal ends of the at least one elongated memory array block and between lateral side surfaces of the at least one elongated memory array block to define contact regions of respective conductive tiers of the stack of alternating conductive tiers and insulating materials.

20 The present disclosure also includes methods of forming a semiconductor device, which may include forming a memory array including a stack of conductive tiers and positioning a stair step structure between first and second portions of the memory array. Contact regions for respective conductive tiers of the stack of conductive tiers may be defined by the stair step structure. A first plurality of select  
25 gates may be formed over the first portion of the memory to extend in a particular direction over the stack of conductive tiers. A second plurality of select gates may be formed over the second portion of the memory array to extend in the particular direction over the stack of conductive tiers.

Methods of operating semiconductor devices include accessing a memory cell  
30 of a three-dimensional memory array block, such as the memory array block 350 shown in FIGS. 3 through 5. The memory cell may be accessed by performing one or more of a read operation, a write operation, and an erase operation. As described in detail above,

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the memory array block 350 may be defined by an elongated stack of conductive tiers and may include at least one stair step structure 340 that defines contact regions for electrically accessing respective conductive tiers 305. The at least one stair step structure 340 may be positioned longitudinally between a first portion of vertical strings 301 of memory cells (e.g., the portion of vertical strings 301 to the left of FIG. 5) and a second portion of vertical strings 301 (e.g., the portion of vertical strings 301 to the right of FIG. 5).

Accessing of the memory cell may be accomplished, in part, by applying a voltage to the access line 306 that is electrically coupled to the desired memory cell. The particular voltage applied to the access line 306 may be based on whether the memory cell is being read from, written to, or erased, for example. For example, during a read operation, the access line 306 that is electrically coupled to the desired memory cell through a conductive tier 305 may be biased to a low (e.g., ground) voltage, while the access lines 306 electrically coupled to the other memory cells in the vertical string 301 through other conductive tiers 305 including the memory cell to be accessed may be biased to a relatively higher voltage (e.g., 5V) to cause the other memory cells to be electrically conductive regardless of their data states. Thus, a voltage across the vertical string 301 may depend on whether the read memory cell is in a charged state (e.g., resulting in high conductivity thereof, resulting in a low voltage across the vertical string 301) or in a non-charged state (e.g., resulting in low or no conductivity thereof, resulting in a high voltage across the vertical string 301).

During a write operation, the access line 306 that is electrically coupled to the desired memory cell through a conductive tier 305 may be biased to a high voltage (e.g., above about 12V) sufficient to drive charge into a floating gate of the memory cell while access lines 306 electrically coupled to the other memory cells in the vertical string 301 through other conductive tiers 305 including the memory cell to be accessed may be biased to a relatively lower voltage (e.g., about 5V) insufficient to drive charge into floating gates thereof.

During an erase operation, a group of memory cells, such as all the memory cells of the memory array block 350, may be erased at substantially the same time (e.g., concurrently). For example, a source tier of the memory array block 350 may be biased to a high voltage (e.g., above about 12V) and a plurality of the access lines 306 and

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corresponding conductive tiers 305 of the memory array block 350 may be biased to a lower voltage (e.g., ground) sufficient to drive charge from a floating gate of each of the memory cells in the memory array block 350 that are erased.

The methods of operating semiconductor devices according to the present  
5 disclosure may provide at least some advantages over conventional methods that may include applying a voltage to an access line. For example, regardless of the voltage level applied to the access lines 306 during an accessing operation of a memory cell, the spacing between the access lines 306 resulting from embodiments of the present disclosure, as discussed above, may reduce electrical stress (e.g., noise) between  
10 adjacent access lines 306 that may otherwise exist if the access lines 306 were formed relatively more closely together.

Accordingly, the present disclosure includes methods of operating semiconductor devices. In accordance with such methods, a memory cell of a three-dimensional memory array block may be accessed. The three-dimensional memory  
15 array block is defined by an elongated stack of conductive tiers and includes at least one stair step structure positioned between longitudinal ends of the three-dimensional memory array block. The at least one stair step structure defines contact regions for electrically accessing respective conductive tiers of the elongated stack of conductive tiers. The at least one stair step structure is also positioned longitudinally between a first  
20 portion of vertical strings of memory cells including the accessed memory cell and a second portion of vertical strings of memory cells.

The embodiments of the disclosure described above and illustrated in the accompanying drawing figures do not limit the scope of the invention, since these embodiments are merely examples of embodiments of the disclosure. The invention is  
25 defined by the appended claims and their legal equivalents. Any equivalent embodiments lie within the scope of this disclosure. Indeed, various modifications of the present disclosure, in addition to those shown and described herein, such as alternative useful combinations of the elements described, will become apparent to those of ordinary skill in the art from the description. Such modifications and embodiments  
30 also fall within the scope of the appended claims and their legal equivalents.

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## CLAIMS

What is claimed is:

- 5           1.       A semiconductor device comprising a memory array, the memory array comprising a stack of conductive tiers and a stair step structure between first and second portions of the memory array, wherein the stair step structure comprises contact regions for respective conductive tiers of the stack of conductive tiers, and wherein: the first portion of the memory array comprises a first plurality of select gates, wherein  
10           each select gate of the first plurality of select gates extends in a particular direction over the stack of conductive tiers; and  
the second portion of the memory array comprises a second plurality of select gates, wherein each select gate of the second plurality of select gates also extends in the particular direction over the stack of conductive tiers.  
15
2.       The semiconductor device of claim 1, wherein the contact regions of the stair step structure are aligned in the particular direction.
3.       The semiconductor device of claim 1, wherein the first and second  
20       pluralities of select gates each have a collective width in another direction that is orthogonal to the particular direction, and wherein the width of the stair step structure in the another direction is less than the collective width.
4.       The semiconductor device of claim 1, wherein the contact regions of  
25       the stair step structure comprise contact regions for less than all of the conductive tiers of the stack of conductive tiers.

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5. The semiconductor device of claim 4, wherein the stair step structure comprises a first stair step structure and the contact regions comprise first contact regions for a first plurality of conductive tiers of the stack of conductive tiers, the semiconductor device further comprising a second stair step structure between the  
5 second portion of the memory array and a third portion of the memory array, wherein the second stair step structure comprises second contact regions for a second plurality of conductive tiers of the stack of conductive tiers.

6. The semiconductor device of claim 5, wherein each select gate of the  
10 first plurality of select gates is coupled to a respective select gate of the second plurality of select gates.

7. The semiconductor device of claim 5, wherein the third portion of the memory array comprises a third plurality of select gates, wherein each select gate of the  
15 third plurality of select gates also extends in the particular direction over the stack of conductive tiers.

8. The semiconductor device of claim 7, wherein each select gate of the first plurality of select gates is coupled to a respective select gate of the second plurality  
20 of select gates, and wherein each select gate of the second plurality of select gates is coupled to a respective select gate of the third plurality of select gates.

9. The semiconductor device of claim 5, further comprising a third stair step structure between the third portion of the memory array and a fourth portion of the  
25 memory array, wherein the third stair step structure comprises third contact regions for a third plurality of conductive tiers of the stack of conductive tiers.

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10. The semiconductor device of claim 9, further comprising:  
a first control unit under the first portion of the memory array and coupled to a first  
portion of the first plurality of conductive tiers;  
a second control unit under the second portion of the memory array and coupled to a  
5 second portion of the first plurality of conductive tiers;  
a third control unit under the second portion of the memory array and coupled to a first  
portion of the second plurality of conductive tiers ;  
a fourth control unit under the third portion of the memory array and coupled to a  
second portion of the second plurality of conductive tiers;  
10 a fifth control unit under the third portion of the memory array and coupled to a first  
portion of the third plurality of conductive tiers; and  
a sixth control unit under the fourth portion of the memory array and coupled to a  
second portion of the third plurality of conductive tiers.

15 11. The semiconductor device of claim 10, wherein each of the first control  
unit, the second control unit, the third control unit, the fourth control unit, the fifth  
control unit, and the sixth control unit comprises pass gates.

12. The semiconductor device of claim 9, further comprising a fourth stair  
20 step structure between the fourth portion of the memory array and a fifth portion of the  
memory array, wherein the fourth stair step structure comprises fourth contact regions  
for a fourth plurality of conductive tiers of the stack of conductive tiers.

13. The semiconductor device of any one of claims 1 through 6, wherein  
25 the memory array comprises a memory array block comprising sub-blocks, wherein  
each of the sub-blocks corresponds to a respective select gate of the first plurality of  
select gates and a respective select gate of the second plurality of select gates, and  
wherein the first portion of the memory array further comprises a first plurality of  
vertical strings of memory cells and wherein the second portion of the memory array  
30 further comprises a second plurality of vertical strings of memory cells.

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14. The semiconductor device of any one of claims 1 through 6, further comprising:  
a first plurality of data lines over the first plurality of select gates, wherein each data line of the first plurality of data lines extends in another direction that is  
5 orthogonal to the particular direction; and  
a second plurality of data lines over the second plurality of select gates, wherein each data line of the second plurality of data lines also extends in the another direction,  
wherein the first plurality of select gates comprise control gates of first select  
10 transistors coupled to the first plurality of data lines, and wherein the second plurality of select gates comprise control gates of second select transistors coupled to the second plurality of data lines.
15. A method of forming a semiconductor device structure, the method  
15 comprising:  
forming a stack of alternating conductive plates and insulating materials;  
patterning the stack of alternating conductive plates and insulating materials to form at least one elongated memory array block; and  
forming one or more stair step structures between longitudinal ends of the at  
20 least one elongated memory array block and between lateral side surfaces of the at least one elongated memory array block to define contact regions of respective conductive plates of the stack of alternating conductive plates and insulating materials.
16. The method of claim 15, wherein forming one or more stair step  
25 structures between lateral side surfaces of the at least one elongated memory array block comprises forming the one or more stair step structures along one of the lateral side surfaces of the at least one memory array block.
17. The method of claim 15, further comprising laterally recessing the one  
30 or more stair step structures from a plane defined by one of the lateral side surfaces of the at least one memory array block.

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18. The method of claim 15, further comprising electrically coupling access lines to respective contact regions defined by the one or more stair step structures.

19. The method of claim 18, further comprising forming the access lines to  
5 have a distance between adjacent access lines of at least about 100 nm.

20. The method of any one of claims 15 through 19, wherein:  
forming a stack of alternating conductive plates and insulating materials  
comprises forming at least 32 conductive plates; and  
10 patterning the stack of alternating conductive plates and insulating materials to  
form at least one elongated memory array block comprises forming the at least one  
elongated memory array block to have a lateral width of about 5  $\mu\text{m}$  or less.