NOT gate 920 is coupled to the first output terminal 916e of the first comparator CC_1 and the output terminal 924b of the first NOT gate 920 is coupled to the second output terminal 916f of the first comparator CC_1. The input terminal 926a of the second NOT gate 922 is coupled to the first output terminal 918e of the second comparator CC_2 and the output terminal 926b of the second NOT gate 922 is coupled to the second output terminal 918f of the second comparator CC_2.

[0062] Further, the first transistor M_{RP1}, the second transistor M_{RPN1}, the third transistor M_{RP2} and the fourth transistor M_{RN2} respectively includes a third terminal 908d, 910d, 912d, 914d. The first dynamic body bias unit 902 has a first terminal 928a, a second terminal 928b and a third terminal 928c. The second dynamic body bias unit 904 a first terminal 930a, a second terminal 930b and a third terminal ~~930d~~930c. The first terminal 928a of the first dynamic body bias unit 902 is coupled to the first terminal 908a of the first transistor M_{RP1}, the first terminal 910a of the second transistor M_{RN1}, the second input terminal 916b of the first comparator CC_1 and the third input terminal 918c of the second comparator CC_2. The second terminal 928b of the first dynamic body bias unit 902 is coupled to the second terminal 908b of the first transistor M_{RP1}, the first input terminal 916a of the first comparator CC_1, the first input terminal 918a of the second comparator CC_2, the second terminal 912b of the third transistor M_{RP2} and the second terminal 930b of the second dynamic body bias unit 904. The third terminal 928d of the first dynamic body bias unit 902 is coupled to the third terminal 908d of the first transistor M_{RP1}. The first terminal 930a of the second dynamic body bias unit 904 is coupled to the first terminal 912a of the third transistor M_{RP2}, the first terminal 914a of the fourth transistor M_{RN2}, the third input terminal 916d of the first comparator CC_1 and the second input terminal 918b of the second comparator CC_2. The third terminal 930c of the second dynamic body bias unit 904 is coupled to the third terminal 912d of the third transistor M_{RP2}. The third terminal 910d of the second transistor M_{RPN1} is coupled to the second terminal 910b of the second transistor M_{RPN1}, and the third terminal 914d of the fourth transistor M_{RN2} is coupled to the second terminal 914b of the fourth transistor M_{RN2}.

[0063] The voltage source 906 has a first terminal 932a and a second terminal 932b. The first terminal 932a of the voltage source 906 is coupled to the first terminal 928a of

M_{N4}. The third terminal 1228d of the fourth transistor M_{N5} is coupled to the first terminal 1228a of the fourth transistor MN5.

[0094] In one embodiment, the comparator 1100 may have an output terminal 1350 coupled between the control terminal 1308d of the sixth transistor M_{P4} of the main comparator unit 1102 and the control terminal 1310d of the seventh transistor M_{N3} of the main comparator unit 1102. The comparator 1100 may have a further output terminal ~~1350~~1352 coupled between the second terminal 1308b of the sixth transistor M_{P4} of the main comparator unit 1102 and the second terminal 1310b of the seventh transistor M_{N3} of the main comparator unit 1102.

[0095] In one embodiment, a voltage DCout (e.g. a DC voltage) may be applied to the first input terminal 1106a of the main comparator unit 1102 and the first input terminal 1108a of the secondary comparator unit 1104. A voltage RF+ may be applied to the second input terminal 1106b of the main comparator unit 1102 and the second input terminal 1108b of the secondary comparator unit 1104. A voltage RF- may be applied to the third input terminal 1106c of the main comparator unit 1102 and the third input terminal 1108c of the secondary comparator unit 1104. The voltage RF+ and the voltage RF- may be a positive voltage value and a negative voltage value of an alternating (AC) voltage. A voltage GND (ground) may be applied to the fourth input terminal 1106d of the main comparator unit 1102 and the fourth input terminal 1108d of the secondary comparator unit 1104.

[0096] In one embodiment, the dynamic body bias units 1302, 1304, 1316 may be used to connect the substrate of the transistors M_{P1}, M_{P4}, M_{P7} respectively in the comparator 1100 to a higher potential between RF+/RF- and DCout in order to avoid the breakdown of the device.

[0097] In one embodiment, the first dynamic body bias unit 902 and the second dynamic body bias unit 904 may be used to connect the substrate of M_{RP1} and M_{RP2} in the rectifier 900 to a higher potential between RF+/RF- and DCout in order to avoid the breakdown of the device.

[0098] In one embodiment, the first transistor M_{P1}, the third transistor M_{P2}, the fifth transistor M_{P3}, the sixth transistor M_{P4} of the main comparator unit 1102 are p-channel metal oxide semiconductor field effect transistors (PMOS). The second transistor M_{N1},

with cross-coupled latched comparators to maximize the power conversion efficiency. An 85% of maximum power conversion efficiency may be achieved at low input signal of 1.1 V at 13.56 MHz operating frequency due to the topology of the rectifier 900.

[0123] Regulator

For implantable devices, both power efficiency and off-chip components minimization are crucial. Existing capacitor-less low dropout (LDO) regulator generally has a low loop gain which limits the stability under low output power condition. Figure 19 shows a conventional capacitor-less LDO regulator 1900. The regulator 1900 may have a loop gain of $6g_mr_o$.

[0124] Figure 20 shows a schematic diagram of a regulator 2000 according to one embodiment. The regulator 2000 includes a first transistor T1 and a second transistor T2. The first transistor T1 has a first terminal 2002a, a second terminal 2002b and a control terminal 2002c. The second transistor T2 has a first terminal 2004a, a second terminal 2004b and a control terminal 2004c. The second terminal 2002b of the first transistor T1 is coupled to the first terminal 2004a of the second transistor ~~T1~~T2. The control terminal ~~2002c~~2004c of the ~~first~~second transistor ~~T1~~T2 is coupled to a first voltage reference (e.g. V_{bias}) 2050.

[0125] The regulator 2000 includes a feedback arrangement 2006 coupled between the control terminal 2002c of the first transistor T1 and the second terminal 2004b of the second transistor T2. The feedback arrangement 2006 includes a current comparator 2008, a third transistor T3 and a fourth transistor T4. The current comparator 2008 has an input terminal 2010a and an output terminal 2010b. The third transistor T3 has a first terminal 2012a, a second terminal 2012b and a control terminal 2012c. The fourth transistor T4 has a first terminal 2014a, a second terminal 2014b and a control terminal 2014c.

[0126] The input terminal 2010a of the current comparator 2008 is coupled to the second terminal 2004b of the second transistor T2. The output terminal 2010b of the current comparator 2008 is coupled to the control terminal 2012c of the third transistor T3 and the control terminal 2014c of the fourth transistor T4. The second terminal 2012b of the third transistor T3 is coupled to the second terminal 2014b of the fourth transistor T4 and the control terminal 2002c of the first transistor T1. The first terminal 2014a of

CLAIMS

What is claimed is:

1. A power transfer device, comprising:

a circuit arrangement comprising:

a primary side having a primary coil;

a secondary side having a secondary coil inductively coupled to the primary coil and a load transformation unit;

wherein the load transformation unit comprises an inductor and a capacitor;

wherein the secondary coil, the inductor and the capacitor ~~respectively comprises~~each comprise a first terminal and a second terminal;

wherein the first terminal of the secondary coil is coupled to the first terminal of the capacitor, the second terminal of the capacitor is coupled to the first terminal of the inductor, and the second terminal of the inductor is coupled to the second terminal of the secondary coil.

2. The power transfer device of claim 1,

wherein an optimal resonant load of the load transformation unit is represented by

$$\frac{\omega L_2 \sqrt{1+k^2 Q_1 Q_2}}{Q_2} - j\omega L_2$$

whereby ω is a power carrier frequency, k is a coupling coefficient between the primary coil and the secondary coil, L_2 is an inductance of the secondary coil, Q_1 is a quality factor of the primary coil and Q_2 is a quality factor of the secondary coil.

3. The power transfer device of claim 1 ~~or 2~~, further comprising:

a rectifier comprising:

a first transistor, a second transistor, a third transistor and a fourth transistor ~~respectively~~each having a first terminal, a second terminal and a control terminal;

a first comparator and a second comparator ~~respectively~~each having a first input terminal, a second input terminal, a third input terminal, a fourth input terminal, a first output terminal and a second output terminal;

wherein the first input terminal of the first comparator is coupled to the first input terminal of the second comparator, the second input terminal of the first comparator is coupled to the third input terminal of the second comparator, the third input terminal of the first comparator is coupled to the second input terminal of the second comparator, and the fourth input terminal of the first comparator is coupled to the fourth input terminal of the second comparator;

wherein the first terminal of the first transistor is coupled to the first terminal of the second transistor, the second terminal of the first transistor is coupled to the second terminal of the third transistor, the second terminal of the second transistor is coupled to the second terminal of the fourth transistor, and the first terminal of the third transistor is coupled to the first terminal of the fourth transistor;

wherein the first output terminal of the first comparator is coupled to the control terminal of the first transistor, the second output terminal of the first comparator is coupled to the control terminal of the fourth transistor, the first output terminal of the second comparator is coupled to the control terminal of the third transistor, and the second output terminal of the second comparator is coupled to the control terminal of the second transistor;

wherein the first comparator is configured to compare a first voltage applied to the first input terminal of the first comparator and a second voltage applied to the second input terminal of the first comparator during a first operation cycle, and the second comparator is configured to compare a first voltage applied to the first input terminal of the second comparator and a second voltage applied to the second input terminal of the second comparator during a second operation cycle;

wherein when the second voltage is greater than the first voltage during the first operation cycle, the first comparator is configured to output a first voltage signal at the first output terminal of the first comparator and a second voltage signal at the second output terminal of the first comparator;

wherein when the second voltage is smaller than the first voltage during the first operation cycle, the first comparator is configured to output the second voltage signal at the first output terminal of the first comparator and the first voltage signal at the second output terminal of the first comparator;

wherein when the second voltage is greater than the first voltage during the second operation cycle, the second comparator is configured to output a first voltage signal at the first output terminal of the second comparator and a second voltage signal at the second output terminal of the second comparator;

wherein when the second voltage is smaller than the first voltage during the second operation cycle, the second comparator is configured to output the second voltage signal at the first output terminal of the second comparator and the first voltage signal at the second output terminal of the second comparator.

4. The power transfer device of claim 3,

wherein the first comparator comprises a first NOT gate having an input terminal and an output terminal and the second comparator comprises a second NOT gate having an input terminal and an output terminal;

wherein the input terminal of the first NOT gate is coupled to the first output terminal of the first comparator and the output terminal of the first NOT gate is coupled to the second output terminal of the first comparator;

wherein the input terminal of the second NOT gate is coupled to the first output terminal of the second comparator and the output terminal of the second NOT gate is coupled to the second output terminal of the second comparator.

5. The power transfer device of claim 3~~ or 4~~,

wherein the first transistor, the second transistor, the third transistor and the fourth transistor ~~respectively comprises~~ each comprise a third terminal;

wherein the rectifier further comprises a first dynamic body bias unit having a first terminal, a second terminal and a third terminal, and a second dynamic body bias unit having a first terminal, a second terminal and a third terminal;

wherein the first terminal of the first dynamic body bias unit is coupled to the first terminal of the first transistor, the first terminal of the second transistor, the second input terminal of the first comparator and the third input terminal of the second comparator;

wherein the second terminal of the first dynamic body bias unit is coupled to the second terminal of the first transistor, the first input terminal of the first comparator, the first input terminal of the second comparator, the second terminal of the third transistor and the second terminal of the second dynamic body bias unit;

wherein the third terminal of the first dynamic body bias unit is coupled to the third terminal of the first transistor;

wherein the first terminal of the second dynamic body bias unit is coupled to the first terminal of the third transistor, the first terminal of the fourth transistor, the third input terminal of the first comparator and the second input terminal of the second comparator;

wherein the third terminal of the second dynamic body bias unit is coupled to the third terminal of the third transistor;

wherein the third terminal of the second transistor is coupled to the second terminal of the second transistor and the third terminal of the fourth transistor is coupled to the second terminal of the fourth transistor.

6. The power transfer device of claim 5,

wherein the rectifier further comprises a first input terminal and a second input terminal;

wherein the first input terminal is coupled to the first terminal of the first dynamic body bias unit and the second input terminal is coupled to the first terminal of the second dynamic body bias unit.

7. The power transfer device of claim ~~5 or~~ 6,

wherein the rectifier further comprises a capacitor having a first terminal and a second terminal, and a first output terminal and a second output terminal;

wherein the first terminal of the capacitor is coupled to the first output terminal and the second terminal of the second dynamic body bias unit;

wherein the second terminal of the capacitor is coupled to the second output terminal, the second terminal of the second transistor, the fourth input terminal of the first comparator, the fourth input terminal of the second comparator and the second terminal of the fourth transistor.

8. The power transfer device of claim 7,

wherein the second terminal of the capacitor, the second output terminal, the second terminal of the second transistor, the fourth input terminal of the first comparator, the fourth input terminal of the second comparator and the second terminal of the fourth transistor are coupled to a reference voltage.

9. The power transfer device of ~~any one of claims 6 to 8~~claim 7, further comprising a regulator comprising:

a first transistor and a second transistor ~~respectively~~ each having a first terminal, a second terminal and a control terminal, wherein the second terminal of the first transistor is coupled to the first terminal of the second transistor and a control terminal of the first transistor is coupled to a first voltage reference;

a feedback arrangement coupled between the control terminal of the first transistor and the second terminal of the second transistor;

wherein the feedback arrangement comprises:

a current comparator having an input terminal and an output terminal;

a third transistor and a fourth transistor ~~respectively~~each having a first terminal, a second terminal and a control terminal;

wherein the input terminal of the current comparator is coupled to the second terminal of the second transistor, and the output terminal of the

current comparator is coupled to the control terminal of the third transistor and the control terminal of the fourth transistor;

wherein the first terminal of the third transistor is coupled to the first voltage reference and the second terminal of the third transistor is coupled to the second terminal of the fourth transistor and the control terminal of the first transistor;

wherein the first terminal of the fourth transistor is coupled to a second voltage reference.

10. The power transfer device of claim 9,

wherein the regulator further comprises a fifth transistor having a first terminal, a second terminal and a control terminal;

wherein the first terminal of the fifth transistor is coupled to the second voltage reference, the second terminal of the fifth transistor is coupled to the second terminal of the second transistor, and the control terminal of the fifth transistor is coupled to a third voltage reference.

11. The power transfer device of claim 9 ~~or 10~~,

wherein the regulator further comprises:

an input terminal coupled to the first terminal of the first transistor and the first terminal of the third transistor;

an output terminal coupled between the second terminal of the first transistor and the first terminal of the second transistor.

12. The power transfer device of ~~any one of~~ claims 9 ~~to 11~~,

wherein the rectifier is coupled between the circuit arrangement and the regulator.

13. The power transfer device of claim 11 ~~or 12~~,

wherein the first input terminal of the rectifier is coupled to the first terminal of the inductor of the load transformation unit of the circuit arrangement, and the second

input terminal of the rectifier is coupled to the second terminal of the inductor of the load transformation unit of the circuit arrangement;

wherein the first output terminal of the rectifier is coupled to the input terminal of the regulator.

14. The power transfer device of ~~any one of~~ claims ~~1 to 13~~,

wherein the power transfer device is a wireless power link device.

15. A rectifier, comprising:

a first transistor, a second transistor, a third transistor and a fourth transistor ~~respectively~~each having a first terminal, a second terminal and a control terminal;

a first comparator and a second comparator respectively having a first input terminal, a second input terminal, a third input terminal, a fourth input terminal, a first output terminal and a second output terminal;

wherein the first input terminal of the first comparator is coupled to the first input terminal of the second comparator, the second input terminal of the first comparator is coupled to the third input terminal of the second comparator, the third input terminal of the first comparator is coupled to the second input terminal of the second comparator, and the fourth input terminal of the first comparator is coupled to the fourth input terminal of the second comparator;

wherein the first terminal of the first transistor is coupled to the first terminal of the second transistor, the second terminal of the first transistor is coupled to the second terminal of the third transistor, the second terminal of the second transistor is coupled to the second terminal of the fourth transistor, and the first terminal of the third transistor is coupled to the first terminal of the fourth transistor;

wherein the first comparator is configured to compare a first voltage applied to the first input terminal of the first comparator and a second voltage applied to the second input terminal of the first comparator during a first operation cycle, and the second comparator is configured to compare a first voltage applied to the first input terminal of the second comparator and a second voltage applied to the second input terminal of the second comparator during a second operation cycle;

wherein when the second voltage is greater than the first voltage during the first operation cycle, the first comparator is configured to output a first voltage signal at the first output terminal of the first comparator and a second voltage signal at the second output terminal of the first comparator;

wherein when the second voltage is smaller than the first voltage during the first operation cycle, the first comparator is configured to output the second voltage signal at the first output terminal of the first comparator and the first voltage signal at the second output terminal of the first comparator;

wherein when the second voltage is greater than the first voltage during the second operation cycle, the second comparator is configured to output a first voltage signal at the first output terminal of the second comparator and a second voltage signal at the second output terminal of the second comparator;

wherein when the second voltage is smaller than the first voltage during the second operation cycle, the second comparator is configured to output the second voltage signal at the first output terminal of the second comparator and the first voltage signal at the second output terminal of the second comparator.

16. The rectifier of claim 15,

wherein the first transistor, the second transistor, the third transistor and the fourth transistor ~~respectively comprises~~each comprise a third terminal;

wherein the rectifier further comprises a first dynamic body bias unit having a first terminal, a second terminal and a third terminal, and a second dynamic body bias unit having a first terminal, a second terminal and a third terminal;

wherein the first terminal of the first dynamic body bias unit is coupled to the first terminal of the first transistor, the first terminal of the second transistor, the second input terminal of the first comparator and the third input terminal of the second comparator;

wherein the second terminal of the first dynamic body bias unit is coupled to the second terminal of the first transistor, the first input terminal of the first comparator, the first input terminal of the second comparator, the second terminal of the third transistor and the second terminal of the second dynamic body bias unit;

wherein the third terminal of the first dynamic body bias unit is coupled to the third terminal of the first transistor;

wherein the first terminal of the second dynamic body bias unit is coupled to the first terminal of the third transistor, the first terminal of the fourth transistor, the third input terminal of the first comparator and the second input terminal of the second comparator;

wherein the third terminal of the second dynamic body bias unit is coupled to the third terminal of the third transistor;

wherein the third terminal of the second transistor is coupled to the second terminal of the second transistor and the third terminal of the fourth transistor is coupled to the second terminal of the fourth transistor.

17. The rectifier of claim 16, further comprising:

a first input terminal and a second input terminal;

wherein the first input terminal is coupled to the first terminal of the first dynamic body bias unit and the second input terminal is coupled to the first terminal of the second dynamic body bias unit.

18. The rectifier of claim ~~16 or~~ 17, further comprising:

a capacitor having a first terminal and a second terminal, and a first output terminal and a second output terminal;

wherein the first terminal of the capacitor is coupled to the first output terminal and the second terminal of the second dynamic body bias unit;

wherein the second terminal of the capacitor is coupled to the second output terminal, the second terminal of the second transistor, the fourth input terminal of the first comparator, the fourth input terminal of the second comparator and the second terminal of the fourth transistor.

19. The rectifier of claim 18,

wherein the second terminal of the capacitor, the second output terminal, the second terminal of the second transistor, the fourth input terminal of the first comparator,

the fourth input terminal of the second comparator and the second terminal of the fourth transistor are coupled to a reference voltage.

20. A regulator, comprising:

a first transistor and a second transistor ~~respectively~~each having a first terminal, a second terminal and a control terminal, wherein the second terminal of the first transistor is coupled to the first terminal of the second transistor, a first terminal of the first transistor is coupled to a first voltage reference and a control terminal of the second transistor is coupled to a second voltage reference;

a feedback arrangement coupled between the control terminal of the first transistor and the second terminal of the second terminal;

wherein the feedback arrangement comprises:

a current comparator having an input terminal and an output terminal;

a third transistor and a fourth transistor ~~respectively~~each having a first terminal, a second terminal and a control terminal;

wherein the input terminal of the current comparator is coupled to the second terminal of the second ~~terminal~~transistor, and the output terminal of the current comparator is coupled to the control terminal of the third transistor and the control terminal of the fourth transistor;

wherein the first terminal of the third transistor is coupled to the first voltage reference and the second terminal of the third transistor is coupled to the second terminal of the fourth transistor and the control terminal of the first transistor;

wherein the first terminal of the fourth transistor is coupled to a third voltage reference.

21. The regulator of claim 20, further comprising:

a fifth transistor having a first terminal, a second terminal and a control terminal;

wherein the first terminal of the fifth transistor is coupled to the third voltage reference, the second terminal of the fifth transistor is coupled to the second terminal of

the second transistor, and the control terminal of the fifth transistor is coupled to a third voltage reference.