[0160] Note that the invention is not limited to such a configuration. For example, the connection state designation circuit 11 may cause all of the switches SWa[1] to SWa[M] to be turned OFF during the control period TA2.

[0161] As illustrated in FIG. 10A, the signal distribution circuit 15 sets a pulse PlsS1 (at which the signal is set to the high level) to the determination signal SigS at the start timing of the control waveform signal Tsig1, and sets a pulse PlsS2 (at which the signal is set to the high level) to the designation signal SigS at the end timing of the control waveform signal Tsig3. Specifically, the designation signal SigS includes the pulse PlsS1 at the time t-11 (at which the signal is set to the high level), and includes the pulse PlsS2 at the time t-32 (at which the signal is set to the high level). The designation signal SigS defines the control period TS from the time t-11 to the time t-32 using the pulses PlsS1 and PlsS2. Note that the control period TS is a period in which the connection state of each switch SWs is maintained (e.g., ON or OFF state).

[0162] Note that the designation signal SigS illustrated in FIG. 10A is merely an example. The designation signal SigS may be an arbitrary signal as long as the designation signal SigS can define the control period TS. For example, the designation signal SigS may be a signal that is set to the high level during the control period TS, and set to the low level during a period other than the control period TS, as illustrated in FIG. 10C.

[0163] The connection state designation circuit 11 generates the connection state designation signals SLs[1] to SLs[M] that ON/OFF-control the switches SWs[1] to SWs[M] based on at least one signal among (at least part of) the individual designation signals Sd[1] to Sd[M], the designation signal SigS, and the determination signal SigT.

[0164] As illustrated in FIG. 10A, the connection state designation circuit 11 sets the connection state designation signals SLs[1] to SLs[M] to the low level so that the switches SWs[1] to SWs[M] are turned OFF during a period other than the control period TS.

[0165] The connection state designation circuit 11 sets the connection state designation signals SLs[1] to SLs[M] to the signal levels that respectively correspond to the individual designation signals Sd[1] to Sd[M] so that the switches SWs[1] to SWs[M] are turned ON or OFF corresponding to the individual designation signals Sd[1] to Sd[M] that are supplied to the connection state designation circuit 11 at a timing at which the pulse PlsT1 occurs during the control period TS that starts at the rising edge of the pulse PlsS1. More specifically, the connection state designation circuit 11 sets the connection state designation signal SLs[m] to the high level so that the switch SWs[m] (SWs-O[m]) is turned ON during the control period TS when the individual designation signal Sd[m] designates the ejecting section D[m] as the diagnosis target. The connection state designation circuit 11 sets the connection state des-

to “1” (i.e., when the head unit HU performs the diagnosis process in the diagnosis period TQ), the individual designation signal Sd[m] that is supplied to the head unit HU during the start-up period TP that precedes the diagnosis period TQ represents a value (1, 1) that designates the ejecting section D[m] as the diagnosis target, or a value (0, 0) that does not designate the ejecting section D[m] as the diagnosis target.

[0235] When the individual designation signal Sd[m] represents the value (1, 1), the decoder DCa[m] outputs the connection state designation signal SLa[m] that is set to the high level during the control periods TA1 and TA3, and is set to the low level during the control period TA2 (see FIG. 14A). In this case, the switch SWa[m] (SWa-O[m]) is turned ON during the control periods TA1 and TA3, and is turned OFF during the control period TA2 (as described above with reference to FIG. 10A, for example).

[0236] When the individual designation signal Sd[m] represents the value (0, 0), the decoder DCa[m] sets the signal level of the connection state designation signal SLa[m] so that the connection state designation signal SLa[m] is set to the high level during the control periods TA1 to TA3 (see FIG. 14A). In this case, the switch SWa[m] (SWa-O[m]) is turned ON during the control periods TA1 to TA3 (as described above with reference to FIG. 10A, for example).

[0237] As illustrated in FIG. 14B, when the operation mode designation signal Md is set to “2” (i.e., when the inkjet printer 1 performs the printing process during the normal operation period TR), the individual designation signal Sd[m] that is supplied to the head unit HU prior to the start of the unit period Tu represents a value (1, 1) that designates formation of a large dot, a value (1, 0) that designates formation of a medium dot, a value (0, 1) that designates formation of a small dot, or a value (0, 0) that designates formation of no dot.

[0238] When the individual designation signal Sd[m] represents the value (1, 1) (see FIG. 14B), the decoder DCa[m] sets the signal level of the connection state designation signal SLa[m] so that the connection state designation signal SLa[m] is set to the high level during the print control periods Tu1 and Tu2. In this case, the switch SWa[m] is turned ON during the print control periods Tu1 and Tu2. Therefore, the ejecting section D[m] is driven by the waveform PAX and the waveform PAY, and ejects a large volume of ink during the unit period Tu.

[0239] When the individual designation signal Sd[m] represents the value (1, 0) (see FIG. 14B), the decoder DCa[m] sets the signal level of the connection state designation signal SLa[m] so that the connection state designation signal SLa[m] is set to the high level during the print control period Tu1, and is set to the low level during the print control period Tu2. In this case, the switch SWa[m] is turned ON during the print control period Tu1, and is turned OFF during the print control period Tu2. Therefore,

is performed), the operation of the decoder DCa2[m] is the same as that of the decoder DCa[m] according to the first embodiment during the printing process, as illustrated in FIG. 14B.

[0312] As illustrated in FIG. 19A, when the operation mode designation signal Md is set to "2", and the check execution signal SP is set to "1" (i.e., when the ejection state check process is performed), the individual designation signal Sd[m] represents a value (1, 1) that designates the ejecting section D[m] as the check target ejecting section D-K, or a value (0, 0) that does not designate the ejecting section D[m] as the check target ejecting section D-K.

[0313] When the individual designation signal Sd[m] represents the value (1, 1) that designates the ejecting section D[m] as the check target ejecting section D-K, the decoder DCa2[m] outputs the connection state designation signal SLa[m] that is set to the high level during the control periods TSS1 and TSS3, and is set to the low level during the control period TSS2. In this case, as illustrated in FIG. 17, the switch SWa (SWa-K[m]) that corresponds to the ejecting section D[m] designated as the check target ejecting section D-K[m] is turned ON during the control periods TSS1 and TSS3, and is turned OFF during the control period TSS2.

[0314] When the individual designation signal Sd[m] represents the value (0, 0) that does not designate the ejecting section D[m] as the check target ejecting section D-K, the decoder DCa2[m] outputs the connection state designation signal SLa[m] that is set to the low level during the control periods TSS1 to TSS3. In this case, as illustrated in FIG. 17, the switches SWa other than the switch SWa-K[m] are turned OFF during the control periods TSS1 to TSS3.

[0315] When the operation mode designation signal Md is set to "1" (i.e., when the diagnosis process is performed), the operation of the decoder DCa2[m] is the same as that of the decoder DCa[m] according to the first embodiment during the diagnosis process (see FIG. 14A) regardless of the value of the individual designation signal Sd.

[0316] FIG. 19B illustrates the generation of the connection state designation signal SLs[m] by the decoder DCs2[m].

[0317] As illustrated in FIG. 19B, when the operation mode designation signal Md is set to "2", and the check execution signal SP is set to "0" (i.e., when the printing process is performed), the decoder DCs2[m] outputs the connection state designation signal SLs[m] that is set to the low level during the print control periods Tu1 and Tu2 in the same manner as the decoder DCa[m] according to the first embodiment.

[0318] As illustrated in FIG. 19B, when the operation mode designation signal Md is set to "2", the check execution signal SP is set to "1" (i.e., when the ejection state check process is performed), and the individual designation signal Sd[m] represents the value (1, 1) that designates the ejecting section D[m] as the check target ejecting section D-