LDMOS WITH NO REVERSE RECOVERY

TECHNICAL FIELD

The present disclosure relates generally to semiconductor devices, and more particularly to a lateral double-diffused metal oxide semiconductor (LDMOS) device.

BACKGROUND

Voltage regulators, such as DC to DC converters, are used to provide stable voltage sources for electronic systems. Efficient DC to DC converters are particularly needed for power management in low power devices, such as laptop notebooks and cellular phones. Switching voltage regulators (or simply "switching regulators") are known to be an efficient type of DC to DC converter. A switching regulator generates an output voltage by converting an input DC voltage into a high frequency voltage, and filtering the high frequency input voltage to generate the output DC voltage. Specifically, the switching regulator includes a switch for alternately coupling and decoupling an input DC voltage source, such as a battery, to a load, such as an integrated circuit. An output filter, typically including an inductor and a capacitor, is coupled between the input voltage source and the load to filter the output of the switch and thus provide the output DC voltage. A controller, such as a pulse width modulator or a pulse frequency modulator, controls the switch to maintain a substantially constant output DC voltage.

LDMOS (laterally diffused metal oxide semiconductor) transistors are used in switching regulators as a result of their specific on-resistance and drain-to-source breakdown voltage.

SUMMARY

In one aspect, a transistor includes a source region including a first impurity region implanted into a substrate, a drain region including a second impurity region implanted into the substrate, and a gate including an oxide layer formed over the substrate and a conductive material formed over the oxide layer, the oxide layer comprising a first side and a second side, the first side formed over a portion of the first impurity region and the second side formed over a portion of the second impurity region, the first side having a thickness of less than about 100Å, and the second side having a thickness equal to or greater than 125Å.

Implementations may include one or of the following features. The thickness of the second side may be at least five times the thickness of the first side. The thickness of the first

side may be about 70Å or less. The thickness of the first side may be about 35Å or less. The source may include a third self-aligned impurity region. A maximum doping concentration of the third impurity region may be between about $1x10^{17}$ atoms/cm^2 and $1x10^{18}$ atoms/cm^2. A doping concentration of the third impurity region at a surface adjacent to the oxide layer may be less than about $5x10^{17}$ atoms/cm^2. The doping concentration may be less than about $3x10^{17}$ atoms/cm^2. The third impurity region may be positioned in a current path of the transistor. The second side may have a thickness of between approximately 120Å and 800Å, e.g., between approximately 200Å and 400Å. The transistor may be a lateral double-diffused metal oxide semiconductor (LDMOS).

In another aspect, a transistor includes a source region including a first impurity region implanted into a substrate, a drain region including a second impurity region implanted into the substrate, and a gate including an oxide layer formed over the substrate and a conductive material formed over the oxide layer, the oxide layer comprising a first side and a second side, the first side formed over a portion of the first impurity region and the second side formed over a portion of the second impurity region, the first side having a thickness such that a turn-on voltage of the transistor is less than 0.6V.

Implementations may include one or of the following features. The turn-on voltage of the transistor may be between 0.4 and 0.5V. The source may include a third self-aligned impurity region. A maximum doping concentration of the third impurity region may be between about $1x10^{17}$ atoms/cm^2 and $1x10^{18}$ atoms/cm^2. A doping concentration of the third impurity region at a surface adjacent to the oxide layer may be less than about $5x10^{17}$ atoms/cm^2. The doping concentration may be less than about $3x10^{17}$ atoms/cm^2. The third impurity region may be positioned in a current path of the transistor. The transistor may be a lateral double-diffused metal oxide semiconductor (LDMOS).

In another aspect, a transistor includes a source region including a first impurity region implanted into a substrate, a drain region including a second impurity region implanted into the substrate, an intrinsic diode, and a gate including an oxide layer formed over the substrate and a conductive material formed over the oxide layer, the oxide layer comprising a first side and a second side, the first side formed over a portion of the first impurity region and the second side formed over a portion of the second impurity region, the first side having a thickness such that a turn-on voltage of the transistor is less than a turn-on voltage of the intrinsic diode.

Implementations may include one or of the following features. The turn-on voltage of the transistor is between 0.4 and 0.6V. The source may include a third self-aligned impurity region. A maximum doping concentration of the third impurity region may be between about $1x10^{17}$ atoms/cm^2 and $1x10^{18}$ atoms/cm^2. A doping concentration of the third impurity region at a surface adjacent to the oxide layer may be less than about $5x10^{17}$ atoms/cm^2. The doping concentration may be less than about $3x10^{17}$ atoms/cm^2. The third impurity region may bes positioned in a current path of the transistor. The transistor may be a lateral double-diffused metal oxide semiconductor (LDMOS).

In another aspect, a method of making a transistor includes applying a photoresist over a gate, the gate including an oxide layer formed over a substrate and a conductive material formed over the oxide layer, using the photoresist as a mask, etching the gate to remove a portion of the conductive material, and using the photoresist and conductive material as a mask, implanting an impurity region into the substrate such that the impurity region is self-aligned to the gate.

Implementations may include one or of the following features. The oxide layer may be formed such that a first side of the oxide layer is thinner than a second side of the oxide layer. The first side may have a thickness of less than about 100Å, and the second side may have a thickness that it at least fie times the thickness of the first side. The photoresist may be less than about 0.5μm thick. Implanting an impurity region may include bombarding the substrate with atoms at an angle that is less than 90° from a main surface of the substrate. Implanting an impurity regions may continues until a doping concentration of the substrate is between about $1x10^{13}$ atoms/cm^2 and $5x10^{18}$ atoms/cm^2.

In another aspect, a method of making a transistor includes etching a first side of a gate, the gate including an oxide layer formed over a substrate and a conductive material formed over the oxide layer, the etching removing a first portion of the conductive material, implanting an impurity region into the substrate such that the impurity region is self-aligned, and etching a second side of the gate to remove a second portion of the conductive material.

Implementations may include one or of the following features. The oxide layer may be formed such that a first side of the oxide layer is thinner than a second side of the oxide layer. The first side may have a thickness of less than about 100Å, and the second side may have a thickness that it at least fie times the thickness of the first side. Implanting an impurity region may include bombarding the substrate with atoms at an that is less than 90° from a main surface of the substrate. Implanting the impurity region may continue until a

doping concentration of the substrate is between about $1x10^{13}$ atoms/cm^2 and $5x10^{18}$ atoms/cm^2.

In another aspect, a method of making a transistor includes applying a first photoresist over a gate, the gate including an oxide layer formed over a substrate and a conductive material formed over the oxide layer, using the first photoresist as a mask, etching a first side of the gate to remove a first portion of the conductive material, implanting an impurity region into the substrate such that the impurity region is self-aligned, applying a second photoresist over the gate, and using the second photoresist as a mask, etching a second side of the gate to remove a second portion of the conductive material.

In another aspect, a method of making a integrated circuit includes forming a plurality of LDMOS transistors on a substrate, each LDMOS transistor including a gate oxide layer comprising a first side closer to a source side of the LDMOS transistor and a second side closer to the drain side of the LDMOS transistor, the first side having a thickness of less than about 100Å, and the second side having a thickness equal to or greater than 125Å, and forming a plurality of CMOS transistor on the substrate, wherein each CMOS transistor includes a gate oxide layer, and wherein forming the gate oxide layer of the CMOS transistor occurs simultaneously with forming the first side of the gate oxide layer of the LDMOS transistor.

Implementations may include one or of the following features. The gate of oxide layer of the CMOS transistor may be formed with the same thickness as the first side of the gate oxide layer of the LDMOS transistor. The thickness of the second side may be at least five times the thickness of the first side. The thickness of the first side may be about 70Å or less, e.g., about 35Å or less. Forming the plurality of LDMOS transistors may include depositing an LDMOS gate conductor and forming the plurality of CMOS transistor may include depositing a CMOS gate conductor, and the LDMOS gate conductor and CMOS gate conductor may be deposited simulataneously. The LDMOS gate conductor and CMOS gate conductor may be polysilicon. The gate oxide layer of the CMOS gate may have a substantially uniform thickness.

Certain implementations may have one or more of the following advantages. A transistor having a gate oxide that is less than about 40Å can make the turn-on voltage of the transistor be less than the turn-on voltage of the intrinsic diode. A transistor having a turn-on voltage that is less than the turn-on voltage of the intrinsic diode can reduce the recovery time of the transistor. Reducing the recovery time can increase the efficiency of the transistor,

particularly at high switching rates. Applying a photoresist over the gate before implanting the p-body can give an added layer of protection to avoid unwanted implantation of impurities in the substrate. Etching through the polygate a first time before implanting the p-body and then etching through the polygate a second time after implanting the p-body ensures that a p-body is implanted only on the source side of the transistor, rather than on both the source and the drain side.

The details of one or more embodiments are set forth in the accompanying drawings and the description below. Other features, aspects, and advantages will become apparent from the description, the drawings, and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram of a buck converter.

FIG. 2 is a simplified circuit diagram of a buck converter.

FIG. 3 is a graph demonstrating the deadtime of a traditional buck converter.

FIG. 4 is a schematic of an LDMOS transistor.

FIGS. 5A and 5B are schematics of an exemplary impurity profile in a transistor as described herein.

FIG. 6 is a graph of doping vs. distance from the surface for a transistor having a thin gate oxide thickness of 35Å, 70Å, and 125Å, respectively.

FIGS. 7A and 7B are a chart, and corresponding graph, showing the characteristics of a transistor having a thin gate oxide thickness of 35Å.

FIGS. 8A and 8B are a chart, and corresponding graph, showing the characteristics of a transistor having a thin gate oxide thickness of 70Å.

FIG. 9A and 9B are a chart, and corresponding graph, showing the characteristics of a transistor having a thin gate oxide thickness of 125Å.

FIGS. 10A-10K show an exemplary process of forming a transistor.

Like reference numbers and designations in the various drawings indicate like elements.

DETAILED DESCRIPTION

When a transistor is used in synchronous rectification in a switching regulator, efficiency losses occur as a result of reverse recovery of the intrinsic body diode charge up during deadtime, as well as diode conduction during deadtime. By having a transistor in which the turn-on voltage of the transistor is less than the turn-on voltage of the intrinsic

diode, the efficiency of the switching regulator can be enhanced by reducing both mechanisms of loss associated with parasitic diodes. The lower threshold voltage prevents minority carrier storage. Moreover, the conduction losses during deadtime will decrease by the ratio of threshold voltage to diode turn-on voltage.

Referring to FIG. 1, a switching regulator 10 is coupled to a first high DC input voltage source 12, such as a battery, by an input terminal 20. The switching regulator 10 is also coupled to a load 14, such as an integrated circuit, by an output terminal 24. The switching regulator 10 serves as a DC-to-DC converter between the input terminal 20 and the output terminal 24. The switching regulator 10 includes a switching circuit 16 which serves as a power switch for alternately coupling and decoupling the input terminal 20 to an intermediate terminal 22. The switching circuit 16 includes a rectifier, such as a switch or diode, coupling the intermediate terminal 22 to ground. Specifically, the switching circuit 16 may include a first transistor 40, called a high-side transistor, having a source connected to the input terminal 20 and a drain connected to the intermediate terminal 22 and a second transistor 42, called a low-side transistor, or synchronous transistor, having a source connected to ground and a drain connected to the intermediate terminal 22.

In one implementation, the first transistor 40 can be a Positive-Channel Metal Oxide Semiconductor (PMOS) transistor, and the second transistor 42 can be a Negative-Channel Metal Oxide Semiconductor (NMOS) transistor. In another implementation, the first transistor 40 and the second transistor 42 can both be NMOS transistors. In another implementation, the first transistor 40 can be a PMOS, NMOS, or a Lateral Double-diffused Metal Oxide Semiconductor (LDMOS), and the second transistor 42 can be an LDMOS.

The intermediate terminal 22 is coupled to the output terminal 24 by an output filter 26. The output filter 26 converts the rectangular waveform of the intermediate voltage at the intermediate terminal 22 into a substantially DC output voltage at the output terminal 24. Specifically, in a buck-converter topology, the output filter 26 includes an inductor 44 connected between the intermediate terminal 22 and the output terminal 24 and a capacitor 46 connected in parallel with the load 14. During a high-side conduction period, the first transistor is closed, and the source 12 supplies energy to the load 14 and the inductor 44 via the first transistor 40. On the other hand, during a low-side conduction period, the second transistor 42 is closed, and current flows through the second transistor 42 as energy is supplied by the inductor 44. The resulting output voltage V_{out} is a substantially DC voltage.

The switching regulator also includes a controller 18, a high-side driver 80 and a low-side driver 82 for controlling the operation of the switching circuit 16. A first control line 30 connects the high-side transistor 40 to the high-side driver 80, and a second control line 32 connects the low-side transistor 42 to the low-side driver 82. The high-side and low-side drivers are connected to the controller 18 by control lines 84 and 86, respectively. The controller 18 causes the switching circuit 16 to alternate between high-side and low-side conduction periods so as to generate an intermediate voltage Vint at the intermediate terminal 22 that has a rectangular waveform. The controller 16 can also include a feedback circuit (not shown), which measures the output voltage and the current passing through the output terminal. Although the controller 18 is typically a pulse width modulator, the invention is also applicable to other modulation schemes, such as pulse frequency modulation.

A simplified circuit diagram of a buck converter 200 is shown in FIG. 2. The buck converter 200 includes a high-side transistor 40, a low-side transistor 42, and an inductor 206. Each transistor has a corresponding intrinsic body diode, 212 and 214, respectively. A voltage V_{in}, for example 12V, is applied to the high-side transistor 40, and when the high-side transistor 40 is on, current will flow through the transistor 40 and the inductor 206. In contrast, when the low-side transistor 42 is on, the inductor 206 will pull current from ground. Under normal operation of the buck circuit 200, the regulator will switch between turning the high-side transistor 40 and the low-side transistor 42 on so that the output of the filter 26 produces the desired voltage V_{out} (V_{out} somewhere between 0V and V_{in}).

To improve efficiency of the buck converter 200, it is desirable to have the high-side transistor 40 on while the low-side transistor 42 is off, and vice versa. However, some downtime is required between the switching in order to avoid having both transistors 40, 42 on and at same time, which can cause shoot-through and result in significant efficiency losses and damage to the transistors. Thus, there is a short period, the intrinsic deadtime t_d, between each high-side conduction and low-side conduction period in which both transistors are open.

When both transistors 40, 42 are off, current through the inductor 206 will not instantly drop to zero. The voltage across the inductor is determined by Equation 1:

$$V = L(di/dt), \qquad \text{(Equation 1)}$$

where V is the voltage, L is the inductance, and i is the current in the inductor. As the inductor current decreases, the voltage at the input end, i.e. near V_{in}, of the inductor is forced

to be negative. When this voltage reaches approximately -0.7 V, the low-side body diode 214 reaches its threshold voltage and begins conducting current into the inductor. As a result, in a traditional buck converter, the current will travel through the diode 214.

When the current flows through the low-side diode, a number of losses in efficiency can result. The most significant loss is associated with reverse recovery. The reverse recovery loss is the loss associated with taking the forward conducting diode from forward to reverse bias. Reverse recovery occurs when the high-side transistor is switched on. In the period before the high-side transistor is switched on, the low-side body diode is forward biased with the inductor drawing current through the diode from ground. In this state, the PN junction of the low-side diode conducts, the depletion region is narrowed to its minimum width, and a buildup of charge carriers is formed on each side of the diode's PN junction. When the high-side transistor is switched on, the low-side diode goes from being forward biased at 0.7 V to being negative biased at -12 V. However, the low-side diode does not instantaneously switch off because the same buildup of charge carriers that allowed conduction across the PN junction during forward bias causes a transient charge to be depleted in negative bias. The reverse recovery loss is thus a current that flows through the high-side transistor in order to restore the equilibrium reverse-biased charge across the low-side's PN junction.

The total amount of the diode recovery loss depends upon the output current, the parasitic inductance, and the high side drive capability. As shown in FIG. 3, the total deadtime t includes both the intrinsic deadtime t_d and the reverse recovery time t_s. The reverse recovery time t_s can account for a large fraction, e.g. more than 25% of the deadtime of the transistor.

FIG. 4 shows a schematic cross-sectional view of an LDMOS transistor 400 that could be used, for example, as a transistor in a buck converter, e.g., as the low side transistor 42, as discussed above. The LDMOS transistor 400 can be fabricated on a high voltage n-type well 402 implanted in a p type substrate 404. A high voltage n-well implant is typically a deep implant and is generally more lightly doped relative to a CMOS n-well. The LDMOS transistor 400 includes a drain region 406, a source region 410, and a gate 412 with a stepped gate oxide layer 424. The drain region 406 includes a doped n+ region 414 and an n doped shallow drain 416. The source region includes an n-doped n+ region 418, a p-doped p+ region 420, and a p-doped p-body 422. The impurities that provide the n-well 402, the n-doped shallow drain 416, and the n+ regions 414, 418 are a first type of doping material, for

example phosphorous. Both the n-doped shallow drain 416 and the n-well 402 have lower concentrations of impurities than the n+ regions 414, 418. Likewise, the impurities that provide the p+ region 420 and the p-body 422 are a second opposite type of doping material, for example boron. The p-body 422 can be self-aligned with the gate 412. In other words, the source-side edge of the gate and the gate-side edge of the p-body can be substantially aligned (subject to implantation effects that can force a portion of the p-body 422 below the gate). Alternatively, the p-body 422 need not be self-aligned with the gate 412.

The p-body can have a maximum doping concentration of, for example, $1x10^{17}$ atoms/cm^2 to $1x10^{18}$ atoms/cm^2. Moreover, the doping concentration at the top surface 422a of the p-body can be less than about $5x10^{17}$ atoms/cm^2, such as less than $3x10^{17}$ atoms/cm^2, for example $2x10^{17}$ atoms/cm^2. Exemplary doping profile is shown in FIGS.. 5A and 5B.

Referring back to FIG. 4, the oxide layer 424 is located underneath the gate 412 and includes two portions, thin portion 424a and thick portion 424b. Thin portion 424a can be closer to the source 410 than thick portion 424b and can partially overlap the n+ region 418 and the p-body 422. Thick portion 424b can be closer to the drain 406 than thin portion 424a and can partially overlap the n+ region 414 and the shallow drain 406. As shown in FIG. 4, thin portion 424a can be thinner than thick portion 424b. Thin portion 424a can be less than 100 Å thick, such as less than 40Å thick, for example 35 Å. In contrast, thick portion 424b can be at least five times as thick as the thin portion 424a, such as at least 10 times as thick, for example between 200Å and 400Å thick.

For the LDMOS transistor 400, a high enough positive voltage on the gate 412, called the turn-on voltage (V_t), will push the positive holes of the p-body 422 away from the gate 412 to form a depletion layer. This will create a channel for electrons (n) (an "n-channel") to flow between the source 410 and the drain 406. Varying the voltage between the gate 412 and the substrate 404 modulates the conductivity of the n-channel and makes it possible to control the current flow between drain and source.

The thin portion 424a of the oxide layer 424, in combination with having a p-body profile as described above, can affect the turn-on voltage (V_t) of the gate and transistor. As the thin portion 242a is made thinner, the turn-on voltage will be reduced. Further, the lower the concentration of the p-body, the lower the turn-on voltage. .

By appropriate selection of the thickness of the thin portion of the oxide layer and reducing the concentration of the p-body, the turn-on voltage (V_t) of the transistor can be less than the turn-on voltage (V_{be}) of the intrinsic diode. For example, the turn-on voltage of the

transistor can be less than 0.6V. Advantageously, by making V_t less than V_{be} for the low-side transistor of a buck converter, the transistor can enter third-quadrant conduction during deadtime, causing current to travel through the transistor instead of the body diode.

Lowering V_t such that the current goes through the transistor instead of the body diode can eliminate the reverse recovery time, thereby greatly enhancing the efficiency of the buck converter. Additionally, power is saved because there is no need to discharge the minority carriers that would otherwise form the reverse recovery charge on the body diode during reverse conduction. If the turn-on voltage of the transistor is too low, however, the ringing caused by switching between the high-side transistor and low-side transistor can unintentionally activate the gate. Therefore, the thickness of the thin portion and the concentration of the p-body can be balanced such that the turn-on voltage of the transistor is between 0.4V and 0.5V.

FIG. 6 shows an exemplary graph of net doping vs. distance into the p-body from a top surface of the p-body 422a (along the line 502 from FIG. 5). In the exemplary embodiments shown in FIG. 6, a thin oxide layer of 35Å requires a surface doping concentration of approximately $2x10^{17}$ atoms/cm^2. A thin oxide layer of 70 Å requires a surface doping concentration of approximately $5x10^{16}$. Moreover, a thin oxide layer of 125Å requires a surface doping concentration of less than $1x10^{16}$. Therefore, the thinner the thin oxide layer is, the greater the maximum doping concentration can be to achieve a V_t that is less than V_{be}.

As shown in the exemplary embodiments of FIGS. 7A-8B, a device having a thin oxide, e.g. less than 100Å, such as 35Å (FIGS. 7A-7B) or 70Å (FIGS. 8A-8B), and the proper p-body concentration, a current through the transistor (IS) can be much greater than the current through the diode (IB). Moreover, provided that the applied voltage is between approximately 0.4V and 0.8V, no current will go through the diode. However, referring to FIGS. 9A and 9B, if the thin oxide thickness rises to above 100Å, such as 125Å, then a much smaller voltage window, e.g. between 0.65 and 0.8V is available in which no current goes through the diode. Moreover, more doping steps are required to get the necessary p-body concentration.

Varying the Vt of the low-side transistor requires additional semiconductor processing steps. To achieve a Vt of approximately 0.4 V, it is helpful to fashion the transistor so that the oxide beneath the gate is thinner where it contacts the source of the transistor than where it contacts the drain of the transistor because the thinner the oxide, the lower the Vt for a

given surface doping. This thin oxide is not suitable for the drain side of the gate, however, because it would compromise the breakdown voltage (BVDSS) of the transistor. Accordingly, the must be shaped as a "step," with the drain side being thicker than the source side.

Referring to FIG. 10A, the process of making the transistor begins by forming an oxide layer 424 on a silicon layer 110.

Referring to FIG. 10B, the oxide layer is patterned to define the gate oxide regions. In addition, a step 902 is formed in the oxide layer 424, creating a thin oxide portion 424a and a thick oxide portion 424b. The thin oxide portion 424a can be on the source side of the gate, whereas the thick oxide portion 424b can be on the drain side of the gate. The step 902 could be formed before or after the oxide layer is patterned. The thin oxide portion 424a can also be deposited simultaneously on any CMOS devices on the substrate, e.g., using a single mask.

In some implementation, the step 902 in the oxide can be formed by growing a thin oxide layer, masking the substrate (including the thin portion 424a) except for where the thick portion is desired, and depositing, e.g., using chemical vapor deposition, the remaining oxide in the unmasked area to form the thick portion 424b. In other implementations, the step 902 can be formed by growing a thick oxide layer, masking the substrate (including the thick portion 424b) except where the thin portion is desired, etching the exposed portion of the oxide layer down to the silicon layer, and growing the thin oxide layer 424a in the region that was etched away, e.g., using the same mask that was used in the etching step. In either process, the mask can then be removed.

Referring to FIG. 10C, the gate conductor 102, e.g. a polysilicon layer, is applied over the oxide layer 424. The gate conductor, e.g. polysilicon layer, can be approximately 0.2-0.5μm thick depending on the base process technology node. The gate conductor 102 can also be deposited simultaneously on any CMOS devices on the substrate, e.g., using a single mask.

Referring to FIG. 10D, photoresist 104 is deposited, e.g., by spin coating, over the gate conductor 102, and patterned to expose at least the source side of the transistor. The photoresist can have a thickness of greater than 0.5μm. Optionally, some portions of the gate conductor 102 on the source side 120 can also be exposed.

Referring to FIG. 10E, the exposed portion of the gate conductor 102 on the source side 120 of the transistor is then removed by etching using the photoresist 104 as a mask, e.g., using dry plasma ecthing. The photoresist 104 can thus act as a mask during the etch.

Referring to FIG. 10F, the p-body 422 is implanted using the combined photoresist 104 and remaining gate conductor 102 as a mask. The p-body 422 is implanted by bombarding the surface of the oxide 424a with the implant atoms. The implant can be performed at an angle to the main surface of the oxide 424a (shown by arrow 108). Because both the gate conductor 102 and the photoresist 104 are used as a mask, the resulting p-body 422 can be self-aligned to the gate, particularly to the source side of the gate conductor.

Referring to FIG. 10G, the photoresist layer 104 is then stripped from the surface.

Referring to FIG. 10H, a new layer of photoresist 124 is applied, e.g., by spin coating, over the exposed surfaces, including the exposed portion of the oxide layer 424a on the source side 120 following the etch of the gate conductor 102 on the source side 120. The photoresist layer 104 is patterned to expose at least the drain side of the transistor. Optionally, some portions of the gate conductor 102 on the drain side 122 can be exposed.

Referring to FIG. 10I, the exposed portion of the gate conductor on the drain side 122 is then removed by etching, e.g., dry plasma etching, using the photoresist 124 as a mask. The photoresist 124 also serves to protect the implanted p-body on the source side 120 during the etching process.

Referring to FIG. 10J, the NDD 415 can be implanted using the combined photoresist 124 and remaining gate conductor 102 as a mask. Because both the gate conductor 102 and the photoresist 124 are used as a mask, the NDD 415 can be self-aligned to the gate, particularly to the drain side of the gate conductor.

Referring to FIG. 10K, the photoresist 124 is then removed.

The p+ and n+ regions 414, 418, 420, can be implanted by conventional implanting processes, e.g., after the P-body 422 and NDD 415 have been implanted.

Although the fabrication of only one gate is illustrated in FIGS. 10a-10g, multiple gates, or the gate of a distributed transistor, can be fabricated simultaneously.

By including a photoresist layer over the polygate during the p-body implantation, a self-aligned p-body can be formed. Moreover, using the photoresist protects the remainder of the substrate from impurities caused during the implantation process. Further, by having two separate etching steps, before and after the implantation process, a single self-aligned p-body can be formed in the source side of the substrate.

Particular embodiments have been described. Other embodiments are within the scope of the following claims.

What is claimed is:

CLAIMS

1. A transistor comprising:

a source region including a first impurity region implanted into a substrate;

a drain region including a second impurity region implanted into the substrate; and

a gate including an oxide layer formed over the substrate and a conductive material formed over the oxide layer, the oxide layer comprising a first side and a second side, the first side formed over a portion of the first impurity region and the second side formed over a portion of the second impurity region, the first side having a thickness such that a turn-on voltage of the transistor is substantially 0.4V;

wherein the transistor is configured as a power switch in a voltage regulator.

2. The transistor of claim 1, wherein the source further comprises a third impurity region, the third impurity region being self-aligning.

3. The transistor of claim 2, wherein a maximum doping concentration of the third impurity region is between about $1x10^{17}$ atoms/cm^2 and $1x10^{18}$ atoms/cm^2.

4. The transistor of claim 2, wherein a doping concentration of the third impurity region at a surface adjacent to the oxide layer is less than about $5x10^{17}$ atoms/cm^2.

5. The transistor of claim 4, wherein the doping concentration is less than about $3x10^{17}$ atoms/cm^2.

6. The transistor of claim 2, wherein the third impurity region is positioned in a current path of the transistor.

7. The transistor of claim 1, wherein the transistor is a lateral double-diffused metal oxide semiconductor (LDMOS).

8. A transistor comprising:

a source region including a first impurity region of a first impurity type implanted into a well region, also of the first impurity type, implanted on a substrate and a third impurity region of an opposite second impurity type abutting the first impurity region, and a fourth impurity region of the second impurity type surrounding the first impurity region and the third impurity region, the fourth impurity region having a lower doping concentration than the third impurity region;

a drain region including a second impurity region of the first impurity type implanted into the substrate;

an intrinsic diode between the fourth impurity region and the drain region, the intrinsic diode formed by the fourth impurity region of the second impurity type and the well region of the first impurity type; and

a gate including an oxide layer formed over the substrate and a conductive material formed over the oxide layer, the oxide layer comprising a first side and a second side, the first side formed over a portion of the first impurity region and the second side formed over a portion of the second impurity region, the first side having a thickness such that a turn-on voltage of the transistor is less than a turn-on voltage of the intrinsic diode.

9. The transistor of claim 8, wherein the turn-on voltage of the transistor is between 0.4 and 0.6V.

10. The transistor of claim 8, wherein the fourth impurity region is self-aligning.

11. The transistor of claim 8, wherein a maximum doping concentration of the fourth impurity region is between about $1x10^{17}$ atoms/cm^2 and $1x10^{18}$ atoms/cm^2.

12. The transistor of claim 8, wherein a doping concentration of the fourth impurity region at a surface adjacent to the oxide layer is less than about $5x10^{17}$ atoms/cm^2.

13. The transistor of claim 12, wherein the doping concentration is less than about $3x10^{17}$ atoms/cm^2.

14. The transistor of claim 10, wherein the fourth impurity region is positioned in a current path of the transistor.

15. The transistor of claim 8, wherein the transistor is a lateral double-diffused metal oxide semiconductor (LDMOS).

16. A system comprising:

an input terminal and an output terminal;

a high-side transistor between the input terminal and an intermediate terminal, having a source connected to the input terminal and a drain connected to the intermediate terminal;

an output filter between the intermediate terminal and the output terminal; and

a low-side transistor between ground and the intermediate terminal, having the source connected to ground and the drain connected to the intermediate terminal, comprising:

a source region including a first impurity region implanted into a substrate;

a drain region including a second impurity region implanted into the substrate; and

a gate including an oxide layer formed over the substrate and a conductive material formed over the oxide layer, the oxide layer comprising a first side and a second side, the first side formed over a portion of the first impurity region and the second side formed over a portion of the second impurity region, the first side having a thickness such that a turn-on voltage of the transistor is substantially 0.4V.

17. The system of claim 16, wherein the source region of the low-side transistor further comprises a third impurity region, the third impurity region being self-aligning.

18. The system of claim 17, wherein a maximum doping concentration of the third impurity region of the low-side transistor is between about $1x10^{17}$ atoms/cm^2 and $1x10^{18}$ atoms/cm^2.

19. The system of claim 17, wherein a doping concentration of the third impurity region of the low-side transistor at a surface adjacent to the oxide layer is less than about $5x10^{17}$ atoms/cm^2.

20. The system of claim 19, wherein the doping concentration is less than about $3x10^{17}$ atoms/cm^2.

21. The system of claim 17, wherein the third impurity region of the low-side transistor is positioned in a current path of the transistor.

22. The system of claim 16, wherein the low-side transistor is a lateral double-diffused metal oxide semiconductor (LDMOS).

23. A system comprising:

an input terminal and an output terminal;

a high-side transistor between the input terminal and an intermediate terminal, having a source connected to the input terminal and a drain connected to the intermediate terminal;

an output filter between the intermediate terminal and the output terminal; and

a low-side transistor between ground and the intermediate terminal, having the source connected to ground and the drain connected to the intermediate terminal, comprising:

a source region including a first impurity region of a first impurity type implanted into a well region, also of the first impurity type, implanted on a substrate, a third impurity region of an opposite second impurity type abutting the first impurity region, and a fourth impurity region surrounding the first impurity region and the third impurity region, the fourth impurity region having a lower doping concentration than the third impurity region;

a drain region including a second impurity region implanted into the substrate;

an intrinsic diode between the fourth impurity region and the drain region, the intrinsic diode formed by the fourth impurity region of the second impurity type and the well region of the first impurity type; and

a gate including an oxide layer formed over the substrate and a conductive material formed over the oxide layer, the oxide layer comprising a first side and a second

side, the first side formed over a portion of the first impurity region and the second side formed over a portion of the second impurity region, the first side having a thickness such that a turn-on voltage of the transistor is less than a turn-on voltage of the intrinsic diode.

24. The system of claim 23, wherein the turn-on voltage of the low-side transistor is between 0.4 and 0.6V.

25. The system of claim 23, wherein the fourth impurity region is self-aligning.

26. The system of claim 23, wherein a maximum doping concentration of the fourth impurity region of the low-side transistor is between about $1x10^{17}$ atoms/cm^2 and $1x10^{18}$ atoms/cm^2.

27. The system of claim 23, wherein a doping concentration of the fourth impurity region of the low-side transistor at a surface adjacent to the oxide layer is less than about $5x10^{17}$ atoms/cm^2.

28. The system of claim 27, wherein the doping concentration is less than about $3x10^{17}$ atoms/cm^2.

29. The system of claim 23, wherein the fourth impurity region of the low-side transistor is positioned in a current path of the transistor.

30. The system of claim 23, wherein the low-side transistor is a lateral double-diffused metal oxide semiconductor (LDMOS).