

REFRESH CONTROL CIRCUIT AND METHOD, AND MEMORY

ABSTRACT

Embodiments of the disclosure provide a refresh control circuit and method, and a memory. The circuit includes: an address output module configured to output a to-be-refreshed address signal including a block address signal and a row address signal; a block decoding module configured to: receive the block address signal; decode the block address signal and output a first block selection signal for selecting multiple data blocks from the memory array, in response to that the memory array is subjected to no row hammer attack, or decode the block address signal and output a second block selection signal for selecting one data block from the memory array, in response to that the memory array is subjected to a row hammer attack; and a row decoding module, configured to receive the row address signal, decode the row address signal and output a row selection signal.

[Fig. 2]