

PATENT SPECIFICATION

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DRAWINGS ATTACHED

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(54) IMPROVEMENTS IN OR RELATING TO SEMI-CONDUCTORS

(71) We, FAIRCHILD CAMERA AND INSTRUMENT CORPORATION, of 464 Ellis Street, Mountain View, California, 94040, United States of America, a corporation organised and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to MOS devices and in particular to MOS devices using appropriately doped semiconductor material as the gate electrode.

An MOS device, where the letters "MOS" stand for metal-oxide-semiconductor, is essentially a voltage-controlled resistor or "channel region" linking two electrically-separated, highly conductive source and drain regions of the first conductivity type diffused into an opposite conductivity type substrate of semiconductor material. The channel region is formed by applying a selection voltage to a metal gate electrode overlying but insulated from the substrate so as to invert the conductivity type of the underlying region of the substrate. By varying the voltage applied to the gate electrode after inversion, the number of mobile carriers (i.e. electrons or holes) in this channel region, and thus the conductivity of this channel, are varied.

MOS devices are commonly used as either capacitors or transistors. When used as a capacitor, charge stored in the gate electrode is matched by an equal charge of opposite polarity stored in the substrate beneath the gate electrode. When used as a transistor, the current flow between source and drain is controlled by controlling both the bias voltages applied to the source and drain, and the voltage applied to the gate electrode overlying the channel region.

There are two types of MOS transistors, an "enhancement mode" transistor, the channel region of which, though normally not conducting, inverts and increases in conductivity in response to an applied gate voltage, and, a "depletion mode" transistor, the channel region of which, though normally conducting, may increase or decrease its conductivity in response to an applied gate voltage.

An enhancement mode P channel MOS transistor contains N type semiconductor materials between P type source and drain regions. Application of a selected negative voltage to the gate electrode overlying but insulated from the channel region inverts the semiconductor material in the channel from N type to P type. Thus, the conductivity of this channel region changes from a low to a high value resulting in a controlled flow of current from the P type source region to the P type drain region.

In the P type depletion mode transistor, the channel region is normally conducting. Application of a positive voltage to the metal electrode overlying but insulated from the channel region deplete the positive mobile carriers from the channel region underlying the gate electrode with the result that this region becomes N type. P—N junctions will then isolate the source and drain regions resulting in very high resistance between these regions.

According to this invention, in a method of forming an MOS device with a doped semiconductor gate electrode comprising the steps of forming an insulation layer on a surface of a silicon substrate; forming a layer of silicon over at least selected portions of said insulating layer, removing selected exposed portions of said insulating layer

or of said insulating layer and said silicon layer to expose parts of silicon substrate; diffusing impurities at a concentration between 10^{17} and 10^{19} atoms/cc into the exposed parts of said silicon substrate to form diffused regions in said substrate on either side of and extending beneath said silicon layer; and diffusing impurities at a concentration between 10^{17} and 10^{19} atoms/cc into the silicon layer to render it conductive; the improvement which comprises; forming said silicon layer by thermally decomposing silane into silicon and hydrogen in a hydrogen atmosphere at a temperature between 630°C and 680°C .

According to another aspect of the invention, in an MOS device containing source and drain regions of one conductivity type in a silicon substrate of the opposite conductivity type and with a silicon gate electrode overlying but separated from the channel region between the source and drain regions by an insulating layer of silicon oxide, that improvement which comprises: the gate electrode being non-single crystal silicon formed on said silicon oxide from the decomposition of silane in a hydrogen atmosphere at a temperature between 630°C and 680°C , said gate electrode being doped with impurity atoms to a concentration between 10^{17} and 10^{19} atoms/cc.

In one embodiment of this invention the gate electrode of an MOS device is made of P-type amorphous silicon while the semiconductor material is monocrystalline N-type silicon containing P-type source and drain regions.

In another embodiment of this invention, the gate electrode is made of N-type amorphous silicon while the semiconductor material is N-type monocrystalline silicon containing P-type source and drain regions.

This invention will be more fully understood in light of the following detailed description taken together with the accompanying drawings.

Brief Description of the Drawings

FIGS. 1a, 1b and 1c shown the potential distribution in a silicon-silicon dioxide-silicon structure when the gate electrode voltage V_G is zero for two different silicon dioxide thicknesses between the silicon gate electrode and the underlying silicon substrate, and when the gate electrode voltage equals the work function difference ϕ_{ss} between the silicon gate and the silicon-semiconductor material;

FIGS. 2a through 2e show in cross-section stages of the construction of an MOS device using a silicon gate electrode selectively doped with P-type impurities;

FIGS. 3a through 3d give top views during various stages of construction of the MOS device shown in FIGS. 2a through 2e;

FIG. 4 plots the Fermi level E_F minus the intrinsic Fermi level E_i versus impurity concentration for both donor and acceptor impurities in the silicon gate;

FIGS. 5a to 5e illustrate one process for making MOS devices with a silicon gate electrode selectively doped with N-type impurities;

FIGS. 6a, 6b and 6c show, respectively, top and cross-sectional views of an MOS complementary inverter and the schematic diagram of this inverter;

FIGS. 6d through 6g showed related input and output signals from the inverter of FIGS. 6a, 6b and 6c.

Detailed Description of the Preferred Embodiments

FIGS. 1a, 1b and 1c show the potential distribution across an MOS device containing P-type amorphous silicon as the gate electrode. Hereafter, it should be understood that the silicon used as a gate electrode is amorphous silicon, even though not explicitly stated, unless of course, another type of silicon is explicitly required. The potential distribution through the P-type silicon is approximately uniform because the P-type silicon has been highly doped with acceptor impurities to a concentration of 10^{17} to 10^{18} atoms per cubic centimeter. Thus the resistivity of this silicon is quite low, typically being less than 0.3 ohm-centimeter. As a result of the use of P-type silicon for the gate electrode, electrons from the N-type silicon are repelled away from the interface of the silicon dioxide and the N-type silicon, as shown in FIG. 1a. This occurs because the Fermi level in all three materials must be uniform when the materials are in equilibrium. For this to occur, the energy bands in the N-type silicon must bend upward as one approaches the silicon-silicon dioxide interface from the silicon. When the intrinsic energy band E_i crosses the Fermi energy level E_F as shown in FIG. 1a, the region of this N-type silicon adjacent the silicon dioxide-silicon interface inverts to the P-type silicon. The thickness of the silicon dioxide in FIG. 1a is about 500 angstroms.

FIG. 1c shows the energy band configuration when the silicon dioxide is 700 to 800 angstroms thick. The intrinsic energy band E_i of the N-type single crystal silicon is just beneath the Fermi energy level E_F . In this situation the surface of the N-type

silicon, though close to inversion, has not inverted. When a negative voltage is applied to the P-type silicon gate, electrons are driven from the silicon-silicon dioxide interface and holes are attracted to this interface. As shown by the closeness of E_i to E_F at the silicon surface, only a small negative voltage is required to invert the region of silicon adjacent the silicon-silicon dioxide interface. As a result, the turn-on voltage of the P-channel MOS device is significantly decreased.

For a P-type silicon gate, the turn-on voltage V_{Ti} is -1.4 volts while the lead turn on voltage (linearly proportional to oxide thickness) is about -15.8 volts. Thus the ratio V_{TL}/V_{TQ} is greater than 11.

When a positive gate voltage is applied to the P-type silicon gate, as shown in FIG. 1b, electrons are attracted to this interface from the N-type silicon. As a result, the valence, conduction and intrinsic bands of the N-type silicon flatten out.

Because the work function of the P-type silicon gate can be varied about 0.2 eV as a function of impurity doping concentration without losing the high conductivity essential to an electrode, the gate voltage needed to invert the surface region of the N-type silicon can be varied a like amount by varying the doping of the silicon gate. This variation of silicon work function with doping, expressed as a shift in Fermi energy level E_F relative to the intrinsic Fermi level E_i for both P and N-type impurities, is shown in FIG. 4. The ordinate of FIG. 4 is $E_F - E_i$, in electron volts. The abscissa is the silicon impurity concentration, in atoms per cubic centimeter, on a logarithmic scale. These curves are calculated from the equation

$$E_F - E_i = kT \ln \frac{[N_D - N_A + \sqrt{(N_D - N_A)^2 + 4n_i^2}]}{2n_i} \quad (1)$$

when donor impurity predominates, or from

$$E_i - E_F = kT \ln \frac{[N_A - N_D + \sqrt{(N_A - N_D)^2 + 4n_i^2}]}{2n_i} \quad (2)$$

when acceptor impurity predominates. In these equations, E_F and E_i have been previously defined, k is Boltzmann's constant, T is temperature in degrees Kelvin, N_D and N_A are the silicon donor and acceptor impurity concentrations in atoms per cubic centimeter, respectively and n_i is the intrinsic carrier concentration of the silicon, also in atoms per cubic centimeter.

When the impurity concentration, either donor or acceptor, is less than 10^{16} atoms per cubic centimeter, the silicon crystal behaves much like intrinsic silicon and the Fermi level E_F of the silicon is approximately the intrinsic Fermi level E_i of the silicon.

As the impurity concentration increases, the Fermi level E_F deviates logarithmically from the intrinsic Fermi level E_i . For donor impurities, the Fermi level rises relative to the intrinsic Fermi level; for acceptor impurities, the Fermi level falls relative to the intrinsic Fermi level. A maximum shift in Fermi level of about ± 0.55 electron volts from the intrinsic energy level occurs as the doping concentration approaches 10^{19} atoms per cubic centimeter. Above this doping, the silicon becomes degenerate and the equations used to calculate FIG. 4 are no longer valid.

Only an acceptor or donor impurity concentration greater than about 10^{17} atoms per cubic centimeter gives silicon a high enough conductivity to allow silicon to be used as a gate electrode in an MOS device. In varying the impurity concentration in the silicon from 10^{17} to about 10^{19} atoms per cubic centimeter, $E_F - E_i$ varies from about 0.35 eV to about 0.55 eV for N-type impurities and from about -0.35 eV to about -0.55 eV for P-type impurities. The resistivities associated with this range of impurity concentrations vary from about 0.3 ohm-centimeters to about 0.01 ohm-centimeters. Interestingly, the silicon resistivities associated with N-type impurities are about half or less than the silicon resistivities associated with P-type impurities.

As discussed by Grove in Chapter 9 of his book, the turn-on voltage V_T of an MOS device is a function of the surface state charge Q_{ss} in the silicon dioxide at the interface between the silicon dioxide and the underlying silicon substrate, the total charge Q_B in the depletion region at the onset of strong inversion, the capacitance C_o of the insulation between the gate electrode and the substrate, the work function difference Φ_{MS} , or Φ_{SS} for a silicon gate electrode, between the metal or semiconductor

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gate electrode and the underlying silicon substrate, and the semiconductor surface potential $2\phi_F$ at the onset of strong inversion, where $\phi_F = E_F - E_i$. Thus

$$V_T = -\frac{Q_{ss}}{C_o} + \phi_{Ms} + 2\phi_F - \frac{Q_B}{C_o} \quad (3)$$

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C_o is the nominal capacitance per unit area of the silicon dioxide layer and is inversely proportional to the silicon dioxide thickness. In a P-type substrate doped to an impurity concentration of about 10^{15} atoms per cubic centimeter, the effects of Q_B and Q_{ss} on V_T cancel; in an N-type substrate with the same impurity concentration these effects add.

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The causes of surface state charge Q_{ss} are not at this time fully understood. However, the parameters of silicon-silicon dioxide processing which affect Q_{ss} are discussed by Deal, Sklar, Snow and Grove in a paper entitled "Characteristics of the Surface State Charge (Q_{ss}) of Thermally Oxidized Silicon" published in March 1967 on pages 266 to 274 of the Journal of the Electrochemical Society. The charge Q_B , on the other hand, is a function of substrate doping. For N channel enhancement mode devices a Q_B of 4 or 5×10^{11} electron charges per cubic centimeter is typical; for P channel devices a Q_B of 0.8 to 2.5×10^{11} electron charges per cubic centimeter is likely.

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Table I shows the relationship of turn-on voltage V_T to work-function difference ϕ_{ss} between a doped amorphous silicon gate and an underlying monocrystalline silicon substrate for a 1000 angstrom silicon dioxide insulation separating the silicon gate and substrate. The turn-on voltage V_T is given for two monocrystalline silicon substrate orientations, the (111) and the (100) orientations.

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TABLE I

Silicon Substrate		Silicon Gate		ϕ_{ss}	V_{T*}	
Impurity type	Impurity concentration	Impurity type	Impurity concentration		Substrate (111) orientation	Substrate (100) orientation
P	10^{15}	P	10^{14}	+0.25	+0.05	+0.85
P	10^{15}	N	10^{19}	-0.85	-1.05	-0.25
N	10^{15}	P	10^{19}	+0.85	-1.35	-0.55
N	10^{15}	N	10^{19}	-0.25	-2.45	-1.65

* $Q_{ss} = 3 \times 10^{11}$ atoms/cc for (111) and 10^{11} atoms/cc for (100)

$Q_B = 10^{11}$ atoms/cc for both (111) and (100)

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FIGS. 2a through 2e and 3a through 3d show one method by which the semiconductor device of this invention is produced. A substrate 11 of N-type monocrystalline silicon, cut in the (111) plane and with a resistivity somewhere between 5 and 8 ohm-centimeters, has grown on it a layer 12 of silicon dioxide. Layer 12 typically is thermally grown to a thickness of one micron in region a and to a thickness of 0.1 micron in region b. Hereafter silicon 11, together with any overlying layers of metal and/or insulation, will be called wafer 10. FIG. 3a shows a top view of wafer 10 with the silicon dioxide layer 12 deposited thereon. The portion of wafer 10 from which the cross sectional view A-A shown in FIG. 2a is derived is clearly marked in FIG. 3a.

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Next, as shown in FIG. 2b, a layer 13 of amorphous silicon is grown over selected portions of layer 12 of silicon dioxide. Silicon layer 13 is grown to a thickness of 0.5 microns by thermally decomposing silane into silicon and hydrogen in a hydrogen atmosphere held between 630°C and 680°C.

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Extreme care is taken in cleaning the surface of silicon dioxide layer 12 before growing amorphous silicon 13 because foreign particles on this surface cause nucleation centers and whisker patterns to appear in the amorphous silicon. To clean the surface of layer 12, wafer 10 is dipped for 10 seconds into a 10 to 1 hydrofluoric rinse at room temperature. Then wafer 10 is subjected for over 5 minutes to a de-ionized water spray rinse. While 5 minutes are adequate to clean the surface of layer 12, 15 minutes are typically used to provide a margin of safety. Water is next removed from the surface of silicon dioxide layer 12 by exposing wafer 10 to isopropyl alcohol vapors. These vapors dry the surface of layer 12 without leaving residual moisture on this surface. Growth of silicon layer 13 then follows immediately after this drying step. Alternatively, wafer 10 is pulled directly out of the oxidation furnace and placed immediately in the silicon deposition reactor for the growth of silicon layer 13.

It should be noted that silicon layer 13 is *grown* on silicon dioxide layer 12 rather than evaporated on this layer. Evaporated silicon has been found to be unsatisfactory for layer 13 because evaporated silicon breaks as it is deposited. Although the nature of these breaks is not understood completely, subsequent etching and diffusing steps enlarge these cracks and cause open circuits in the evaporated silicon, thus rendering devices incorporating this silicon inoperative.

Next, the grown silicon 13 and the exposed surfaces of silicon dioxide layer 12 are masked and selected portions of the silicon and silicon dioxide are etched away to expose portions 14 and 41 (FIG. 3b) of the underlying silicon substrate 11.

Wafer 10 is next placed in a diffusion furnace and P type impurities, typically boron, are diffused into portion 14 and 41 (FIG. 3b) of silicon 11 to a concentration of about 10^{17} to 10^{19} atoms per cubic centimeter. These P type impurities likewise diffuse into the deposited silicon 13. This last diffusion is essential to obtain the highly conductive silicon gate electrode of this invention. FIG. 3b shows a top view of wafer 10 after this diffusion.

Next, a layer 15 of silicon dioxide is deposited over exposed silicon dioxide layer 12, P+ regions 14 and 41 and silicon layer 13. Layer 15 typically is 0.6 to 0.8 microns thick. Windows 16, 42 and 17 are etched through this deposited silicon dioxide layer 15 to expose portions of P-type regions 14 and 41 as well as a portion of silicon 13. FIG. 3c shows the top view of wafer 10 from which the cross-sectional view "C-C" shown in FIG. 2c is obtained.

After windows 16, 42 and 17 have been etched in layer 15, wafer 10 is masked and aluminum contact 18, shown in FIG. 2d, is evaporated onto the wafer so as to make contact with the exposed portion of P+ region 14. In addition, aluminum contact 48, shown in FIG. 3d, is evaporated through window 42 over a corresponding P+ region 41 (shown in FIGS. 3b and 3d) to make similar contact with a portion of region 41. And as shown in FIG. 3d, aluminum 49 is selectively evaporated over silicon dioxide 15 to contact the underlying silicon gate electrode 13 through window 17 cut in layer 15. FIG. 2e shows in cross-section this aluminum layer 49 contacting silicon electrode 13. A typical thickness for aluminum layers 18, 48 and 49 is one to one and a half micron.

As shown in FIG. 3d, the resulting structure consists of an MOS device with P+ source and drain regions 14 and 41 and with a silicon gate electrode 13 connected by aluminum layer 49 to a gate voltage source. Because silicon gate electrode 13 is grown prior to the diffusion of the source and drain regions, gate 13 is automatically correctly aligned between the source and drain. And, because of the symmetry of the MOS device, regions 14 and 41 can be used interchangeably as sources or drains, depending on the bias voltage applied thereto. Upon application to the silicon gate electrode of a negative gate voltage slightly larger in an absolute sense than the turn-on voltage (-1.35 volts) of the device, a channel region beneath the gate electrode is depleted of N-type carriers and thereby inverted to P-type material with the result that the region becomes highly conductive. Current then flows from the source to the drain.

FIGS. 5a through 5e show one method of constructing an alternative embodiment of this invention using a silicon gate electrode doped with N-type impurities.

In FIG. 5a, N-type silicon 101 has thermally grown on it silicon dioxide layer 102. Layer 102 is typically 1 micron thick in region *a* and 0.1 micron thick in region *b*. Silicon 101 is of the single crystal type cut in the (111) plane. Single crystal silicon 101 can, if desired, be cut in the (100) orientation. Hereafter, silicon 101, together with any overlying layers of metal and/or insulation, will be called wafer 100.

Next, as shown in FIG. 5b, layer 103 of amorphous silicon is grown over silicon dioxide layer 102 to a thickness of about 0.5 microns. Silicon layer 103 is grown by thermally decomposing silane into silicon and hydrogen in a hydrogen atmosphere

held between 630°C and 680°C. N-type impurities are then diffused into silicon layer 103 to a concentration of about 10^{19} atoms per cubic centimeter. There follows, as shown in FIG. 7c, a layer 104 of silicon dioxide deposited over silicon 103.

Most of silicon dioxide layer 104 and the underlying silicon 103 are then etched away to leave region 110 consisting of a layer of silicon 103 overlayed by a layer of silicon dioxide 104 (FIG. 5d). Windows 109 are etched through silicon dioxide layer 102 to expose regions of the underlying single crystal silicon 101. P-type dopants are then diffused through these windows to form P-type source and drain regions 111 and 112 in the underlying N type silicon substrate. Silicon dioxide 104 prevents these P-type dopants from changing the conductivity type of silicon gate 103 from N to P-type.

Next, a thin layer of silicon dioxide 113 is grown over the surface of wafer 100. Windows are then etched through layer 113 to expose surface areas of regions 111, 112 and silicon gate electrode 103. Aluminum electrodes 105, 106 and 107 are finally deposited on the exposed surface areas to provide electrical contact to the source and drain regions of the MOS device and the gate electrode 103.

FIG. 6a shows an integrated circuit containing MOS devices using the doped silicon gate electrodes of this invention. Shown in FIG. 6a is the schematic top view of a basic complementary MOS inverter. This inverter contains in its semiconductor substrate both N-type silicon 215 and P-type silicon 212. This substrate is preferably cut in the (100) orientation to minimize Q_{ss} . Region 215 has an impurity concentration of about 10^{15} atoms per cubic centimeter. Region 212 is formed within region 215 by diffusing P-type impurities into the N-type substrate to a concentration of about 10^{16} acceptor atoms per cubic centimeter. N-type source and drain regions 210 and 211 are diffused into P-type region 212 to a concentration of about 10^{19} atoms per cubic centimeter. Silicon gate electrode 217 contains N-type impurities likewise diffused to a concentration of about 10^{19} atoms per cubic centimeter. Electrode 217 is separated from the underlying P-type silicon substrate by a layer of insulation 224 shown in FIG. 6b.

Contained within the N-type silicon 215 are source and drain regions 219 and 220. Regions 219 and 220 consist of P-type impurities diffused into N-type silicon substrate 215 to a concentration of about 10^{19} atoms per cubic centimeter. Overlying the channel region between regions 219 and 220 and separated therefrom by insulation 224 is silicon gate electrode 218. Electrode 218, contrary to electrode 217, is doped with P-type impurities to a concentration of about 10^{19} atoms per cubic centimeter. Attached to P-type source and drain regions 219 and 220 through windows 221 and 222 are aluminum electrodes 202 and 203 respectively. Attached to N-type source and drain regions 210 and 211 through windows 213 and 214, are aluminum electrodes 205 and 203, respectively. Thus, region 211 is at the same potential as region 220. P-type silicon substrate 212 is biased to a selected potential by means of aluminum conductor 204 which contacts substrate 212 through window 223 in silicon dioxide layer 224. Aluminum contact 201 is attached to silicon gate electrodes 217 and 218. Line 216 marks the NP junction between gate electrodes 217 and 218.

FIG. 6c shows the circuit schematic of the integrated circuit shown in FIG. 6a. For use as an inverter, lead 201 serves as the input lead to the device while lead 203 serves as the output lead from the device. The PN junction between P type region 212 and N type region 215 in the silicon substrate is back biased by applying a negative supply voltage through lead 204 to P type region 212. Lead 225, shown in FIG. 6b attached to the bottom of N type region 215, is grounded. Lead 202 to P type region 219 is also electrically grounded. And lead 205 to N type region 210 (FIG. 6a) is electrically attached to the negative supply voltage.

When an input signal, such as the square wave shown in FIG. 6d, is applied to lead 201, the output signal on lead 203 has the same shape as this input signal, but is inverted in polarity. The two MOS devices shown in FIG. 6c are enhancement mode devices; that is, the channel regions between the source and drain regions of the two devices are normally non-conducting. But when a positive voltage, such as square wave shown in FIG. 6d, is applied to lead 201, the output signal taken from lead 203 resembles the input signal in shape but is of opposite polarity. This occurs because when a positive voltage is supplied to input lead 201, a region just beneath, and including, the surface of region 212 inverts and creates a channel region in which minority carriers predominate between source and drain 211 and 210. The conductivity of this N type channel is much greater than the conductivity of the P type silicon. As a result, output lead 203 quickly drops almost to the potential of the negative supply voltage. This drop, which generates the output signal, is shown in

FIG. 6e. On the other hand, when the input voltage on lead 201 becomes negative, this voltage has no effect on the depletion channel between source and drain regions 211 and 210 but rather depletes the electrons from the channel region between source and drain 219 and 220. Source 219 is grounded. Upon depletion of these electrons from the channel region, the channel region inverts and becomes P type, with a conductivity several orders of magnitude higher than possessed by the same channel region with N type impurities. As a result, the output voltage on lead 203 rises to ground potential. The circuit is thus an inverter.

While this invention has been described with an underlying substrate consisting of single crystal silicon cut in either the (111) or (100) orientation, other single crystal silicon substrates cut in other orientations can also be used in this invention. Finally, while an inverter using MOS devices containing silicon gate electrodes doped with both P types and N type impurities has been described, other more complicated integrated circuits, using similar gate electrodes, can be built.

WHAT WE CLAIM IS:—

1. In a method of forming an MOS device with a doped semiconductor gate electrode comprising the steps of forming an insulation layer on a surface of a silicon substrate; forming a layer of silicon over at least selected portions of said insulating layer; removing selected exposed portions of said insulating layer or of said insulating layer and said silicon layer to expose parts of said silicon substrate; diffusing impurities at a concentration between 10^{17} and 10^{19} atoms/cc into the exposed parts of said silicon substrate to form diffused regions in said substrate on either side of and extending beneath said silicon layer; and diffusing impurities of a concentration between 10^{17} and 10^{19} atoms/cc into the silicon layer to render it conductive; the improvement which comprises; forming said silicon layer by thermally decomposing silane into silicon and hydrogen in a hydrogen atmosphere at a temperature between 630°C and 680°C .

2. The method of claim 1 wherein said insulating layer between said silicon layer and said underlying silicon substrate comprises a single layer of silicon dioxide.

3. In an MOS device containing source and drain regions of one conductivity type in a silicon substrate of the opposite conductivity type and with a silicon gate electrode overlying but separated from the channel region between the source and drain regions by an insulating layer of silicon oxide, that improvement which comprises; the gate electrode being non-single crystal silicon formed on said silicon oxide from the decomposition of silane in a hydrogen atmosphere at a temperature between 630°C and 680°C , said gate electrode being doped with impurity atoms to a concentration between 10^{17} and 10^{19} atoms/cc.

4. Methods of forming an MOS device substantially as described.

5. The improvement in an MOS device as claimed in claim 3 substantially as described with reference to Figs. 2d, 2e, and 3d or Fig. 5e.

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Reference has been directed in pursuance of section 9, subsection (1) of the Patents Act, 1949, to patent No. 1,186,625.

FIG. 6e. On the other hand, when the input voltage on lead 201 becomes negative, this voltage has no effect on the depletion channel between source and drain regions 211 and 210 but rather depletes the electrons from the channel region between source and drain 219 and 220. Source 219 is grounded. Upon depletion of these electrons from the channel region, the channel region inverts and becomes P type, with a conductivity several orders of magnitude higher than possessed by the same channel region with N type impurities. As a result, the output voltage on lead 203 rises to ground potential. The circuit is thus an inverter.

While this invention has been described with an underlying substrate consisting of single crystal silicon cut in either the (111) or (100) orientation, other single crystal silicon substrates cut in other orientations can also be used in this invention. Finally, while an inverter using MOS devices containing silicon gate electrodes doped with both P types and N type impurities has been described, other more complicated integrated circuits, using similar gate electrodes, can be built.

WHAT WE CLAIM IS:—

1. In a method of forming an MOS device with a doped semiconductor gate electrode comprising the steps of forming an insulation layer on a surface of a silicon substrate; forming a layer of silicon over at least selected portions of said insulating layer; removing selected exposed portions of said insulating layer or of said insulating layer and said silicon layer to expose parts of said silicon substrate; diffusing impurities at a concentration between 10^{17} and 10^{19} atoms/cc into the exposed parts of said silicon substrate to form diffused regions in said substrate on either side of and extending beneath said silicon layer; and diffusing impurities of a concentration between 10^{17} and 10^{19} atoms/cc into the silicon layer to render it conductive; the improvement which comprises; forming said silicon layer by thermally decomposing silane into silicon and hydrogen in a hydrogen atmosphere at a temperature between 630°C and 680°C .

2. The method of claim 1 wherein said insulating layer between said silicon layer and said underlying silicon substrate comprises a single layer of silicon dioxide.

3. In an MOS device containing source and drain regions of one conductivity type in a silicon substrate of the opposite conductivity type and with a silicon gate electrode overlying but separated from the channel region between the source and drain regions by an insulating layer of silicon oxide, that improvement which comprises; the gate electrode being non-single crystal silicon formed on said silicon oxide from the decomposition of silane in a hydrogen atmosphere at a temperature between 630°C and 680°C , said gate electrode being doped with impurity atoms to a concentration between 10^{17} and 10^{19} atoms/cc.

4. Methods of forming an MOS device substantially as described.

5. The improvement in an MOS device as claimed in claim 3 substantially as described with reference to Figs. 2d, 2e, and 3d or Fig. 5e.

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