

deposited  $Ta_2O_5$  treated under different annealing conditions is effectively unavailable at this stage and is still under investigation.

### SUMMARY OF THE INVENTION

5           It is therefore the primary object of the present invention to provide a process for fabricating capacitor dielectrics of semiconductor memory devices having low leakage current characteristics.

          It is another object of the present invention to provide a process for fabricating in low pressure environment the capacitor dielectrics of semiconductor  
10       memory devices having low leakage current characteristics.

          It is yet another object of the present invention to provide a process for fabricating at low cost in a manner suitable for mass production the capacitor dielectrics of semiconductor memory devices having low leakage current characteristics.

15           To achieve the above-identified objects, the present invention provides a process for fabricating  $Ta_2O_5$  films for capacitor dielectrics of semiconductor memory devices such as stacked DRAM having low leakage current characteristics. The process comprises the steps of first preparing a semiconductor silicon substrate carrying an  $NH_3$ -nitrided polysilicon electrode layer. A  $Ta_2O_5$  film is  
20       then deposited over the surface of the electrode layer. The deposited  $Ta_2O_5$  film is then annealed in a furnace in  $N_2O$  gas at a temperature of about 800 °C for about 30 minutes. The novel post-deposition annealing procedure yields  $Ta_2O_5$  film for semiconductor memory device capacitor dielectrics having low leakage current, good reliability, and is particularly suitable for batch processing in conventional  
25       oxidation furnaces.

### BRIEF DESCRIPTION OF THE DRAWING

          Other objects and features of the present invention are described with reference to the preferred embodiments exemplified below with the accompanying  
30       drawing in which

FIGS. 1a and 1b schematically show cross-sectional views of the storage dielectrics of the memory device together with the electrode thereof being fabricated in accordance with a preferred embodiment of the present invention as depicted from the selected process stages respectively;

5           FIG. 2 shows the leakage current characteristics of Ta<sub>2</sub>O<sub>5</sub> films on n<sup>+</sup> polysilicon as a function of effective electric field before and after various post-deposition annealing treatments; and

          FIG. 3 shows the critical field distribution characteristics of Ta<sub>2</sub>O<sub>5</sub> films after various post-deposition annealing treatments; and

10          FIG. 4 shows a prediction of lifetime expectancy in terms of reliability for the device fabricated in accordance with the preferred embodiment of the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

15           To provide for fabricating capacitor dielectrics of semiconductor memory devices having low leakage current characteristics, the process of the present invention is exemplified in a preferred embodiment as described in the following paragraphs. Note that the dimensions in the FIGS. 1a and 1b are not drawn to the exact scale as they only schematically depict the cross-sectional views  
20           of the device being fabricated.

##### Step 1

          Prepare a semiconductor silicon substrate carrying an electrode layer as the basis for the fabrication of a high-density memory device utilizing the Ta<sub>2</sub>O<sub>5</sub> film as its memory cell capacitor dielectric layer.

25           As is seen in FIG. 1a, the substrate 10 may, for example, be an n<sup>+</sup> type silicon (Si) substrate, or an n<sup>+</sup> polysilicon (poly-Si) substrate carrying an electrode layer 11 made of NH<sub>3</sub>-nitrided polycrystalline silicon (poly-Si).

##### Step 2

          Deposit a Ta<sub>2</sub>O<sub>5</sub> film over the semiconductor silicon substrate.

In FIG. 1b, the Ta<sub>2</sub>O<sub>5</sub> film 12 may be seen deposited in, for example, a low-pressure chemical vapor deposition (LPCVD) reactor. The Ta<sub>2</sub>O<sub>5</sub> film 12 may be deposited to have a thickness of about 8-16 nm.

### Step 3

5           Subject the deposited Ta<sub>2</sub>O<sub>5</sub> film to a furnace N<sub>2</sub>O annealing procedure.

The thermal annealing procedure of the deposited Ta<sub>2</sub>O<sub>5</sub> film 12 may be conducted in an N<sub>2</sub>O atmosphere, for example, at about 800 °C for about 30 minutes. The annealing processing in N<sub>2</sub>O may be conducted in conventional  
10   oxidation furnaces. This means that the thermal annealing procedure may be conducted in batch order, allowing the processing of a multiple number of wafers simultaneously. This is particularly advantageous for commercial mass production.

The above-described procedural steps essentially comprise the process of the present invention for the making of the low leakage current LPCVD Ta<sub>2</sub>O<sub>5</sub>  
15   capacitor storage dielectrics in high-density semiconductor memory devices such as stacked DRAM. It should be noted that, as persons skilled in the art should all well appreciate, a complete fabrication process for making semiconductor memory devices such as DRAM would include pre- and post-procedural steps in addition to those described in the above exemplified embodiment.

20           In order to demonstrate the effects of post-deposition annealing as outlined in the above step 3 using N<sub>2</sub>O on the electrical characteristics of LPCVD Ta<sub>2</sub>O<sub>5</sub> storage dielectrics on NH<sub>3</sub>-nitrided polysilicon electrodes for stacked DRAM, samples of LPCVD Ta<sub>2</sub>O<sub>5</sub> capacitor storage dielectrics undertaking three other different post-deposition annealing conditions are investigated. These  
25   include (a) rapid thermal O<sub>2</sub> annealing (RTO<sub>2</sub>), (b) conventional furnace O<sub>2</sub> annealing (FO<sub>2</sub>), and (c) rapid thermal N<sub>2</sub>O annealing (RTN<sub>2</sub>O). Results indicate that Ta<sub>2</sub>O<sub>5</sub> films with furnace N<sub>2</sub>O annealing of the present invention have the lowest leakage current, the best dielectric breakdown field distribution, and the best reliability.

30           FIG. 2 shows the leakage current characteristics of Ta<sub>2</sub>O<sub>5</sub> films on n<sup>+</sup> poly Si as a function of effective electric field before and after various post-

deposition annealing treatments. These post-deposition annealing treatments have their respective conditions as listed below.

- 5
- (a) RTO<sub>2</sub> at 800 °C for 60 seconds.
  - (b) Furnace O<sub>2</sub> at 800 °C for 30 minutes.
  - (c) RTN<sub>2</sub>O at 800 °C for 60 seconds.
  - (d) Furnace N<sub>2</sub>O at 800 °C for 30 minutes.

10 It is clearly shown in FIG. 2 that the furnace N<sub>2</sub>O annealing procedure of the present invention conducted at 800 °C for 30 minutes produces the lowest leakage current. A plausible mechanism for this leakage reduction by furnace N<sub>2</sub>O annealing can be attributed to the reactive atomic oxygen species (O<sup>+</sup>) generated by the dissociation of N<sub>2</sub>O gas at elevated temperature, and the furnace annealing allows sufficient time to reduce film defects. The reactive atomic oxygen species  
15 generated may contribute to fill the oxygen vacancies that result during the CVD Ta<sub>2</sub>O<sub>5</sub> deposition procedure as well as reducing the carbon and hydrogen content in the film. This is the reason why furnace N<sub>2</sub>O annealing produces a lower leakage than the rapid thermal N<sub>2</sub>O annealing. Moreover, this furnace annealing procedure may be conducted in conventional oxidation furnaces that, as mentioned  
20 above, are perfectly suitable for mass production. In other words, a batch of wafers typically more than 50 can be processed each batch.

FIG. 3 shows that Furnace N<sub>2</sub>O annealing procedure of the present invention possesses a tighter and higher critical field distribution as compared to three other methods of annealing. The critical field was measured at a current  
25 density of 1 μA/cm<sup>2</sup> with top electrode biased at positive voltage.

FIG. 4 shows a prediction of device life expectancy. When the inventive process of the present invention is compared to the prior art, better device lifetime expectancy can be anticipated. As is seen in the drawing, during the analyzed 10 year lifetime period, the device as fabricated in accordance with  
30 the process of the present invention exhibits higher reliability with its capability to sustain a higher effective electric field.

The examination to the LPCVD Ta<sub>2</sub>O<sub>5</sub> capacitor dielectrics samples which have undergone the above-described various post-deposition annealing procedures demonstrates that the furnace N<sub>2</sub>O annealing procedure of the present invention yields the lowest leakage current and best reliability characteristics.

- 5 Even better is the fact that, as mentioned above, the furnace N<sub>2</sub>O annealing procedure can be performed in conventional oxidation furnaces by a batch processing. This is particularly advantageous for the mass production requirements where the cost can be reduced and the overall efficiency increased.

- 10 While the present invention has been described by way of example and in terms of preferred embodiments, it is to be understood that the invention need not be limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structures.



WHAT IS CLAIMED IS:

1. A process for fabricating Ta<sub>2</sub>O<sub>5</sub> films for capacitor dielectrics of semiconductor memory devices having low leakage current characteristics, said  
5 process comprising the steps of:  
preparing a semiconductor silicon substrate carrying an electrode layer;  
depositing a Ta<sub>2</sub>O<sub>5</sub> film over said electrode layer; and  
furnace annealing said deposited Ta<sub>2</sub>O<sub>5</sub> film in N<sub>2</sub>O gas.
- 10 2. The process of claim 1, wherein said Ta<sub>2</sub>O<sub>5</sub> film is annealed at a temperature of about 800 °C.
3. The process of claim 2, wherein said Ta<sub>2</sub>O<sub>5</sub> film is annealed for about 30 minutes.
- 15 4. The process of claim 3, wherein said semiconductor silicon substrate is an n<sup>+</sup> type silicon substrate, or an n<sup>+</sup> type polysilicon substrate.
5. The process of claim 4, wherein said layer of electrode is formed  
20 of NH<sub>3</sub>-nitrided polycrystalline silicon.
6. The process of claim 5, wherein said Ta<sub>2</sub>O<sub>5</sub> film has a thickness of about 8-16 nm.
- 25 7. The process of claim 6, wherein said Ta<sub>2</sub>O<sub>5</sub> film is deposited in a low-pressure chemical vapor deposition (LPCVD) reactor.
8. The process of claim 7, wherein said Ta<sub>2</sub>O<sub>5</sub> film is annealed in an oxidation furnace.



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9. The process of claim 7, wherein said  $\text{Ta}_2\text{O}_5$  film is annealed in an oxidation furnace in a batch manner simultaneously with other  $\text{Ta}_2\text{O}_5$  films contained in different wafers.

- 5                   10. A process for fabricating  $\text{Ta}_2\text{O}_5$  films for capacitor dielectrics of semiconductor memory devices having low leakage current characteristics, said process comprising the steps of:
- preparing a semiconductor silicon substrate carrying an electrode layer;
- depositing a  $\text{Ta}_2\text{O}_5$  film over said electrode layer; and
- 10                   furnace annealing said deposited  $\text{Ta}_2\text{O}_5$  film in  $\text{N}_2\text{O}$  gas at a temperature of about 800 °C for about 30 minutes.