SPECIFICATION

A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND A METHOD OF MANUFACTURING THE SAME

Technical Field

The present invention relates to a semiconductor integrated circuit device and a technique for manufacturing the same, and particularly to a device isolation structure for forming fine or micro MISFETs (Metal Insulator Semiconductor Field Effect Transistors) and a technique effective for application to a forming process thereof.

Technical Background

With scale-down and high integration of semiconductor chips or elements, the introduction of a shallow groove isolation (SGI) of such a type that an insulating film is embedded inside each groove defined in a silicon substrate, is proceeding as a device isolation structure as an alternative to a local oxidization of silicon (LOCOS) method.

The above-described shallow groove isolation is considered to be advantageous to ensuring of sub-threshold characteristics and reductions in junction leakage and a backgate effect as compared with the LOCOS method because (a) a device isolation interval or space can be reduced, (b) it is easy to control a film thickness for device isolation and set a field reverse

voltage, and (c) since an inversion preventive layer can be separated from a diffused layer and a channel region by separately implanting an impurity in side walls of the inside of each groove and the bottom thereof.

A common method for forming the shallow groove isolation is as follows: First of all, a silicon substrate is subjected to thermal oxidation and a thin silicon oxide film is formed on the surface thereof. Thereafter, a silicon nitride film is deposited thereabove by a CVD (Chemical Vapor Deposition) method. Next, each silicon nitride film lying in a device isolation region is removed by dry etching with a photoresist film as a mask. Thereafter, trenches or grooves are defined in the substrate by dry etching with the silicon nitride films left in each active region as masks.

Next, a thick silicon oxide film is deposited on the substrate including the interiors of the grooves by the CVD method. Thereafter, the substrate is subjected to a thermal process and the silicon oxide films embedded inside the grooves are elaborately densified. Thereafter, the silicon oxide films above the silicon nitride films are removed by a polishing process such as etchback or chemical mechanical polishing (CMP) or the like, and the unnecessary silicon nitride films are then removed, whereby shallow groove isolations are completed. Shallow groove isolations are set out, for example, in Japanese

Laid-Open Patent Application No. Hei 02-260660, No. Hei 04-303942, No. Hei 08-97277 etc.

SUMMARY OF THE INVENTION

The present inventors have found out that thinning (local thinning) that a gate oxide film formed on the surface of the substrate corresponding to each active region would locally be thinned at a peripheral portion of the active region, and a phenomenon (called MOS-IV kink characteristic) that a drain current would flow by a low gate voltage, have been developed in the above-described device isolation structure. As a measure for solving it, the present inventors have discussed a technique for rounding the peripheral portion of the active region (effecting round processing on it).

As a result, the present inventors have found out that the (round processing) technique for rounding the peripheral portion of each active region after the grooves are defined in the substrate, has a problem in that since it needs a high-temperature thermal oxidizing process, a thermal oxide film formed on an inner wall of each groove due to a thermal oxidizing process at the round processing would grow to the active region side, thereby reducing the size of the active region, and hence this would be a hindrance to high integration and scale-down of each MISFET.

Namely, a problem arises in that when the round

processing (round) is insufficient, thinning (local thinning) that a gate oxide film is thinly formed at a peripheral portion of each pointed active region upon oxidation for forming the gate oxide film, and a variation in the threshold voltage of each MISFET due to a MOS-IV kink characteristic. It is necessary to sufficiently effect round processing (round) as its measure. However, when the sufficient round is applied to the peripheral portion of the active region, the active region (particularly, the direction of a gate width of each MISFET) becomes narrow. Therefore, the size (particularly, the gate width of the MISFET) of the active region cannot be ensured and semiconductor elements cannot be scaled down. In addition, this would be a hindrance to the fact that the width of each shallow groove isolation is miniaturized and the semiconductor elements are scaled down so as to be brought into high integration.

An object of the present invention is to provide a technique capable of pressing ahead with the scale-down of MISFETs.

Another object of the present invention is to provide a technique capable of promoting the scale-down of the width of each shallow groove isolation.

The above and other objects and novel features of the present invention will become apparent from the description of the present specification and the

accompanying drawings.

Summaries of typical ones of the inventions disclosed in the present application will be described briefly as follows:

(1) A semiconductor integrated circuit device according to the present invention comprises a plurality of active regions each having an island-shaped plane pattern whose periphery is surrounded by shallow groove isolations, which are disposed on a main surface of a substrate so as to have predetermined intervals in a first direction, and semiconductor elements formed in the plurality of active regions, and wherein the sum of the width of each active region extending in the first direction and the space defined between the adjacent active regions constitutes a minimum pitch in the first direction, and the width of each active region in the first direction is set larger than one-half the minimum pitch.

(2) In a semiconductor integrated circuit device according to the item 1, the half of the minimum pitch is a minimum processing size determined according to a resolution limit of photolithography.

(3) In a semiconductor integrated circuit device according to the item 1 or 2, the semiconductor elements are respectively coupled to interconnections disposed so as to have predetermined intervals, and the width of each interconnection and the space between the adjacent

interconnections are respectively set to the minimum pitch.

(4) A semiconductor integrated circuit device according to the present invention comprises a plurality of active regions each having an island-shaped plane pattern whose periphery is surrounded by shallow groove isolations, which are disposed on a main surface of a substrate so as to have predetermined intervals in a first direction, and semiconductor elements formed in the plurality of active regions, and wherein the sum of the width of each active region extending in the first direction and the space defined between the adjacent active regions is set to twice a minimum processing size determined according to a resolution limit of photolithography, the width of each active region is greater than or equal to the minimum processing size and the space defined between the adjacent active regions is less than or equal to the minimum processing size.

(5) In a semiconductor integrated circuit device according to the item 2, 3 or 4, the semiconductor elements are respectively coupled to interconnections disposed so as to have predetermined intervals, and the width of each interconnection and the space between the adjacent interconnections are respectively set to the minimum processing size determined according to the resolution limit of photolithography.

(6) In a semiconductor integrated circuit device

according to the item 3 or 5, each of the semiconductor elements constitutes a memory cell, and each of the interconnections constitutes a word line or a bit line connected to the memory cell.

(7) In a semiconductor integrated circuit device according to any of the items 1 to 6, a peripheral portion of each active region whose periphery is surrounded by the shallow groove isolations, is shaped in the form of a section with a convex round.

(8) In a semiconductor integrated circuit device according to any of the items 1 to 7, the thickness of a gate insulating film of each semiconductor element formed on the surface of the substrate in each active region is equal in central and peripheral portions of the active region.

(9) In a semiconductor integrated circuit device according to any of the items 1 to 8, the semiconductor elements formed in each active region are comprised of MISFETs respectively, the MISFETs are memory cell selection MISFETs each of which constitutes part of each memory cell in a DRAM, and a capacitative element which constitutes another part of the memory cell in the DRAM, is connected in series with the memory cell selection MISFET.

(10) A method of manufacturing a semiconductor integrated circuit device, according to the present invention, comprises the following steps of:

forming silicon nitride films on a main surface of a substrate so that the sum of the width of each silicon nitride film extending in a first direction and the space defined between the adjacent silicon nitride films extending in the first direction constitutes a minimum pitch in the first direction,

forming side wall spacers on side walls of each silicon nitride film and thereafter defining grooves in the substrate in self-alignment with the side wall spacers,

removing the side wall spacers and thereafter oxidizing the substrate to thereby effect round processing on the surface of the substrate, and

forming an insulating film on the substrate including the interiors of the grooves and thereafter removing the insulating film lying outside the grooves, and embedding the insulating film in the grooves to thereby define shallow groove isolations for defining each active region.

(11) A method of manufacturing a semiconductor integrated circuit device, according to the present invention, comprises the following steps of:

selectively forming silicon nitride films on a main surface of a substrate,

forming side wall spacers on side walls of the silicon nitride films respectively and thereafter etching the substrate in self-alignment with the side wall

spacers to thereby define grooves in the substrate in each device isolation region,

removing the side wall spacers and thereafter subjecting the substrate to thermal oxidation to thereby effect round processing on the surface of the substrate at a peripheral portion of each active region, and

forming an insulating film on the substrate including the interiors of the grooves, thereafter removing the insulating film lying over each silicon nitride film and embedding the insulating film in the grooves to thereby define shallow groove isolations.

(12) A method of manufacturing a semiconductor integrated circuit device, according to the present invention, comprises the following steps of:

selectively forming silicon nitride films on a main surface of a substrate,

forming side wall spacers on side walls of the silicon nitride films respectively and thereafter etching the substrate in self-alignment with the side wall spacers to thereby define grooves in the substrate in each device isolation region,

removing the side wall spacers and thereafter subjecting the substrate to thermal oxidation to thereby effect round processing on the surface of the substrate at a peripheral portion of each active region,

etching each silicon nitride film to thereby recess a peripheral portion of each silicon nitride film to the

center side of the active region, and

forming an insulating film on the substrate including the interiors of the grooves, thereafter removing the insulating film lying over each silicon nitride film and embedding the insulating film in the grooves to thereby define shallow groove isolations for defining the active regions.

(13) In a method of manufacturing a semiconductor integrated circuit device, according to the item 12, the etching for recessing the peripheral portion of the silicon nitride film to the center side of the active region is isotropic etching.

(14) A method of manufacturing a semiconductor integrated circuit device, according to any of the items 10 to 13 further includes a step of subjecting the substrate to thermal oxidation after the insulating film is embedded in the grooves to thereby form a gate insulating film for each MISFET on the surface of the substrate in each active region and then form each gate electrode for the MISFET on the gate insulating film.

(15) A method of manufacturing a semiconductor integrated circuit device, according to the item 14 further includes a step of forming a silicon oxide film on the surface of the substrate in each active region prior to the gate insulating film forming step, a step of implanting impurity ions in the substrate through the silicon oxide film, a step of subjecting the substrate to

a thermal process to diffuse the impurity ions, thereby forming wells in the substrate, and a step of etching the surface of the substrate to thereby remove the silicon oxide film.

(16) In a method of manufacturing a semiconductor integrated circuit device, according to the item 14, the gate electrodes for the MISFETs extend across the active regions and the shallow groove isolations.

(17) In a method of manufacturing a semiconductor integrated circuit device, according to the item 14, the MISFETs are respectively memory cell selection MISFETs each of which constitutes part of each memory cell in a DRAM.

(18) In a method of manufacturing a semiconductor integrated circuit device, according to any of the items 10 to 17, each silicon nitride film has a slender and island-shaped plane pattern, and the size of each silicon nitride film in the first direction and the space defined between the silicon nitride films adjacent to each other in the first direction are respectively equal to a minimum size determined according to a resolution limit of photolithography.

(19) In a method of manufacturing a semiconductor integrated circuit device, according to the item 18, the gate electrodes for the MISFETs linearly extend along a second direction intersecting the first direction of each active region at the same widths and same spaces, and the

widths and spaces are respectively equal to a minimum size determined according to a resolution limit of photolithography.

(20) In a method of manufacturing a semiconductor integrated circuit device, according to any of the items 10 to 19, the side wall spacers comprise a silicon oxide film.

(21) In a method of manufacturing a semiconductor integrated circuit device, according to any of the items 10 to 20, the thickness of each side wall spacer ranges from 5nm to 40nm.

(22) A method of manufacturing a semiconductor integrated circuit device, according to any of the items 10 to 21 further includes a step of forming the side wall spacers on the side walls of the silicon nitride films and thereafter implanting impurity ions in the neighborhood of the surface of the substrate including regions below the side wall spacers prior to the step of defining the grooves in the substrate.

(23) In a method of manufacturing a semiconductor integrated circuit device, according to any of the items 10 to 22, when the substrate is etched in self-alignment with the side wall spacers to define the grooves, the neighborhood of the surface of the substrate is first isotropically etched to thereby isotropically etch the neighborhood of the surface of the substrate in the regions below the side wall spacers, and the substrate is

then anisotropically etched to define the grooves.

(24) In a method of manufacturing a semiconductor integrated circuit device, according to any of the items 10 to 23, the neighborhood of the surface of the substrate in the regions below the side wall spacers is isotropically etched after the removal of the side wall spacers, and the substrate is then subjected to thermal oxidation to thereby effect round processing on the surface of the substrate at the peripheral portion of each active region.

(25) In a method of manufacturing a semiconductor integrated circuit device, according to any of the items 10 to 24, the thermal oxidation for effecting the round processing on the surface of the substrate is performed plural times in parts.

(26) In a method of manufacturing a semiconductor integrated circuit device, according to any of the items 10 to 25, the inner walls of the grooves are etched prior to the step of embedding the insulating film in the grooves after the round processing of the surface of the substrate, whereby silicon oxide films formed on inner walls of the grooves by the thermal oxidation at the round processing are removed or thinned.

(27) In a method of manufacturing a semiconductor integrated circuit device, according to any of the items 10 to 26, the substrate is subjected to a thermal process after the insulating film is embedded in the grooves or

in the course thereof to thereby densify the insulating film.

(28) A method of manufacturing a semiconductor integrated circuit device, according to the present invention, comprises the following steps of:

(a) selectively forming silicon nitride films on main surfaces of first and second regions of a substrate,

(b) forming first side wall spacers on side walls of the silicon nitride films left on the substrate,

(c) covering the first region of the substrate with a first photoresist film and etching the first side wall spacers in the second region, thereby forming thin second side wall spacers thicker than the first side wall spacers on the side walls of the silicon nitride films in the second region,

(d) removing the first photoresist film and thereafter etching the substrate in self-alignment with the first side wall spacers and second side wall spacers, thereby defining grooves in the substrate,

(e) removing the first side wall spacers and second side wall spacers and thereafter subjecting the substrate to thermal oxidation, thereby effecting round processing on the surface of the substrate at a peripheral portion of each active region, and

(f) forming an insulating film on the substrate including the interiors of the grooves, thereafter removing the insulating film above each silicon nitride

film and embedding the insulating film in the grooves, thereby forming shallow groove isolations for defining each active region.

(29) A method of manufacturing a semiconductor integrated circuit device, according to the item 28, further includes, after the step (f), steps of:

(g) removing the silicon nitride films and performing an etching process for reducing a step between the surface of the substrate corresponding to the active region and the surface of the insulating film lying within each shallow groove isolation,

(h) subjecting the substrate to thermal oxidation to thereby form a first gate oxide film for a first MISFET on the surface of the substrate in the active region,

(i) covering the second region of the substrate with a second photoresist film and etching the surface of the first region of the substrate, thereby removing the first gate oxide film in the first region, and

(j) removing the second photoresist film and thereafter subjecting the substrate to thermal oxidation, thereby forming a second gate oxide film for a second MISFET on the surface of the first region of the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims

particularly pointing out and distinctly claiming the subject matter which is regarded as the invention, it is believed that the invention, the objects and features of the invention and further objects, features and advantages thereof will be better understood from the following description taken in connection with the accompanying drawings in which:

Fig. 1 is a fragmentary plan view of a substrate lying in the course of a process for manufacturing a semiconductor integrated circuit device showing one embodiment of the present invention;

Fig. 2 is an equivalent circuit diagram of a memory array in a DRAM;

Fig. 3 is a fragmentary cross-sectional view of the substrate taken along lines A - A′ and B - B′ in Fig. 1;

Fig. 4 is a fragmentary cross-sectional view of a substrate, which shows a method of manufacturing a semiconductor integrated circuit device according to an embodiment 1 of the present invention;

Fig. 5 is a fragmentary cross-sectional view of the substrate, which illustrates the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 6 is a fragmentary plan view of the substrate, which depicts the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 7 is a fragmentary cross-sectional view of the substrate, which shows the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 8 is a fragmentary plan view of the substrate, which illustrates the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 9 is a fragmentary cross-sectional view of the substrate, which shows the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 10 is a fragmentary cross-sectional view of the substrate, which illustrates the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 11 is a fragmentary cross-sectional view of the substrate, which depicts the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 12 is a fragmentary cross-sectional view of the substrate, which illustrates the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 13 is a fragmentary cross-sectional view of the substrate, which shows the method of manufacturing the semiconductor integrated circuit device according to

the embodiment 1 of the present invention;

Fig. 14 is a fragmentary cross-sectional view of the substrate, which depicts the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 15 is a fragmentary cross-sectional view of the substrate, which illustrates the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 16 is a fragmentary cross-sectional view of the substrate, which shows the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 17 is a fragmentary cross-sectional view of the substrate, which illustrates the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 18 is a fragmentary cross-sectional view of the substrate, which shows the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 19 is a fragmentary cross-sectional view of the substrate, which illustrates the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 20 is a fragmentary cross-sectional view of the substrate, which shows the method of manufacturing

the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Figs. 21(a) and 21(b) are respectively fragmentary cross-sectional views of the substrates, which show the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 22 is a fragmentary cross-sectional view of the substrate, which illustrates the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 23 is a fragmentary cross-sectional view of the substrate, which depicts the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 24 is a fragmentary cross-sectional view of the substrate, which shows the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 25 is a fragmentary plan view of the substrate, which illustrates the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 26 is a fragmentary cross-sectional view of the substrate, which shows the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 27 is a fragmentary plan view of the substrate, which illustrates the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 28 is a fragmentary cross-sectional view of the substrate, which depicts the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 29 is a fragmentary plan view of the substrate, which shows the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 30 is a fragmentary cross-sectional view of the substrate, which shows the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 31 is a fragmentary cross-sectional view of the substrate, which illustrates the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 32 is a fragmentary cross-sectional view of the substrate, which shows the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 33 is a fragmentary cross-sectional view of the substrate, which depicts the method of manufacturing the semiconductor integrated circuit device according to

the embodiment 1 of the present invention;

Fig. 34 is a fragmentary cross-sectional view of the substrate, which shows the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 35 is a fragmentary cross-sectional view of the substrate, which illustrates the method of manufacturing the semiconductor integrated circuit device according to the embodiment 1 of the present invention;

Fig. 36 is a fragmentary cross-sectional view of a substrate, which depicts a method of manufacturing a semiconductor integrated circuit device according to an embodiment 2 of the present invention;

Fig. 37 is a fragmentary cross-sectional view of the substrate, which shows the method of manufacturing the semiconductor integrated circuit device according to the embodiment 2 of the present invention;

Fig. 38 is a fragmentary cross-sectional view of the substrate, which illustrates the method of manufacturing the semiconductor integrated circuit device according to the embodiment 2 of the present invention;

Fig. 39 is a fragmentary cross-sectional view of the substrate, which depicts the method of manufacturing the semiconductor integrated circuit device according to the embodiment 2 of the present invention;

Figs. 40(a) and 40(b) are respectively fragmentary cross-sectional views of substrates, which show a method

of manufacturing a semiconductor integrated circuit device according to an embodiment 3 of the present invention;

Figs. 41(a) and 41(b) are respectively fragmentary cross-sectional views of the substrates, which show the method of manufacturing the semiconductor integrated circuit device according to the embodiment 3 of the present invention;

Figs. 42(a) and 42(b) are respectively fragmentary cross-sectional views of the substrates, which illustrate the method of manufacturing the semiconductor integrated circuit device according to the embodiment 3 of the present invention;

Figs. 43(a) and 43(b) are respectively fragmentary cross-sectional views of the substrates, which depict the method of manufacturing the semiconductor integrated circuit device according to the embodiment 3 of the present invention;

Figs. 44(a) and 44(b) are respectively fragmentary cross-sectional views of the substrates, which show the method of manufacturing the semiconductor integrated circuit device according to the embodiment 3 of the present invention;

Figs. 45(a) and 45(b) are respectively fragmentary cross-sectional views of the substrates, which depict the method of manufacturing the semiconductor integrated circuit device according to the embodiment 3 of the

present invention; and

Figs. 46(a) and 46(b) are respectively fragmentary cross-sectional views of the substrates, which show the method of manufacturing the semiconductor integrated circuit device according to the embodiment 3 of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will hereinafter be described in detail with reference to the accompanying drawings. Incidentally, ones or components having the same function in all the drawings for describing the embodiments are identified by the same reference numerals and the repetitive description thereof will therefore be omitted.

[Embodiment 1]

Fig. 1 is a fragmentary plan view of a substrate lying in the course of a manufacturing process, Fig. 2 is an equivalent circuit diagram of a memory array in a DRAM, and Fig. 3 is a cross-sectional view of the substrate taken along line A - A′ of Fig. 1 on the left side thereof and is a cross-sectional view of the substrate taken along line B - B′ of Fig. 1 on the right side thereof, respectively.

Active regions L whose peripheries are respectively defined by device isolation trenches or grooves or shallow groove isolations 2, are formed on a p type well

3 formed on a main surface of a substrate 1 comprised of, for example, p type mono-crystalline silicon. As shown in Fig. 1, the active regions L are respectively formed in slender and island-shaped plane patterns which extend in the direction taken along line A - A'. As also shown in Fig. 3, the surface of the substrate 1 (p type well 3) in or corresponding to each active region L takes a sectional form whose central portion is flat and whose peripheries (ends) are respectively shaped in the form of a convex round.

Two MISFETs (memory cell selection MISFETs Qs), which share one of the source and drain (n type semiconductor regions 10), are respectively formed within the active regions L. Each memory cell selection MISFET Qs and an information storage capacitative element C to be described later are electrically series-connected to each other and constitutes a one-bit memory cell MC of a DRAM (Dynamic Random Access Memory). As shown in Fig. 2, each memory cell MC is electrically coupled to a point where a word line WL and a bit line BL intersect.

Each of the memory cell selection MISFETs Qs is comprised principally of a gate oxide film 7 formed on the surface of the substrate 1 (p type well 3) corresponding to the active region L, a gate electrode 8 formed on the gate oxide film 7, and a pair of n type semiconductor regions 10, 10 (source and drain) formed in the substrate 1 (p type well 3) in the active region L.

As will be described later, either one of the n type semiconductor regions 10 and 10 (source and drain) is electrically connected to its corresponding bit line BL, whereas the other thereof is electrically connected to one electrode (lower electrode 33) of each information storage capacitative element C.

The gate electrode 8 of each memory cell selection MISFET Qs is formed integrally with its corresponding word line WL. Namely, the gate electrode 8 is electrically connected to its corresponding word line WL. The gate electrodes 8 (word lines WL) linearly extend at the same widths and intervals or spaces along the line B - B' of Fig. 1, i.e., the transverse direction of the active region L. The width (gate length) (Lw) thereof and the interval or space (Ls) thereof are respectively equal to the minimum size (e.g., 0.16μm = Lw = Ls) determined according to a resolution limit of photolithography.

Thus, each wiring pitch corresponding to the sum of the width (Lw) of each word line WL (gate electrode 8) and the interval or space (Ls) between the adjacent word lines WL (gate electrodes 8) is set to twice the minimum processing size. Thus, since the wiring pitch (Lw + Ls) in the direction in which each word line WL (gate electrode 8) extends, can be reduced, each memory cell can be miniaturized or scaled down and brought into high integration.

The gate electrode 8 (word line WL) is formed by a

polymetal structure in which a barrier metal film such as WN (tungsten nitride) and a W (tungsten) film are stacked over a low-resistance poly-crystalline silicon film doped with an n type impurity such as P (phosphorus). A silicon nitride film 9 having the same plane pattern as the gate electrode 8 (word line WL) is formed over each gate electrode 8 (word line WL).

As will be also described later, the bit lines BL are formed at the same line widths and same intervals or spaces along the direction in which they intersect the word lines WL (gate electrodes 8). The line width (Lw') and space (Ls') are respectively defined to the minimum size (e.g., 0.16μm) determined according to the resolution limit of photolithography (see Fig. 29).

As described above, each wiring pitch corresponding to the sum of the width (Lw') of each bit line BL and the spaced width (Ls') between the adjacent bit lines BL is set to twice the minimum processing size. Thus, since the wiring pitch (Lw' + Ls') in the direction in which each bit line BL extends, can be reduced, each memory cell can be miniaturized or scaled down and brought into high integration.

Each of the shallow groove isolations (device isolation regions) 2, which surround the substrate 1 (p type well 3) having the active regions L, is defined such that a silicon oxide film 6 is embedded inside trenches or grooves each having a depth of about 350nm, which are

defined in the substrate 1 (p type well 3). The surface of the silicon oxide film 6 is flattened and the height thereof is substantially equal to the surface of the substrate 1 (p type well 3) corresponding to each active region L. A thin silicon oxide film 11 for relaxing stress developed between the silicon oxide film 6 and the substrate 1 (p type well 3) is formed at an interface between an inner wall of each shallow groove isolation 2 and the silicon oxide film 6. Incidentally, the size (a) of the short side of each active region L forms a gate width (a) of each memory cell selection MISFET Qs.

A method of manufacturing the above-described DRAM will next be described in process order by using Figs. 4 through 35. Of these drawings, the left portions of Figs. 4, 5, 7, 9, 11 through 20, 22, 24, 26, 28 and 30 through 35 are respectively cross-sectional views of a substrate 1, which are taken along the longitudinal direction (the direction as seen along line A - A′ of Fig. 1) of each active region L, whereas the right portions thereof are respectively cross-sectional views of the substrate 1, which are taken along the transverse direction (the direction as seen along line B - B′ of Fig. 1) of each active region L. Only plane patterns for the active regions, gate electrodes (word lines), bit lines and connecting holes (contact holes and through holes) are respectively shown in plan views (Figs. 6, 8, 25, 27 and 29), and the illustration of insulating films (silicon

oxide film, silicon nitride film) and a conductive film constituting a plug will be omitted.

First, the substrate 1 comprised of p type monocrystalline silicon having a resistivity of from about 1 Ωcm to about 10Ωcm, for example is subjected to thermal oxidation at about 850°C. A thin oxide silicon film (first silicon oxide film) 13 having a thickness of about 10nm is formed on the surface of the substrate 1. Thereafter, a silicon nitride film 14 having a thickness of about 120nm is deposited over the silicon oxide film 13 by a CVD method. The silicon oxide film 13 between the silicon nitride film 14 and the substrate 1 is formed to relax stress developed at an interface between the substrate 1 and the silicon nitride film 14 and prevent defects such as dislocation from occurring in the surface of the substrate 1 due to the stress.

Next, the silicon nitride film 14 in each device isolation region and the silicon oxide film 13 located therebelow are selectively removed by dry etching with a photoresist film (not shown) as a mask as shown in Fig. 5. When the silicon oxide film is left even slightly on the surface of the substrate 1 corresponding to each device isolation region at this time, this lead to the occurrence of foreign substances. Therefore, the substrate 1 is overetched to completely remove the silicon oxide film on the surface thereof. The amount of overetching made to the substrate 1 may be about 10nm to

30nm. Further, the end of the overetched portion of the substrate 1 may preferably be tapered without being set vertically because it is easy to round upon the subsequent round processing.

As shown in Figs. 5 and 6, each silicon nitride film 14 left on the substrate 1 is formed in a slender and island-shaped plane pattern which defines each active region L. The size (W) of a short side thereof extending along line B - B' and the space (S) between the adjacent silicon nitride films 14 are respectively equal to the minimum size (e.g., 0.16μm = W = S) determined according to the resolution limit of photolithography. The size of a long side thereof extending along line A - A' of each silicon nitride film 14 is equal to five times (e.g., 0.8μm) the size (W) of the short side.

Thus, in the present embodiment, since the width Lw' of each bit line BL formed in the subsequent process and the space Ls' between the adjacent bit lines BL are respectively set to the minimum size determined according to the resolution limit of photolithography, the size (W) of the short side of each silicon nitride film 14 defining the active region L and the space (S) between the adjacent silicon nitride films 14 are respectively set to such a minimum size.

Next, as shown in Figs. 7 and 8, the silicon oxide film deposited over the substrate 1 by the CVD method is anisotropically etched to thereby form side wall spacers

16 on their corresponding side walls of each silicon nitride film 14.

The film thickness (spacer length) Lsi of each side wall spacer 16 referred to above is set to a range from 5nm to 40nm, preferably, 10nm to 20nm, more preferably, about 15nm. When a thermal oxidation process for performing round processing on a peripheral portion of the active region L in the subsequent process is performed where the spacer length is less than 5nm, the size of the short side of the post-process active region L would become smaller than the minimum size (e.g., 0.16μm) determined according to the resolution limit of photolithography. On the other hand, when the spacer length Lsi exceeds 40nm, the amount of rounding of the peripheral portion of each active region L becomes insufficient. Further, since an aspect ratio (corresponding to the depth/width of each groove or trench) of each trench or groove 2a defined in the substrate 1 having the device isolation regions in the subsequent process becomes large, the coverage of a silicon oxide film 6 to be embedded in the groove 2a and the flatness of the surface thereof result in insufficiency.

Next, impurity ions are implanted in the substrate 1 as shown in Fig. 9 to thereby give damage to the surface of the substrate 1 in a region serving as the peripheral portion of each active region L in the

subsequent process. Since the region, which serves as the peripheral portion of each active region L, is located below each side wall spacer 16 at this time, the impurity ions are implanted diagonally with respect to a main surface of the substrate 1 to damage the substrate 1 in this region. While the implantation of the impurity ions is not an essential process, the peripheral portion of each active region L is easy to round when the substrate 1 is subjected to thermal oxidation if the surface of the substrate 1 is damaged in advance and covalent bonds of silicon are locally cut off. When an element large in atomic weight, like Ge (Germanium) or As (arsenic) is used as the impurity, it is possible to give damage only to the surface of the substrate 1 corresponding to the peripheral portion of each active region L.

Next, foreign substances left on the surface of the substrate 1 are removed by cleaning using, for example, an SC-1 solution (mixed solution of ammonia solution/hydrogen peroxide solution) and an SC-2 solution (mixed solution of hydrochloric acid/hydrogen peroxide solution). Further, a native oxide film on the surface of the substrate 1 is removed by cleaning using hydrofluoric acid. While it is not an essential process, the peripheral portion of each active region L is easy to round in the subsequent process where the above cleaning is performed for a time interval longer than usual to isotropically etch the surface of the substrate 1,

thereby producing undercuts in the substrate 1 below each side wall spacer 16.

Next, as shown in Fig. 11, grooves 2a each having a depth of about 350nm are defined in the substrate 1 corresponding to each device isolation region by dry etching with the silicon nitride films 14 and side wall spacers 16 as masks. When the composition of a gas (e.g., $CF_4 + O_2$) for etching the substrate 1 is adjusted upon defining each groove 2a and a taper of 80° or thereabout is made to the side wall of the groove 2a, the silicon oxide film 6 deposited in the subsequent process becomes easy to be embedded inside the groove 2a. It is however needless to say that the angle of the taper is limited by the depth and width of each groove.

Next, as shown in Fig. 12, the side wall spacers 16 on the side walls of the silicon nitride films 14 are removed by wet etching using hydrofluoric acid. Incidentally, this is not an essential process. However, when wet etching using the SC-1 solution or the like is performed after the above wet etching, and the surface of the substrate 1 below each side wall spacer 16 is lightly rounded, the peripheral portion of each active region L becomes easy to round in the next thermal oxidation process.

Thus, in the present embodiment, the grooves 2a are defined in the substrate 1 corresponding to the device isolation regions by dry etching with the silicon nitride

films 14 and the side wall spacers 16 formed on their side walls as the masks. Thus, an actual size W' of each active region L becomes larger than a size W of the silicon nitride film 14 defining each active region L by a size equivalent to twice the thickness (spacer length) Lsi of each side wall spacer 16 ($W' = W + 2Lsi > W$). On the other hand, the space ($S' = S - 2Lsi < S$) between the adjacent active regions L extending along the transverse direction thereof becomes narrow correspondingly. Thus, when the size (W) of the short side of each silicon nitride film 14 defining the active region L and space between the adjacent silicon nitride films 14 are respectively set to the minimum size determined according to the resolution limit of photolithography ($W = S =$ minimum size), the actually obtainable size W' ($> W$) of the short side of each active region L becomes larger than the minimum size determined according to the resolution limit of photolithography, and the space (size of each groove 2a) S' ($< S$) between the adjacent active regions L extending along the transverse direction thereof becomes smaller than the minimum size.

Next, as shown in Fig. 13, the substrate 1 is subjected to thermal oxidation at a temperature of from about 850°C to about 1000°C to thereby form a thin silicon oxide film 11 having a thickness of about 10nm is formed on inner walls of the grooves 2a. The silicon oxide film 11 is formed to recover damage of dry etching, which has

been developed in the inner wall of each groove 2a and relax stress developed at an interface between the silicon oxide film 6 embedded inside each groove 2a in the subsequent process and the substrate 1 (p type well 3). Owing to the execution of this thermal oxidation process, the surface of the substrate 1 corresponding to the peripheral portion of each active region L is subjected to round processing, thus resulting in a sectional shape with a convex round.

As described above, the size of each active region L at the time that the grooves 2a are defined in the substrate 1 having the device isolation regions is larger than the size of each silicon nitride film 14 defining the active region L (by the size equivalent to twice the thickness of each side wall spacer 16). Therefore, even if the thin silicon oxide film 11 having the thickness of about 10nm is formed on the inner wall of each groove 2a, the size (a) of each active region L is not reduced as compared with the size (W) of the silicon nitride film 14. According to the present embodiment as described above, the surface of the substrate 1 at the end of each active region L can be subjected to round processing without reducing the size of the active region L.

Incidentally, the above-described thermal oxidation process for rounding the peripheral portion of each active region L may be performed twice in parts. Since the end becomes round to some extent in the first thermal

oxidation process in this case, the end can be easily rounded by the thermal oxidation process corresponding to the second time.

When the thickness of the silicon oxide film 11 becomes excessively thick, stress is developed in the peripheral portion of each active region L and the inner wall of each groove 2a as well as a reduction in the size of each active region L, so that defects are apt to occur. Thus, when the thermal oxidation process is performed twice in parts, for example, the end may be sufficiently rounded in the first thermal oxidation process and the second thermal oxidation process may be set as a light thermal process corresponding to such an extent that the forms of the peripheral portion of each active region L and the inner wall of each groove 2a are improved. In order to relax the above-described stress, the substrate 1 may be subjected to thermal processing in a high-temperature and hydrogen atmosphere prior to a process for executing the thermal oxidation process after the removal of the side wall spacers 16. Further, the silicon oxide film 11 may be removed by wet etching using hydrofluoric acid or the like after the execution of round processing, or the thickness of the silicon oxide film 11 may be thinned.

Next, a silicon oxide film 6 is deposited over the substrate 1 including the inside of each groove 2a by the CVD method as shown in Fig. 14. The silicon oxide film 6

is deposited thereon with a thickness (for example, a thickness of from about 450nm to about 500nm) thicker than the depth of each groove 2a and formed so as to be embedded inside each groove 2a without any space. The silicon oxide film 6 is deposited by a film growing or depositing method having good step coverage as in the case of a silicon oxide film grown by a CVD method using oxygen and tetraethoxysilane ($(C_2H_5)_4Si$), for example. Incidentally, a silicon nitride film (not shown) may be deposited thinly over the inner wall of each groove 2a by the CVD method prior to the process for depositing the silicon oxide film 6. This silicon nitride film has the function of retraining the thin silicon oxide film 11 on the inner wall of each groove 2a from growing thick on the active region L side upon densifying the silicon oxide film 6 embedded in each groove 2a.

Next, the densifying for improving the quality of the silicon oxide film 6 is executed by subjecting the substrate 1 to thermal oxidation at a temperature of from about 1000°C to about 1150°C. Thereafter, the silicon oxide film 6 provided over each groove 2a is polished by a chemical mechanical polishing (CMP) method to thereby flatten the surface thereof as shown in Fig. 15. This polishing is performed with the silicon nitride film 14 covering the substrate 1 corresponding to each active region L as a stopper. The time when slight over polishing is performed to such an extent that the surface

of each silicon nitride film 14 is exposed and the silicon oxide film 6 lying over each silicon nitride film 14 is not left behind, will be defined as an end point.

When the silicon oxide film 6 is flattened, the silicon oxide film 6 lying over each silicon nitride film 14 is first removed by dry etching with each photoresist film as a mask. Next, the photoresist film is removed and thereafter the silicon oxide film 6 left over each groove 2a may be polished by the CMP method. Further, the densifying of the silicon oxide film 6 may be performed after the flattening of the silicon oxide film 6. Since, in this case, the densifying thereof is carried out in a state in which the thickness of the silicon oxide film 6 is thin, a thermal processing condition can be reduced as compared with the case where the thick silicon oxide film 6 antecedent to its polishing is densified. Each shallow groove isolation 2 with the silicon oxide film 6 embedded in each groove 2a is substantially completed by the processes up to now.

Next, each silicon nitride film 14 covering the substrate 1 corresponding to each active region L is removed by wet etching using thermal phosphoric acid, whereby each silicon oxide film 13 located therebelow is made bare or exposed. When such etching is done, a step having a height equivalent to the thickness of the silicon nitride film 14 occurs between the surface of the silicon oxide film 13 and the surface of the silicon

oxide film 6 embedded in each shallow groove isolation 2.

Next, when the silicon oxide film 13 lying over the surface of the substrate 1 corresponding to each active region L is wet-etched by hydrofluoric acid as shown in Fig. 17, the surface of the substrate 1 corresponding to each active region L is exposed and at the same time the surface of the silicon oxide film 6 lying within each shallow groove isolation 2 is etched, so that the step is reduced.

When the above-described wet etching is done, the end of each silicon oxide film 6 lying within the shallow groove isolation 2, i.e., the sides as well as the upper surface of each silicon oxide film 6 lying in the region which has adjoined the silicon nitride film 14, are also subjected to an etchant. Therefore, the etched amount increases as compared with each portion distant from the active region L. However, since the size of each active region L is greater than that of the silicon nitride film 14 in the present embodiment, the end of each silicon oxide film 6 at the time that the silicon nitride film 14 has been removed, is located on the active region L side rather than the end of each shallow groove isolation 2. Therefore, even if the etched amount of the end of each silicon oxide film 6 increases, the silicon oxide film 6 is not recessed greatly downwards at the end of each shallow groove isolation 2.

Next, the substrate 1 is subjected to thermal

oxidation at about 850°C as shown in Fig.18 to thereby form a thin silicon oxide film 17 having a thickness of about 10nm on the surface of the substrate 1 corresponding to each active region L. The silicon oxide film 17 is formed to lessen the influence of damage to the substrate 1 and its contamination due to ion implantation of an impurity, which is to be performed in the following process.

Next, a p type impurity (boron) and an n type impurity (e.g., phosphorus) are ion-implanted in the substrate 1 through the silicon oxide films 17 to form wells (p type well 3 and n type well 4) as shown in Fig. 19. In order to form a p type semiconductor region (not shown) in which a channel for each memory cell selection MISFET Qs is formed, the p type impurity (boron) is ion-implanted in the substrate 1 through each silicon oxide film 17 referred to above. Impurity ions for forming the wells (p type well 3 and n type well 4) are implanted in a deep region of the substrate 1 with high energy, whereas impurity ions for forming each channel are implanted in a shallow region of the substrate 1 with low energy.

Next, the substrate 1 is subjected to thermal processing at about 950°C as shown in Fig. 20 to diffuse the impurities, thereby forming the p type well 3 and the n type well 4. The n type well 4 located below the p type well 3 is formed to prevent the entry of noise into the p

type well 3 through the substrate 1 from an unillustrated input/output circuit or the like.

Next, the silicon oxide film 17 provided on the surface of the substrate 1 is removed by wet etching using hydrofluoric acid and thereafter the substrate 1 is subjected to thermal oxidation at a temperature of from about 800°C to about 850°C, whereby a clean gate oxide film 7 having a thickness of about 7nm is formed on the surface thereof. Since the surface of the substrate 1 corresponding to the peripheral portion of each active region L is provided with the convex round as described above, the thickness of the gate oxide film 7 becomes substantially equal at the central and peripheral portions of each active region L.

The gate oxide film 7 may be comprised of a silicon oxynitride film whose part contains silicon nitride. Since the silicon oxynitride film has the high effect of restraining or controlling the occurrence of an interface state in the film and reducing an electronic trap as compared with the silicon oxide film, hot carrier resistance of the gate oxide film 7 can be improved. In order to form the silicon oxynitride film, the substrate 1 may be subjected to thermal oxidation in an atmosphere containing a nitrogen gas like NO or NO_2, for example.

Owing to the provision of the peripheral portion of each active region L with the round in this way, a thinning defect in the thickness of each gate oxide film

7 at the peripheral portion of each active region L is prevented from occurring, and an electric field based on a gate voltage is restrained from concentrating on the peripheral portion of each active region L. It is thus possible to prevent the occurrence of a MOS-IV kink characteristic (or hump characteristic) in which a drain current flows due to a low gate voltage, and a reduction in withstand voltage of each gate oxide film 7, whereby each memory cell selection MISFET Qs is improved in characteristic. Further, since a leakage current is restrained from occurring at the peripheral portion of each active region L, a refresh characteristic of each memory cell is improved. Furthermore, a variation in threshold voltage of each MISFET due to the thinning and MOS-IV kink characteristic is prevented from occurring.

Fig. 21(a) is a cross-sectional view taken along the direction extending along line B - B′ of the substrate 1 when the gate oxide films 7 have been formed. In the processes done up to now as shown in the drawing, the size (a) of the short side of each active region L becomes greater than or equal to the size (W) of the short side of the silicon nitride film 14 ($a \geq W$). Further, the interval or space (size of each shallow groove isolation 2) (b) between the adjacent active regions L along the short-side direction becomes less than or equal to the space (S) between the adjacent silicon nitride films 14 ($b \leq S$). Namely, when the size

(W) of the short size of each silicon nitride film 14 and the space (S) defined between the adjacent silicon nitride films 14 are respectively set to the minimum size (e.g., 0.16μm) determined according to the resolution limit of photolithography, the size (a) of the short side of each active region L reaches greater than or equal to the minimum size.

On the other hand, when each shallow groove isolation is defined by dry etching with only each silicon nitride film 14 as a mask without forming the side wall spacers 16 on their corresponding side walls of each pattern for the silicon nitride film 14 for defining each active region, and thereafter the peripheral portion of each active region is rounded by round processing corresponding to Fig. 13, the peripheral portion of each active region is sufficiently rounded according to this round process. Therefore, the size (a') of the short side of each active region L becomes smaller than the size (W) of the short side of each silicon nitride film 14, for defining the dimension of each active region L ($a' < W$), and the interval or space (corresponding to the size of the shallow groove isolation 2) (b') between the adjacent regions L extending along the direction of the short side becomes greater than the space (S) defined between the silicon nitride films 14 ($b' > S$). Namely, since the active region L cannot ensure the minimum size determined according to the resolution limit of photolithography in

this case, a memory cell cannot be formed.

Thus, even if the width (W') of the pattern for the silicon nitride film 14 and the space (S') between the patterns for the silicon nitride films 14, both of which are used to define the active region, are respectively set to the minimum processing size determined according to the resolution limit of photolithography for the purpose of high integration of the memory cell, the size (a) of the short side of the active region L, which is used as a gate width of each MISFET Qs, reaches the minimum processing size or more. Therefore, the MISFET Qs can be scaled down. Thus, the wiring pitch (Lw' + Ls') lying in the direction of the bit line BL is set to twice the minimum processing size to achieve high integration, and the size (a) of the active region L can be ensured, whereby the MISFET Qs can be scaled down.

Next, gate electrodes 8 (word lines WL) are formed over their corresponding gate oxide films 7 as shown in Fig. 22. The gate electrodes 8 (word line WL) are formed by, for example, depositing a low resistance poly-crystalline silicon film doped with phosphorus (P) over its corresponding gate oxide film 7 by a CVD method, then depositing a WN film and a W film over the low resistance poly-crystalline silicon film by a sputtering method, further depositing a silicon nitride film 9 over those films by the CVD method and thereafter patterning these films by dry etching with a photoresist film as a mask.

Each of the gate electrodes 8 (word lines WL) is formed such that the line width (gate length) thereof and space therebetween are respectively set to the minimum size (e.g., 0.16μm) determined according to the resolution limit of photolithography.

Fig. 23 is a cross-sectional view of the substrate 1 along the direction in which the gate electrodes 8 (word lines WL) extend. As shown in the drawing, the word lines WL extend across the short sides of the active regions L and the shallow groove isolations 2 and function as gate electrodes 8 of memory cell selection MISFETs Qs at upper portions of gate oxide films 7 formed on the surface of the substrate 1 corresponding to the active region L, respectively. Since the surface of the silicon oxide film 6 embedded in each shallow groove isolation 2 is not greatly recessed downwards in the neighborhood of the peripheral portion of the active region L in the present embodiment as described above, the end of the gate oxide film 7 does not reach the side wall of the shallow groove isolation 2 in which an impurity concentration for channel formation is lowered. It is thus possible to prevent the threshold voltage of the memory cell selection MISFET Qs from varying.

Next, an n type impurity (phosphorus or arsenic) is ion-implanted in a p type well 3 to form n type semiconductor regions 10 (sources and drains), whereby the memory cell selection MISFETs Qs shown in Figs. 1 and

3 are completed.

Next, as shown in Fig. 24, a silicon nitride film 18 having a thickness of from about 50nm to about 100nm is deposited over the substrate 1 by the CVD method and a silicon oxide film 20 having a thickness of about 600nm is deposited over the silicon nitride film 18 by the CVD method. Thereafter, the silicon oxide film 20 is polished by a CMP method so that the surface thereof is flattened.

Next, as shown in Figs. 25 and 26, the silicon oxide film 20 and silicon nitride film 18 lying over the sources and drains (n type semiconductor regions 10) of the memory cell selection MISFETs Qs are dry-etched with photoresist films (not shown) as masks to define contact holes 21 over one of the sources and drains (n type semiconductor regions 10) and define contact holes 22 over the other thereof. Thereafter, plugs 23 are respectively formed inside these contact holes 21 and 22. The contact holes 21 and 22 are defined in self alignment with the gate electrodes 8 with the silicon nitride film 18 as an etching mask. Further, the plugs 23 are formed by depositing a low resistance poly-crystalline silicon film doped with an n type impurity such as phosphorus (P) over the silicon oxide film 20 including the interiors of the contact holes 21 and 22 and thereafter etching back the poly-crystalline silicon film (or polishing it by the CMP method) to thereby leave it only inside the contact holes 21 and 22.

Next, as shown in Figs. 27 and 28, a silicon oxide film 24 having a thickness of about 200nm is deposited over the silicon oxide film 20 by the CVD method and thereafter dry-etched with a photoresist film (not shown) as a mask, whereby through holes 25 are defined above the contact holes 21 (plugs 23) respectively. As shown in Fig. 24, the through holes 25 are formed in such slender patterns that parts thereof extend above the shallow groove isolations 2.

Next, as shown in Figs. 29 and 30, plugs 26 are formed inside the through holes 25 respectively and thereafter bit lines BL are formed over the silicon oxide film 24. The plugs 26 are formed by depositing a Co film (or Ti film) over the silicon oxide film 24 including the interiors of the through holes 25 by the sputtering method, further depositing a TiN film and a W film thereon by the CVD method, thereafter polishing the W film, TiN film and Co film (or Ti film) lying over the silicon oxide film 24 by the CMP method, and leaving these films only inside the through holes 25.

Further, the bit lines BL are formed by depositing a W film having a thickness of about 200nm over the silicon oxide film 24 by the sputtering method and thereafter dry etching the W film with a photoresist film (not shown) as a mask. The bit lines BL are formed so as to linearly extend along the direction (direction taken along line A - A') orthogonal to the gate electrodes 8

(word lines WL) at the same line widths and same intervals or spaces. The width Lw' of each bit line BL and space Ls' defined between the adjacent bit lines BL are respectively defined as the minimum size (e.g., 0.16μm = Lw' = Ls' = Lw = Ls) determined according to the resolution limit of photolithography.

Next, as shown in Fig. 31, a silicon oxide film 27 having a thickness of about 300nm is deposited over each line BL by the CVD method as shown in Fig. 31. Thereafter, the silicon oxide film 27 and the silicon oxide film 24 provided therebelow are dry-etched to thereby form through holes 28 above the contact holes 22 (plugs 26) respectively.

In order to prevent plugs 29 formed inside the through holes 28 in the next process and the bit lines BL from being short-circuited, the through holes 28 are defined in a diameter smaller than the minimum size determined according to the resolution limit of photolithography. The through hole 28 having such a minute diameter is defined by the following method, for example.

First of all, a silicon oxide film 27 is deposited over each bit line BL and thereafter a first poly-crystalline silicon film (not shown) is deposited over the silicon oxide film 27. Next, the poly-crystalline silicon film is dry-etched with a photoresist film as a mask, whereby through holes are defined in the poly-

crystalline silicon film just above the contact holes 22 (plugs 26). The diameter of each through hole will be defined as the minimum size determined according to the resolution limit of photolithography.

Next, a second poly-crystalline silicon film is deposited over the first poly-crystalline silicon film including the interiors of the through holes and thereafter anisotropically etched to thereby leave it only on inner walls of the through holes, whereby side wall spacers are formed on the inner walls of the through holes. Thus, the diameter of each through hole becomes smaller than the minimum size determined according to the resolution limit of photolithography.

Next, through holes 28 are defined in the silicon oxide film 27 at the bottoms thereof and the silicon oxide film 24 located in a layer therebelow by dry etching with the first poly-crystalline silicon film and side wall spacers as masks. Thereafter, the unnecessary first poly-crystalline silicon film and side wall spacers are removed by etching.

Next, as shown in Fig. 32, plugs 29 are formed inside the through holes 28 and thereafter a silicon nitride film 30 having a thickness of about 100nm is deposited over its corresponding silicon oxide film 27 by the CVD method. Continuously, a thick silicon oxide film 31 having a thickness of about 1.3μm is deposited over the silicon nitride film 30 by the CVD method. The plugs

29 are formed by, for example, depositing a low resistance poly-crystalline silicon film doped with an n type impurity such as phosphorus (P) over the silicon oxide film 27 including the interiors of the through holes 28 and etching back the poly-crystalline silicon film to thereby leave it only inside the through holes 28. Further, the silicon nitride film 30 is used as an etching stopper used upon dry etching the silicon oxide film 31 in the next process.

Next, as shown in Fig. 33, the silicon oxide film 31 is dry-etched with a photoresist film (not shown) as a mask and thereafter the silicon nitride film 30 lying in a layer below the silicon oxide film 31 is wet-etched to thereby define trenches or grooves 32 above the through holes 28.

Next, as shown in Fig. 34, a low resistance poly-crystalline silicon film having a thickness of about 50nm, which is doped with the n type impurity such as phosphorus (P), is deposited over the silicon oxide films 31 including the interiors of the grooves 32 by the CVD method, and thereafter the poly-crystalline silicon film above the silicon oxide films 31 is removed by etchback, whereby lower electrodes 33 are formed along inner walls of the grooves 32 respectively.

Next, as shown in Fig. 35, a capacitive insulating film 34 comprised of, for example, a tantalum oxide film and an upper electrode 35 comprised of, for example, a

TiN film are formed over the lower electrodes 33. In order to form the capacitive insulating film 34 and the upper electrode 35, a thin tantalum oxide film having a thickness of about 20nm is first deposited over the silicon oxide films 31 including the interiors of the grooves 32 and a TiN film is then deposited over the tantalum oxide film by the CVD method and sputtering method, whereby the TiN film is embedded inside the grooves 32 without any space. Thereafter, the TiN film and tantalum oxide film are patterned by dry etching with a photoresist film (not shown) as a mask. Thus, each information storage capacitative element C comprising the lower electrode 33 comprised of the poly-crystalline silicon film, the capacitive insulating film 34 comprised of the tantalum oxide film and the upper electrode 35 comprised of the TiN film is formed. According to the processes up to now, each memory cell in the DRAM, which is comprised of the memory cell selection MISFET Qs and the information storage capacitative element C connected in series with it, is completed.

Thereafter, Al (aluminum) wires or interconnections corresponding to two layers or so are formed over the information storage capacitative element C, and a surface protective film is further formed over the Al interconnections. However, their illustrations will be omitted.

(Embodiment 2)

Fig. 36 is a cross-sectional view of a substrate 1, which shows a state in which grooves 2a are defined in the substrate 1 corresponding to device isolation regions by dry etching with silicon nitride films 14 and side wall spacers 16 (unillustrated in the same drawing) formed on their side walls as masks, the side wall spacers 16 are then removed by wet etching and thereafter the substrate 1 is subjected to thermal oxidation, whereby a thin silicon oxide film 11 is formed on inner walls of the grooves 2a and the surface of the substrate 1 corresponding to a peripheral portion of each active region L is subjected to round processing. Processes used up to now are the same as those (see Figs. 4 through 13) described in the aforementioned embodiment 1.

Next, the silicon nitride films 14 are isotropically etched by a dry etching process or the like as shown in Fig. 37. Owing to the present etching, the size of the silicon nitride film 14 is reduced and its peripheral portion is recessed toward the central side of each active region L. While the recessed amount of the silicon nitride film 14 is set to about 20nm, for example, it may be determined in consideration of the amount in which a silicon oxide film 6 to be embedded inside the grooves 2a in the subsequent process is recessed to the substrate 1 side in a process up to the formation of a gate oxide film 7 on the surface of the substrate 1 corresponding to each active region L.

According to the processes (see Figs. 14 ad 15) described in the embodiment 1, the silicon oxide film 6 is next deposited over the substrate 1 including the interiors of the grooves 2a by a CVD method and then densifying for improving the quality of the silicon oxide film 6 is performed. Thereafter, the silicon oxide film 6 lying above the grooves 2a is polished by a CMP method so that the surface thereof is flattened. According to the processes used up to now, shallow groove isolations 2 with the silicon oxide films 6 embedded inside the grooves 2a are substantially completed (see Fig. 38).

Next, the silicon nitride films 14 covering the substrate 1 corresponding to each active region L are removed by wet etching using thermal phosphoric acid in a manner similar to the embodiment 1, whereby silicon oxide films 13 located therebelow are made bare or exposed. When such etching is done, a step having a height equivalent to the remaining thickness of each silicon nitride film 14 occurs between the surface of the silicon oxide film 13 and the surface of the silicon oxide film 6 embedded in the shallow groove isolation 2. However, when the silicon oxide film 13 lying over the surface of the substrate 1 corresponding to the active region L is wet-etched by hydrofluoric acid, the surface of the substrate 1 corresponding to the active region L is exposed and at the same time the surface of each silicon oxide film 6 is etched, so that such a step is reduced (see Fig. 39).

When the above-described wet etching is performed, the end of each silicon oxide film 6 lying within the shallow groove isolation 2, i.e., the sides as well as the upper surface of the silicon oxide film 6 lying in the region which has contacted the silicon nitride film 14, are also subjected to hydrofluoric acid. Therefore, the etched amount increases as compared with each portion away from the active region L. However, since the periphery of the silicon nitride film 14 is recessed to the central side of each active region L and the amount of an offset between a peripheral portion of the active region L and a peripheral portion of the silicon nitride film 14 is made sufficiently great in advance in the present embodiment, the end of each silicon oxide film 6 at the time that the silicon nitride film 14 has been removed, is located on the side much near the center of the active region L rather than the peripheral portion of the active region L. Therefore, even if the end of the silicon oxide film 6 is recessed to the shallow groove isolation 2 side by wet etching for reducing each step referred to above, the silicon oxide film 6 is not greatly recessed downwards at the end of each shallow groove isolation 2. Since the subsequent processes are identical to those employed in the aforementioned embodiment 1, the description thereof will be omitted.

Thus, according to the present embodiment, since it is possible to prevent the occurrence of a failure that

the surface of the silicon oxide film 6 lying within each shallow groove isolation 2 is recessed downwards in the neighborhood of the active region L, a variation in the threshold voltage of each memory cell selection MISFET Qs can be controlled.

A manufacturing method according to the present embodiment, for recessing the peripheral portion of the silicon nitride film 14 to the central side of each active region L to thereby increase the amount of the offset between the peripheral portion of the active region L and the peripheral portion of the silicon nitride film 14 is particularly effective as countermeasures taken against the case in which a design rule for MISFETs becomes extremely fine and the mere formation of the side wall spacers 16 on the side walls of the silicon nitride films 14 disenables control on the recessing of each silicon oxide film 6 at the end of the shallow groove isolation 2.

Incidentally, it is desirable to perform the recessing of the silicon nitride films 14 due to the above-described isotropic etching after the execution of the thermal oxidation process for rounding the surface of the substrate 1 at the peripheral portion of each active region L. Since the surface of the substrate 1 corresponding to the inner walls of the grooves 2a is also etched to some extent and isotropically recessed when the dry etching for recessing the silicon nitride

films 14 is performed before the round processing, i.e., before the silicon oxide film 11 is formed on the inner wall of each groove 2a by the thermal oxidation process, the size of the active region L might be reduced.

(Embodiment 3)

A description will next be made of an embodiment in which the present invention is applied to a process for manufacturing an LSI (hereinafter called "DRAM-LOGIC mixed LSI") in which a DRAM and a logic LSI are formed on the same substrate.

The operation of the logic LSI at a high speed needs to form a gate oxide film as thin as possible. On the other hand, the DRAM requiring a high voltage upon a rise in the potential on each word line is not able to so thin the thickness of the gate oxide film in terms of ensuring of a withstand voltage. Thus, when the DRAM-LOGIC mixed LSI is manufactured, it is necessary to form at least two types of MISFETs different from each other in the thickness of the gate oxide film.

In a process for forming two types of gate oxide films different in thickness on the same substrate, a region for forming a thin gate oxide film on the substrate and a region for forming a thick gate oxide film thereon are different form each other in the amount of recessing of a silicon oxide film within each shallow groove isolation. It is therefore necessary to take measures for uniformizing the amount of its recessing

between the region for forming the thin gate oxide film and the region for forming the thick gate oxide film in terms of prevention of a variation in the characteristic of each MISFET.

Fig. 40 is a cross-sectional view of a substrate 1 in which according to the processes (see Figs. 4 through 8) described in the embodiment 1, silicon nitride films 14 are formed on the substrate 1 having active regions L with silicon oxide films 13 interposed therebetween, and thereafter side wall spacers 16A each comprised of a silicon oxide film are formed on their side walls. Here, Fig. 40(a) shows the substrate 1 having a logic region (first region) for forming a thin gate oxide film, and Fig. 40(b) illustrates the substrate 1 having a DRAM region (second region) for forming a thick gate insulating film, respectively. The processes used up to now are identical in logic and DRAM regions.

Next, as shown in Fig. 41, the substrate 1 having the logic region is covered with a photoresist film 41 and the side wall spacers 16A formed on the side walls of the silicon nitride films 14 in the DRAM region are etched, thereby thinning their film thicknesses (spacer lengths). Thus, two types of side wall spacers 16A and 16B different in spacer length are formed in the logic and DRAM regions respectively.

The photoresist film 41 is next removed. Thereafter, as shown in Fig. 42, grooves 2a are

thereafter defined in the substrate 1 having the logic region by dry etching with the silicon nitride films 14 and side wall spacers 16A as masks, and grooves 2a are defined in the substrate 1 having the DRAM region by dry etching with the silicon nitride films 14 and side wall spacers 16B as masks. Since, at this time, the side wall spacers 16A and 16B formed on the side walls of the silicon nitride films 14 are different from each other in spacer length, the amount of an offset between a peripheral portion of each active region L and a peripheral portion of the silicon nitride film 14 differ between the logic region and the DRAM region. Namely, the distance from the side wall (corresponding to the peripheral portion of the active region L) of each groove 2a to the peripheral portion of the silicon nitride film 14 becomes large in the logic region in which the side wall spacers 16A great in thickness are formed.

Next, the side wall spacers 16A and 16B formed on the side walls of the silicon nitride films 14 are removed by wet etching using hydrofluoric acid. Thereafter, the substrate 1 is subjected to thermal oxidation in accordance with the processes (see Figs. 13 through 15) described in the embodiment 1 as shown in Fig. 43, whereby a thin silicon oxide film 11 is formed on the inner walls of the grooves 2a and the surface of the substrate 1 at the peripheral portion of each active region L is subjected to round processing. Thereafter, a

silicon oxide film 6 deposited over the substrate 1 including the interiors of the grooves 2a is densified and the silicon oxide films 6 lying above the grooves 2a are then polished by a CMP method, whereby the surfaces thereof are flattened. According to the processes up to now, shallow groove isolations 2 with the silicon oxide films 6 embedded inside the grooves 2a are substantially completed.

As described above, the logic region is larger than the DRAM region in the distance (amount of offset) between the peripheral portion of the active region L and the peripheral portion of the silicon nitride film 14. Therefore, the end of the silicon oxide film 6 lying within each shallow groove isolation 2 is located on the center side of the active region L in the case of the logic region rather than the DRAM region.

Next, as shown in Fig. 44, the removal of the silicon nitride films 14, the removal of the silicon oxide film 13 by wet etching and the formation of each silicon oxide film 17, ion implantation of an impurity through the silicon oxide film 7 and the formation of wells (p type well 3 and n type well 4) by thermal processing, and the removal of the silicon oxide film 17 by wet etching are performed in accordance with the processes (see Figs. 16 through 20) described in the embodiment 1. Thereafter, a clean gate oxide film 7 having a thickness of from about 6nm to about 7nm is

formed on the surface of the substrate 1 corresponding to the respective active regions L in the logic and DRAM regions.

When the silicon oxide film 13 is wet-etched, the end of each silicon oxide film 6 is recessed toward the shallow groove isolation 2 side. Since the end of the silicon oxide film 6 is located on the center side of each active region L in the case of the logic region rather than the DRAM region, the amount of recessing of the silicon oxide film 6 at the end of the shallow groove isolation 2 is reduced in the case of the logic region.

Next, as shown in Fig. 45, the substrate 1 having the DRAM region is covered with a photoresist film 42 and the gate oxide film 7 provided on the surface of the substrate 1 having the logic region is selectively removed by wet etching using hydrofluoric acid, whereby the surface of the substrate 1 is exposed. When such wet etching is done, the surface of each silicon oxide film 6 embedded in the shallow groove isolation 2 in the logic region is also etched simultaneously, and the end thereof is recessed toward the shallow groove isolation 2 side. Since the substrate 1 having the DRAM region is covered with the photoresist film 42 at this time, the gate oxide film 7 formed on the surface of the substrate 1 lying in this region and the silicon oxide film 6 lying within each shallow groove isolation 2 are not etched. As a result, the amount of recessing of the silicon oxide film

6 at the end of each shallow groove isolation 2 becomes substantially identical in the logic and DRAM regions.

Next, the photoresist film 42 is removed and thereafter the substrate 1 is subjected to thermal oxidation as shown in Fig. 46, whereby a thin gate oxide film 7A having a thickness of about 4nm is formed on the surface of the substrate 1 having the logic region. The gate oxide film 7 formed on the surface of the substrate 1 having the DRAM region by the thermal oxidation is further oxidized, so that it grows to a thick gate oxide film 7B having a thickness of from about 8nm to about 9nm.

Thus, according to the present embodiment, since the amount of recessing of the silicon oxide film 6 at the end of each shallow groove isolation 2 can be uniformized in the logic region for forming each thin gate oxide film 7A and the DRAM region for forming each thick gate oxide film 7B, variations in characteristics of MISFETs formed in the logic region and MISFETs formed in the DRAM region can be reduced.

According to the present embodiment in which the grooves 2a are defined in the substrate 1 in the device isolation regions by dry etching with the silicon nitride films 14 and the side wall spacers 16A and 16B formed on their side walls as the masks, an effect similar to that obtained in the embodiment 1 can be also obtained.

While the invention made by the present inventors has been described above specifically by the embodiments,

the present invention is not necessarily limited to the embodiments. It is needless to say that various changes can be made thereto within the scope not departing from the substance thereof.

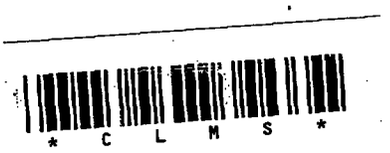
While the embodiments have described the case in which the invention is principally applied to the DRAM, the present invention is not limited to this. The present invention can be widely applied to various LSIs wherein fine MISFETs are formed on a substrate having shallow groove isolations.

Industrial Utility

Advantageous effects obtained by typical ones of the inventions disclosed in the present application will be described briefly as follows:

According to the present invention, a peripheral portion of each active region can be subjected to round processing without reducing the size of the active region, thus making it possible to facilitate scale down of MISFETs.

According to the present invention, since it is possible to prevent a failure that a silicon oxide film lying in each shallow groove isolation is recessed in the neighborhood of a peripheral portion of each active region, the characteristic of a scaled-down MISFET can be improved.



WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a plurality of active regions each having an island-shaped plane pattern whose periphery is surrounded by shallow groove isolations, said active regions being disposed on a main surface of a substrate so as to have predetermined intervals in a first direction; and

semiconductor elements formed in said plurality of active regions; and

wherein the sum of the width of said each active region extending in the first direction and the space defined between said adjacent active regions constitutes a minimum pitch in the first direction, and the width of said each active region in the first direction is set larger than one-half the minimum pitch.

2. A semiconductor integrated circuit device according to claim 1, wherein the half of the minimum pitch is a minimum processing size determined according to a resolution limit of photolithography.

3. A semiconductor integrated circuit device according to claim 1 or 2, wherein said semiconductor elements are respectively coupled to interconnections disposed so as to have predetermined intervals, and the

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width of said each interconnection and the space between said adjacent interconnections are respectively set to said minimum pitch.

4. A semiconductor integrated circuit device comprising:

a plurality of active regions each having an island-shaped plane pattern whose periphery is surrounded by shallow groove isolations, said active regions being disposed on a main surface of a substrate so as to have predetermined intervals in a first direction; and

semiconductor elements formed in said plurality of active regions; and

wherein the sum of the width of said each active region extending in the first direction and the space defined between said adjacent active regions is set to twice a minimum processing size determined according to a resolution limit of photolithography, the width of said each active region is greater than or equal to the minimum processing size and the space defined between said adjacent active regions is less than or equal to the minimum processing size.

5. A semiconductor integrated circuit device according to claim 2, 3 or 4, wherein said semiconductor elements are respectively coupled to interconnections disposed so as to have predetermined intervals, and the



width of said each interconnection and the space between said adjacent interconnections are respectively set to the minimum processing size determined according to the resolution limit of photolithography.

6. A semiconductor integrated circuit device according to claim 3 or 5, wherein said each semiconductor element constitutes a memory cell, and said each interconnection constitutes a word line or a bit line connected to said memory cell.

7. A semiconductor integrated circuit device according to any of claims 1 to 6, wherein a peripheral portion of said each active region whose periphery is surrounded by said shallow groove isolations, is shaped in the form of a section with a convex round.

8. A semiconductor integrated circuit device according to any of claims 1 to 7, wherein the thickness of a gate insulating film of said each semiconductor element formed on the surface of the substrate in said each active region is equal in central and peripheral portions of said active region.

9. A semiconductor integrated circuit device according to any of claims 1 to 8, wherein said semiconductor elements formed in said each active region

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are comprised of MISFETs respectively, said MISFETs are memory cell selection MISFETs each of which constitutes part of each memory cell in a DRAM, and a capacitative element which constitutes another part of the memory cell in the DRAM, is connected in series with said memory cell selection MISFET.

10. A method of manufacturing a semiconductor integrated circuit device, comprising the following steps of:

forming silicon nitride films on a main surface of a substrate so that the sum of the width of said each silicon nitride film extending in a first direction and the space defined between said adjacent silicon nitride films extending in the first direction constitutes a minimum pitch in the first direction;

forming side wall spacers on side walls of said each silicon nitride film and thereafter defining grooves in the substrate in self-alignment with said side wall spacers;

removing said side wall spacers and thereafter oxidizing the substrate to thereby effect round processing on the surface of the substrate; and

forming an insulating film on the substrate including the interiors of said grooves and thereafter removing the insulating film lying outside said grooves, and embedding the insulating film in said grooves to



thereby define shallow groove isolations for defining each active region.

11. A method of manufacturing a semiconductor integrated circuit device, comprising the following steps of:

selectively forming silicon nitride films on a main surface of a substrate;

forming side wall spacers on side walls of said silicon nitride films respectively and thereafter etching the substrate in self-alignment with said side wall spacers to thereby define grooves in the substrate in each device isolation region;

removing said side wall spacers and thereafter subjecting the substrate to thermal oxidation to thereby effect round processing on the surface of the substrate at a peripheral portion of each active region; and

forming an insulating film on the substrate including the interiors of said grooves, thereafter removing the insulating film lying over said each silicon nitride film and embedding the insulating film in said grooves to thereby define shallow groove isolations.

12. A method of manufacturing a semiconductor integrated circuit device, comprising the following steps of:

selectively forming silicon nitride films on a main

surface of a substrate;

forming side wall spacers on side walls of said silicon nitride films respectively and thereafter etching the substrate in self-alignment with said side wall spacers to thereby define grooves in the substrate in each device isolation region;

removing said side wall spacers and thereafter subjecting the substrate to thermal oxidation to thereby effect round processing on the surface of the substrate at a peripheral portion of each active region;

etching said each silicon nitride film to thereby recess a peripheral portion of said each silicon nitride film to the center side of said each active region; and

forming an insulating film on the substrate including the interiors of said grooves, thereafter removing the insulating film lying over said each silicon nitride film and embedding the insulating film in said grooves to thereby define shallow groove isolations for defining the active regions.

13. A method according to claim 12, wherein the etching for recessing the peripheral portion of said silicon nitride film to the center side of said active region is isotropic etching.

14. A method according to any of claims 10 to 13, further including a step of subjecting the substrate to

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thermal oxidation after the insulating film is embedded in the grooves to thereby form a gate insulating film for each MISFET on the surface of the substrate in said each active region and then form each gate electrode for said MISFET on said gate insulating film.

15. A method according to claim 14, further including a step of forming a silicon oxide film on the surface of the substrate in said each active region prior to said gate insulating film forming step, a step of implanting impurity ions in the substrate through said silicon oxide film, a step of subjecting the substrate to a thermal process to diffuse said impurity ions, thereby forming wells in the substrate, and a step of etching the surface of the substrate to thereby remove said silicon oxide film.

16. A method according to claim 14, wherein the gate electrodes for said MISFETs extend across said active regions and said shallow groove isolations.

17. A method according to claim 14, wherein said MISFETs are respectively memory cell selection MISFETs each of which constitutes part of each memory cell in a DRAM.

18. A method according to any of claims 10 to 17,

wherein said each silicon nitride film has a slender and island-shaped plane pattern, and the size of said each silicon nitride film in the first direction and the space defined between said silicon nitride films adjacent to each other in the first direction are respectively equal to a minimum size determined according to a resolution limit of photolithography.

19. A method according to claim 18, wherein the gate electrodes for the MISFETs linearly extend along a second direction intersecting the first direction of said each active region at the same widths and same spaces, and said widths and spaces are respectively equal to a minimum size determined according to a resolution limit of photolithography.

20. A method according to any of claims 10 to 19, wherein said side wall spacers comprise a silicon oxide film.

21. A method according to any of claims 10 to 20, wherein the thickness of said each side wall spacer ranges from 5nm to 40nm.

22. A method according to any of claims 10 to 21, further including a step of forming the side wall spacers on the side walls of said silicon nitride films and

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thereafter implanting impurity ions in the neighborhood of the surface of the substrate including regions below said side wall spacers prior to the step of defining the grooves in the substrate.

23. A method according to any of claims 10 to 22, wherein when said substrate is etched in self-alignment with said side wall spacers to define the grooves, the neighborhood of the surface of the substrate is first isotropically etched to thereby isotropically etch the neighborhood of the surface of the substrate in the regions below said side wall spacers, and said substrate is then anisotropically etched to define the grooves.

24. A method according to any of claims 10 to 23, wherein the neighborhood of the surface of the substrate in the regions below the side wall spacers is isotropically etched after the removal of the side wall spacers, and the substrate is then subjected to thermal oxidation to thereby effect round processing on the surface of the substrate at the peripheral portion of said each active region.

25. A method according to any of claims 10 to 24, wherein the thermal oxidation for effecting the round processing on the surface of the substrate is performed plural times in parts.

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26. A method according to any of claims 10 to 25, wherein the inner walls of the grooves are etched prior to the step of embedding the insulating film in the grooves after the round processing of the surface of the substrate, whereby silicon oxide films formed on inner walls of the grooves by the thermal oxidation at the round processing are removed or thinned.

27. A method according to any of claims 10 to 26, wherein said substrate is subjected to a thermal process after the insulating film is embedded in the grooves or in the course thereof to thereby densify the insulating film.

28. A method of manufacturing a semiconductor integrated circuit device, comprising the following steps of:

(a) selectively forming silicon nitride films on main surfaces of first and second regions of a substrate;

(b) forming first side wall spacers on side walls of the silicon nitride films left on the substrate;

(c) covering the first region of the substrate with a first photoresist film and etching the first side wall spacers in the second region, thereby forming thin second side wall spacers thicker than the first side wall spacers on the side walls of the silicon nitride films in

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the second region;

(d) removing the first photoresist film and thereafter etching the substrate in self-alignment with the first side wall spacers and second side wall spacers, thereby defining grooves in the substrate;

(e) removing the first side wall spacers and second side wall spacers and thereafter subjecting the substrate to thermal oxidation, thereby effecting round processing on the surface of the substrate at a peripheral portion of each active region; and

(f) forming an insulating film on the substrate including the interiors of the grooves, thereafter removing the insulating film above said each silicon nitride film and embedding the insulating film in the grooves, thereby forming shallow groove isolations for defining each active region.

29. A method according to claim 28, further including, after said step (f), steps of:

(g) removing the silicon nitride films and performing an etching process for reducing a step between the surface of the substrate corresponding to the active region and the surface of the insulating film lying within said each shallow groove isolation;

(h) subjecting the substrate to thermal oxidation to thereby form a first gate oxide film for a first MISFET on the surface of the substrate in the active

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region;

(i) covering the second region of the substrate with a second photoresist film and etching the surface of the first region of the substrate, thereby removing the first gate oxide film in the first region; and

(j) removing the second photoresist film and thereafter subjecting the substrate to thermal oxidation, thereby forming a second gate oxide film for a second MISFET on the surface of the first region of the substrate.