

PATENT SPECIFICATION (11)

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DRAWINGS ATTACHED (19)



- (21) Application No. 26140/71 (22) Filed 19 April 1971
(31) Convention Application No. 26374 (32) Filed 7 April 1970 in
(33) United States of America (US)
(44) Complete Specification published 22 Aug. 1973
(51) International Classification H01L 5/00
(52) Index at acceptance
H1K 217 223 22Y 273 287 288 312 341 34Y 353 361 362 36Y
374 37Y 413 418 41Y 422 42X 51Y 530 578 579 583
611 618 619 61Y 629

(54) SEMICONDUCTOR DEVICE FABRICATION

(71) We, RCA CORPORATION, a corporation organised under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices of the type comprising an insulating substrate and a number of semiconductor components on the substrate.

Certain types of semiconductor devices, such as integrated circuits of the "silicon-on-sapphire" type, comprise one or more extremely thin, e.g., a few microns thick, layers of semiconductor materials on an insulating substrate, the various layers containing regions of different conductivity characteristics providing a number of individual semiconductor components, e.g., transistors and diodes.

An advantage of such devices is that owing to the thinness of the semiconductor material layers and the fact that the layers are supported by a substrate of insulating material, the degree of electrical coupling among the various components is small. A problem associated with the use of the thin semiconductor layers, however, is the difficulty of providing the various regions with the particular conductivity characteristics desired of the individual semi-conductor components of the device. That is, the various processing sequences heretofore used tend to interact and affect all the components of the substrate, whereby it has been difficult, in the past, to fabricate devices having closely spaced components of widely differing conductivity characteristics. Also, while a main advantage of such devices is the electrical isolation obtainable among the various components on the substrate, in some instances even more complete isolation than was heretofore available is required.

According to the invention we provide a method of providing individual semiconduc-

tor components of differing electrical conductivity characteristics on an insulating substrate comprising forming a first layer of semiconductor material on a portion of said substrate, covering said first layer with a masking layer, covering said first layer, said masking layer, and other portions of said substrate with a second layer of semiconductor material having a conductivity characteristic different from that of said first layer, removing portions of said second layer to leave a portion of said second layer on said substrate spaced from said first layer and forming a junction device within each of said first and second layers, the device formed in said first layer being of a conductivity characteristic different from that of the device formed in said second layer.

In the accompanying drawings:

Figures 1 to 6 are cross-sectional views of a semiconductor wafer workpiece, the various figures illustrating a sequence of operations performed on the workpiece in accordance with the instant invention.

With reference to Figure 1, herein, an insulating substrate 10 is shown having a first layer 12 of a semiconductor material thereon. In the instant embodiment, the substrate 10 is of monocrystalline sapphire, and the semiconductor material is an epitaxially deposited layer of monocrystalline silicon.

In general, the substrate 10 can comprise any of a number of materials on which a semiconductor material, such as silicon, germanium, silicon carbide, various III-V compounds, or the like, can be deposited. Examples of suitable substrate materials are sapphire, spinel, diamond, and silicon carbide. Although not limited thereto, the instant invention has particular utility in the fabrication of devices utilizing epitaxially deposited monocrystalline semiconductor materials, especially silicon, germanium, and gallium arsenide. With presently known techniques, the epitaxial deposition of monocrystalline layers of these materials requires the use of a monocrystalline substrate having a crystal lattice spacing similar to the crystal lattice spacing of the material being deposited,

e.g., substrates of sapphire or spinel for epitaxial depositions of silicon or germanium.

Returning to a consideration of Figure 1, the layer 12 has a specific conductivity characteristic dependent upon the particular device being fabricated. By "conductivity characteristic" is meant both the degree of conductivity and the type of conductivity, and the phrase "different conductivity characteristics", as used hereafter, encompasses both differences in the type of conductivity and differences in degrees of conductivity of the same type.

For purposes of illustration, in the instant embodiment, the layer 12 comprises 1 ohm-cm P type silicon having a thickness of one micron.

Using known photolithographic techniques, including the use of masking layers and photoresist materials, portions of the layer 12 are removed leaving a single region 14 of P type silicon, as shown in Figure 2.

For convenience of illustration and description, only a single P region is shown. It will be appreciated, however, that in actual practice, a number of spaced P regions are generally formed on the substrate.

Thereafter, a masking layer 16, as shown in Figure 3, is formed on the P region 14. In a preferred embodiment, the masking layer 16 comprises an oxide of the material of the region 14, provided, for example, by known thermal growth techniques. Using such techniques, all the exposed surfaces of the P region 14 are coated with the masking layer 16. This prevents any contact of the semiconductor material of the P region 14 with the semiconductor material layer to be subsequently deposited, as described hereinafter.

Alternatively, a masking layer, such as silicon oxide, silicon nitride, or the like, can be applied as a separate layer covering the entire substrate and the region 14, and thereafter photolithographically defined to cover only the P region 14.

Thereafter, a second layer 20 (Figure 4) of a semiconductor material, 2 ohm-cm N type monocrystalline silicon, in the instant embodiment, is epitaxially deposited on the substrate 12 including the region 14. Owing to the presence of the masking layer 16, there is no contact between the two layers 20 and 12, hence little possibility of cross-doping therebetween. Also, because the second layer 20 is provided independently of the first layer 12, the conductivity characteristics of the second layer 20, as well as the thickness thereof, can be selected independently of the conductivity characteristics of the first layer 12, and can be as desired depending upon the particular device being fabricated.

Thereafter, a second region 24 (Figure 5) comprising N type silicon is defined using known photolithographic techniques, including an etching process to remove portions of

the silicon layer 20 not protected by a defined layer of photoresist material (not shown). Preferably, an etchant is used which does not attack the material of the masking layer 16 covering the first region 14, whereby this region 14 is not disturbed by the second region defining process.

This protection of the first region 14 in the second region 24 forming step is an advantage of the instant invention. It has been found that owing to the extreme thinness of the layers used, it is somewhat difficult to remove the second layer from the first layer without simultaneously removing the first layer.

Various combinations of masking layer materials, photoresists, and etchants for practicing the above-described steps with various semiconductor materials are known.

An advantage of covering all the exposed surfaces of the first region 14 with the masking layer 16 is that, as mentioned, there is no contact between the second layer 20 and the first layer 12 along the sides of the region 14. Experience has shown that the process of completely separating two bodies of the same semiconductor material having the same or similar lattice structure is somewhat difficult with respect to reproducibility and control over the process.

The resulting structure, comprising two regions 14 and 24, formed substantially independently of one another and spaced from one another, is shown in Figure 5. The masking layer 16 can be removed or left in place, depending upon the particular device being fabricated.

Having provided the two regions 14 and 24, a different semiconductor component is formed in each. With reference to Figure 6, an example of one type of semiconductor component which can be formed in each region is shown. The component 30, formed in the region 14, is a P-channel field effect transistor having a source region 32 of N conductivity type, a channel region 34 of P conductivity type, and a drain region 36 of N conductivity type. Covering the surface 40 of the region 14 is an insulating layer 42 which can, although not necessarily, be the masking layer 16 originally provided on the region 14. Extending through openings through the layer 42 are a source electrode 44 connected to the source region 32, and a drain electrode 46 connected to the drain region 36. A gate electrode 50 is provided on top of the layer 42 overlying the channel region 34.

The component 56, formed in the region 24, is similar to the component 30 with the exception that the conductivity type of the various source, drain, and channel regions is the opposite of those of the component 30.

Details of the fabrication of the individual

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components 30 and 56, with the regions 14 and 22 as the starting point in the process, are not provided since various techniques for fabricating various semiconductor components, including components different from the components 30 and 56 shown herein, in thin films of semiconductor material are well known.

Of importance herein, however, is the fact that individual films or regions of semiconductor material can be provided on a substrate in a simple and reproducible manner, the various regions being formed independently of one another, and having the exact conductivity characteristics and thickness desired of the semiconductor components to be made therefrom. Also, while the space between the regions 14 and 24 can be filled in, preferably with an insulating material, such as silicon dioxide, or a semiconductor material including a blocking junction, in certain devices, such as that shown in Figure 6, the space between the regions is left empty. This provides reduced electrical coupling between the semiconductor components from region to region in comparison with devices where the different conductivity characteristic regions touch one another.

While, in the example shown, the two regions 14 and 24 are formed of the same kind of semiconductor material, different semiconductor materials for each region, e.g., silicon for one and gallium arsenide for the other, can be used. The only requirement for such usage is that each material be compatible with the substrate 10.

WHAT WE CLAIM IS:—

1. A method of providing individual semiconductor components of differing electrical

conductivity characteristics on an insulating substrate comprising forming a first layer of semiconductor material on a portion of said substrate, covering said first layer with a masking layer, covering said first layer, said masking layer, and other portions of said substrate with a second layer of semiconductor material having a conductivity characteristic different from that of said first layer, removing portions of said second layer to leave a portion of said second layer on said substrate spaced from said first layer, and forming a junction device within each of said first and second layers, the device formed in said first layer being of a conductivity characteristic different from that of the device formed in said second layer.

2. A method as claimed in claim 1, wherein said forming step includes the step of forming said masking layer on all sides of said first layer not in contact with said substrate to prevent any contact between said second layer and said first layer.

3. A method as claimed in claim 1, wherein said second layer is provided with a thickness different from the thickness of said first layer.

4. A method as claimed in claim 1, wherein said second layer is formed of a material different from the material of said first layer.

5. A method of providing individual semiconductor components of differing electrical conductivity substantially as described herein.

For the Applicants,
MATTHEWS, HADDAN & Co.,
Chartered Patent Agents,
Haddan House,
33 Elmfield Road,
Bromley, BR1 1SU.

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For the Applicants,
MATTHEWS, HADDAN & Co.,
Chartered Patent Agents,
Haddan House,
33 Elmfield Road,
Bromley, BR1 1SU.

(10498)

Printed in Scotland by Her Majesty's Stationery Office
at HMSO Press, Edinburgh, 1973.

Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY,
from which copies may be obtained.

