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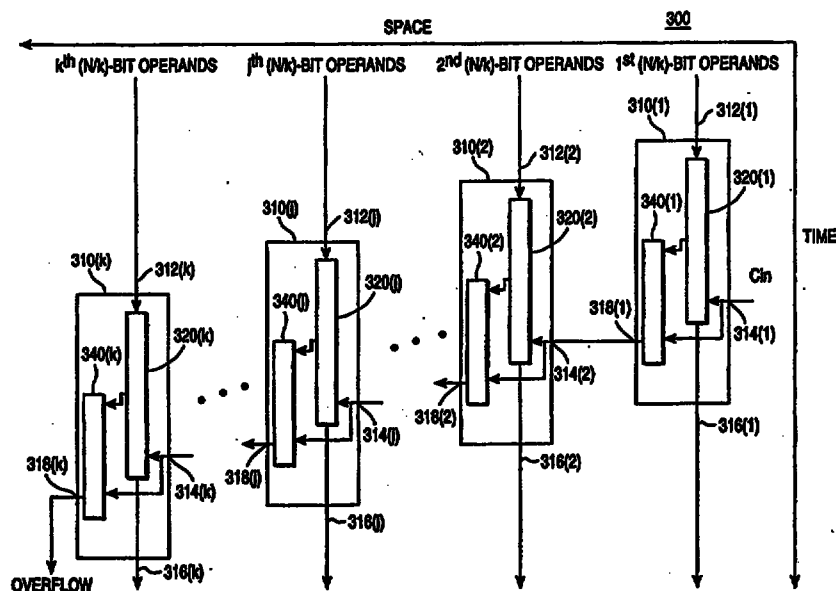
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(54) Title: SPATIALLY PIPELINED ARITHMETIC LOGIC UNIT



(57) Abstract

The present invention provides a 64-bit adder having 4 spatially pipelined, 16-bit adder blocks (310). Each adder block includes 16-bit sum and carry-out logic configured in parallel. The sum logic (320) of an adder block provides a 16-bit result (326) to an associated block output, according to 16-bit operands (312) and a carry-in signal (314) input to the adder block. The carry-out logic (340) of an adder block determines a carry-in signal (318) for an adjacent adder block. The first adder block provides a 16-bit result to its associated block output at a speed determined by the latency of the 16-bit sum logic. The 16-bit results from the next three adder blocks are determined sequentially, as the carry in from each preceding 16-bit block becomes available.