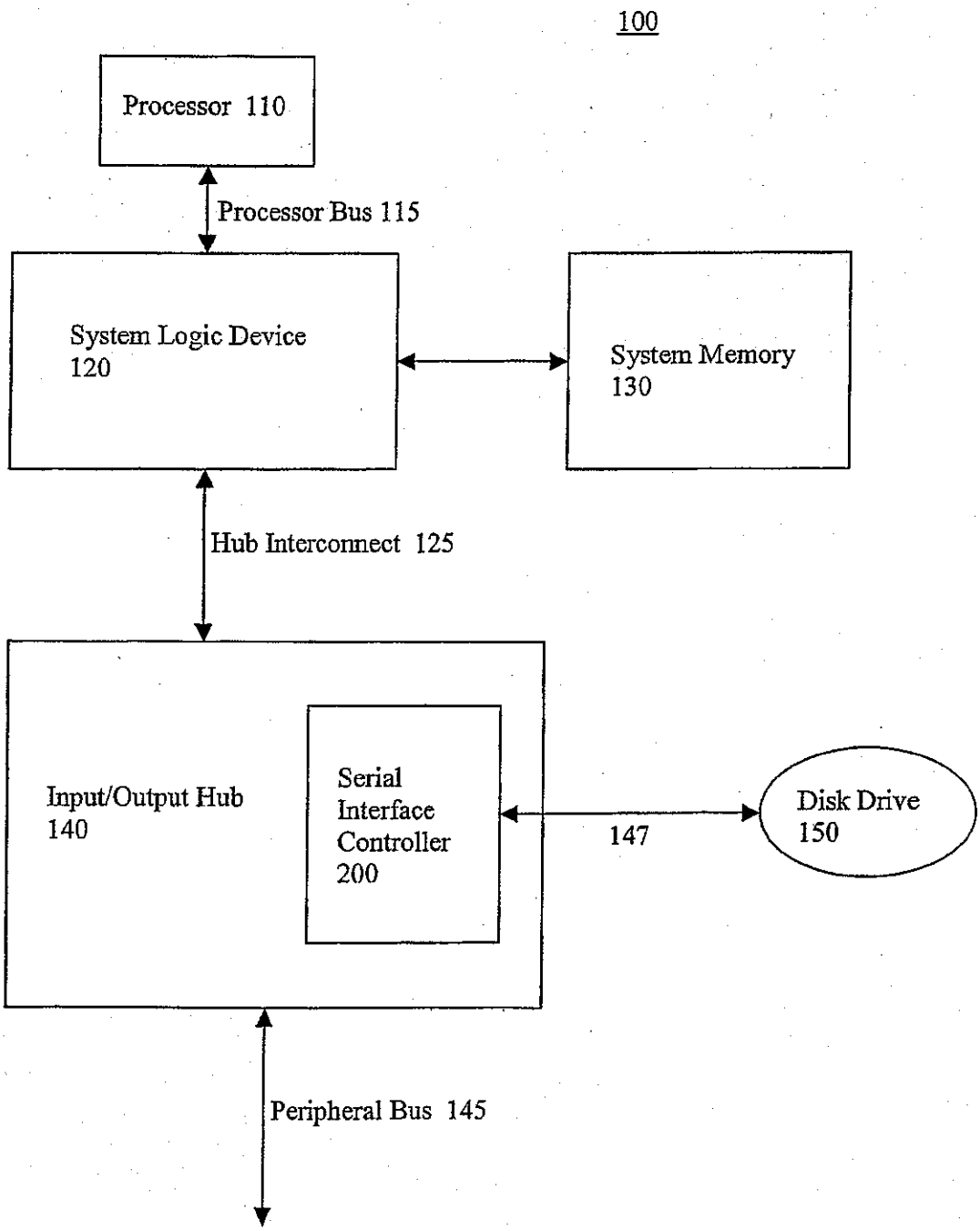

100
Processor 110
Processor Bus 115
System Logic Device
120
System Memory
130
Hub Interconnect 125
Input/Output Hub
140
Serial
Interface
Controller
200
147
Disk Drive
150
Peripheral Bus 145

Figure 1

200

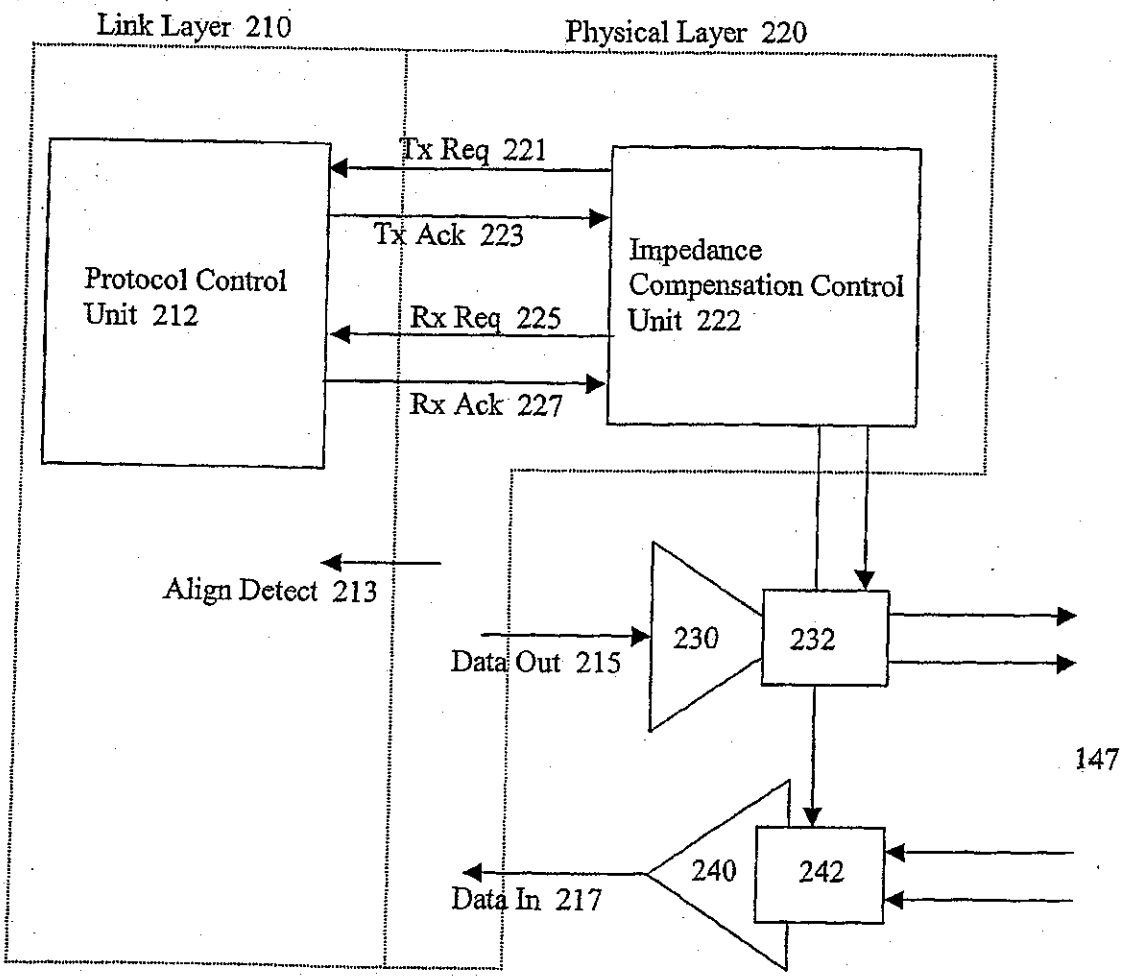

Link Layer 210
Physical Layer 220
Protocol Control Unit 212
Tx Req 221
Tx Ack 223
Rx Req 225
Rx Ack 227
Impedance Compensation Control Unit 222
Align Detect 213
Data Out 215
230
232
147
240
242
Data In 217

Figure 2

19 MAY 2006

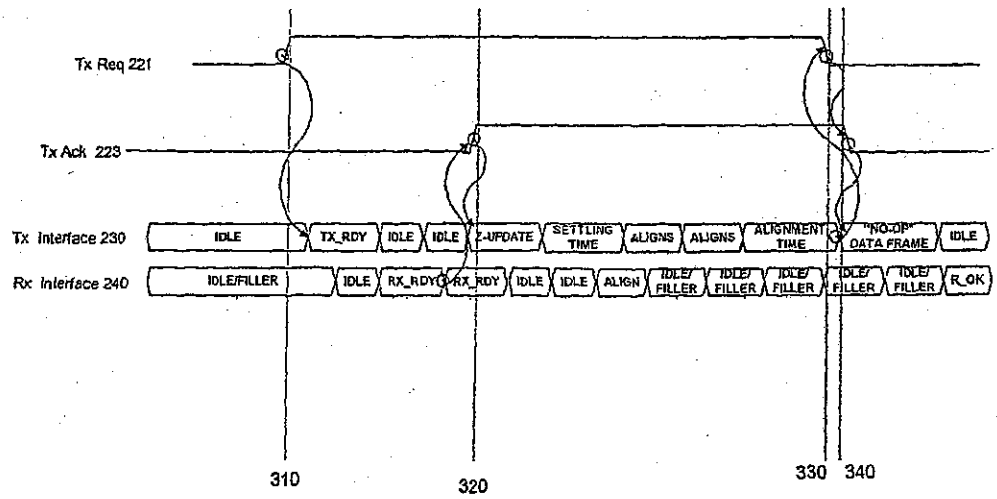


Figure 3

19 MAY 2006

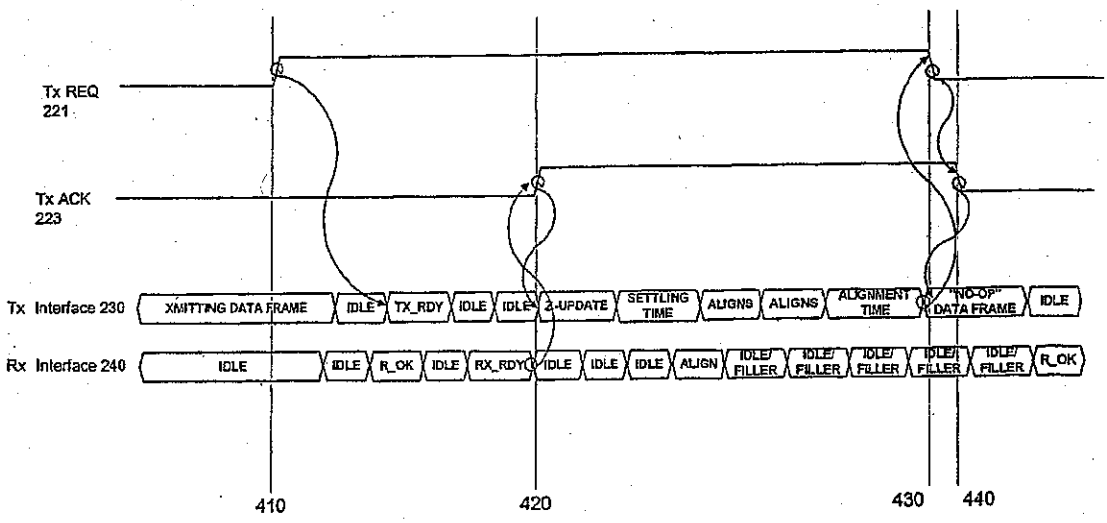


Figure 4

19 MAY 2006

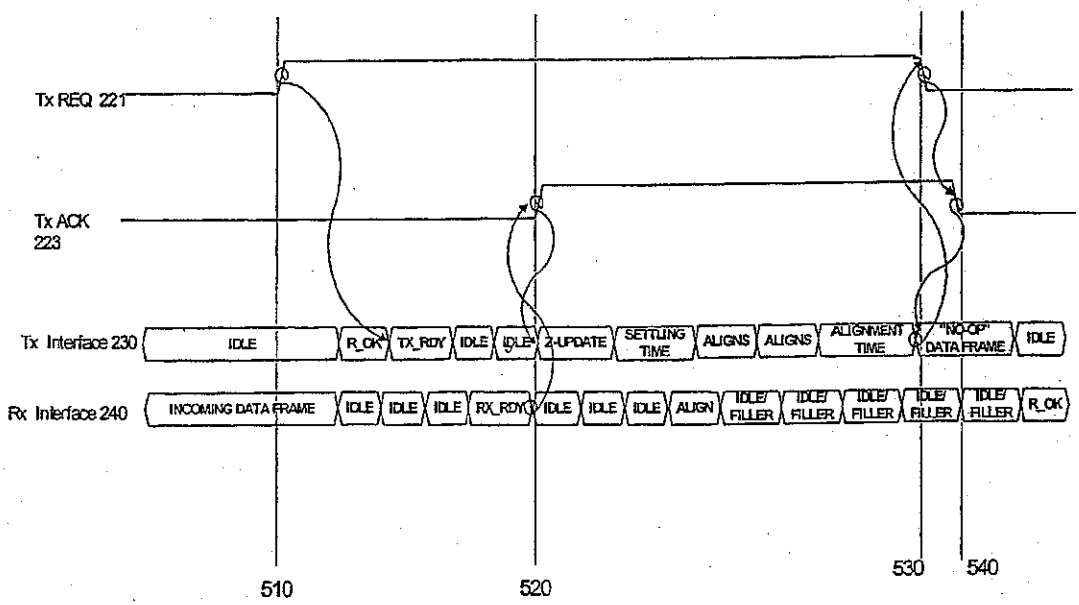


Figure 5

19 MAY 2006

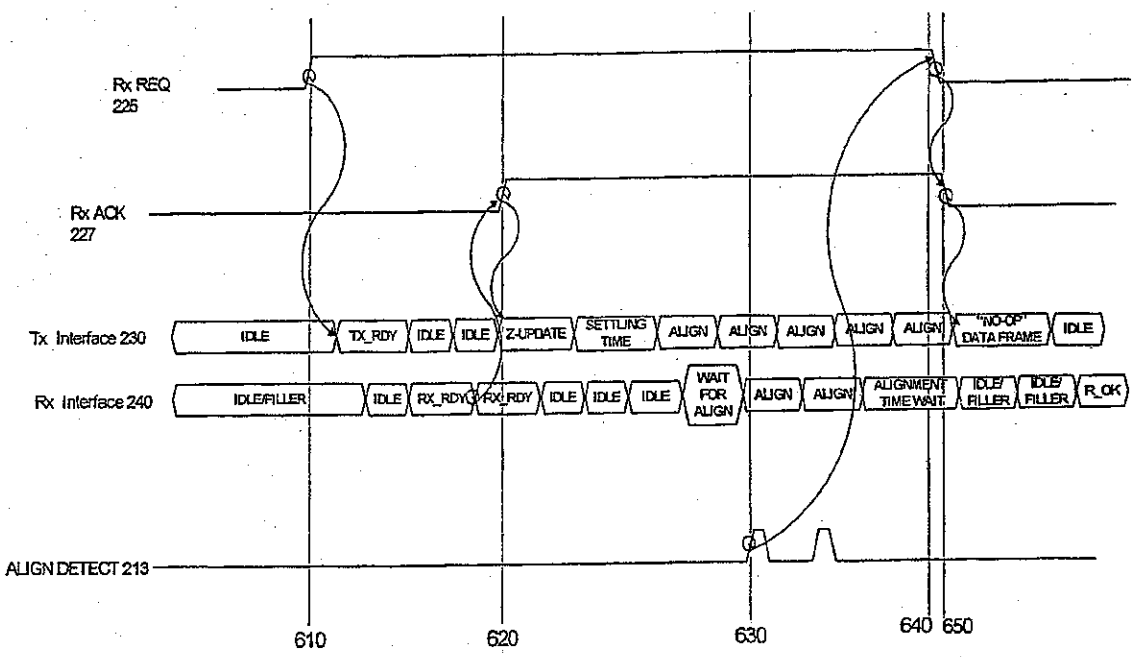


Figure 6

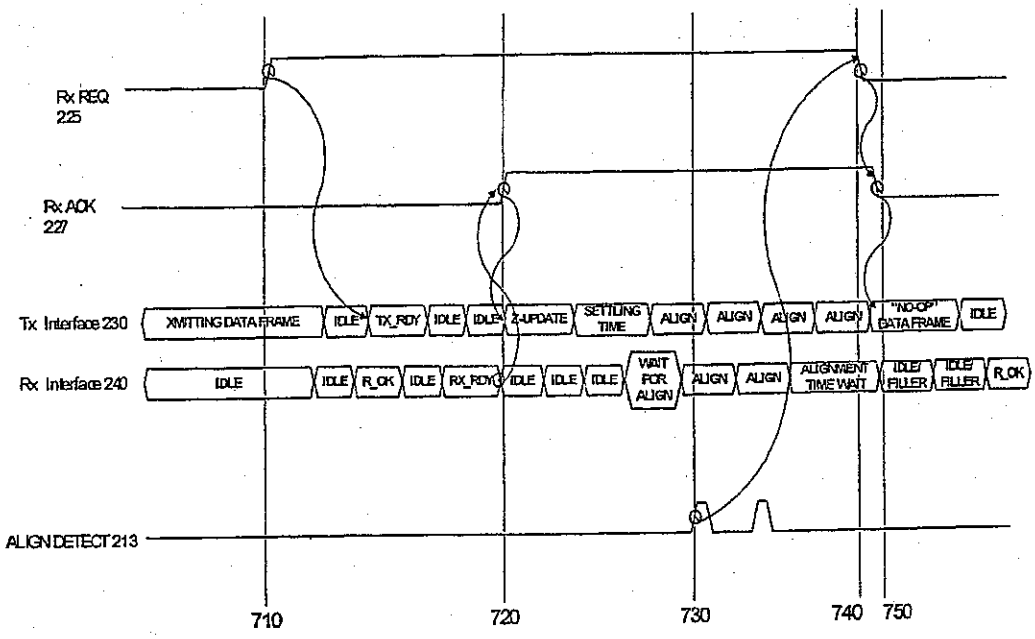

Rx REQ
225
Rx ACK
227
Tx Interface 230
XMITTING DATA FRAME
IDLE
TX_RDY
IDLE
IDLE
Z-UPDATE
SETTLING TIME
ALIGN
ALIGN
ALIGN
ALIGN
"NO-OP" DATA FRAME
IDLE
Rx Interface 240
IDLE
IDLE
R_OK
IDLE
RX_RDY
IDLE
IDLE
IDLE
WAIT FOR ALIGN
ALIGN
ALIGN
ALIGNMENT TIME WAIT
IDLE/ FILLER
IDLE/ FILLER
R_OK
ALIGN DETECT 213
710
720
730
740
750

Figure 7

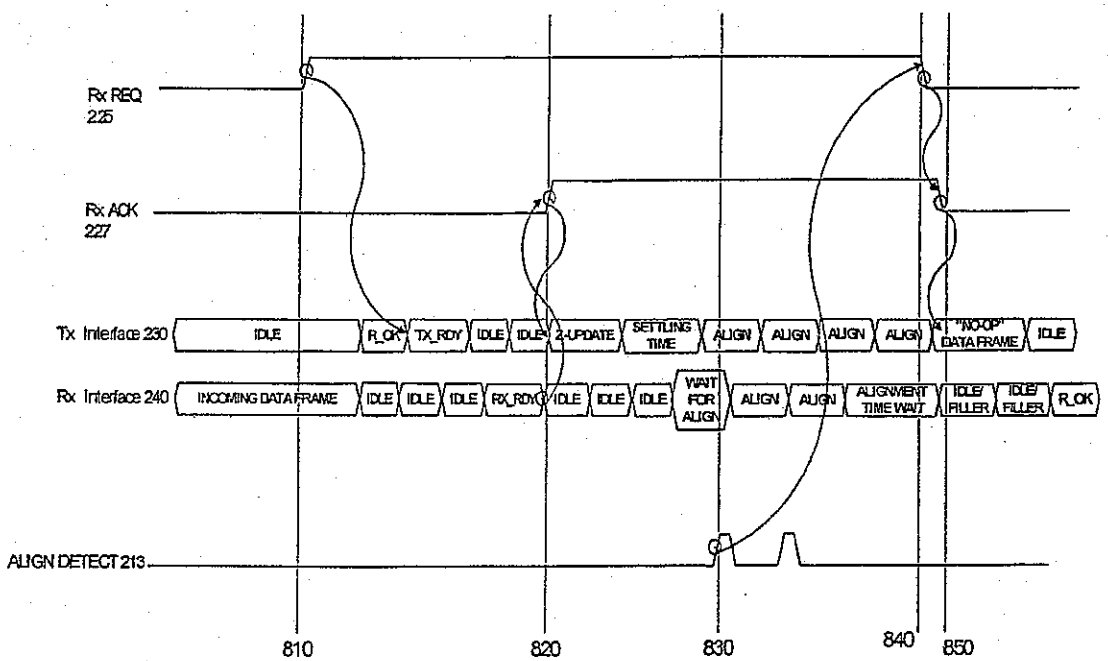

Rx REQ
225
Rx ACK
227
Tx Interface 230
IDLE
R_OK
TX_RDY
IDLE
IDLE
2-UPDATE
SETTLING TIME
ALIGN
ALIGN
ALIGN
ALIGN
"NO-OP" DATA FRAME
IDLE
Rx Interface 240
INCOMING DATA FRAME
IDLE
IDLE
IDLE
RX_RDY
IDLE
IDLE
IDLE
WAIT FOR ALIGN
ALIGN
ALIGN
ALIGNMENT TIME WAIT
IDLE/ FILLER
IDLE/ FILLER
R_OK
ALIGN DETECT 213
810
820
830
840
850

Figure 8