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- 1 -



TEST AND BURN-IN APPARATUS, IN-LINE SYSTEM USING THE APPARATUS, AND TEST METHOD USING THE SYSTEM

Background of the Invention

Field of the Invention

5 The present invention relates generally to an apparatus and method for testing semiconductor devices. More particularly, the present invention relates to the test and burn-in apparatus for semiconductor chip package devices, an in-line system including the apparatus, and test method employing the system

Description of the Prior Art

10 The manufacturing process for semiconductor devices has generally three sub-processes: wafer fabrication; package assembly; and back-end process. The wafer fabrication encompasses the processes that create a large number of circuits in and on a thin disc, i.e., a wafer, of semiconductor material such as silicon. The package assembly is the process in which an individual chip which has been separated from the wafer is assembled in a package
15 for establishing interconnections and a suitable operating environment. The back-end process includes several steps including test steps where the packaged devices are tested to determine their parameters and whether the devices perform their intended function, and sort steps in which the tested devices are sorted according to their individual parameters

 FIG. 1 is a flow chart illustrating a conventional overall back-end process 80 for
20 semiconductor devices 89. As shown in FIG. 1, the conventional back-end process 80 includes four test steps 81, 82, 83 and 84, three associated sort steps 91, 92 and 93, a marking step 85, a visual inspection step 86, a packing step 87, and a stocking step 88. Four test steps include DC test 81, burn-in 82, room/cold test 83, and hot sort test 84, for instance,

- 2 -

which are performed in sequence

When the assembled devices 89 in package form are provided to the back-end process 80, the DC test 81 is done to detect electrical failures which occur during the package assembly process. Failed devices are scrapped at the first sort step 91, while good devices
5 are transferred to the burn-in step 82. The assembled devices 89 provided to the DC test step 81 have been loaded in a device tray. After the DC test 81, good devices in the device tray should be shifted to a burn-in board during the first sort step 91. The burn-in board containing the devices which were DC tested is then supplied to the burn-in step 82.

The burn-in 82 is the uncommon test in which the devices are subjected to extreme
10 conditions such as high temperature in order to pre-screen out early device failures that might take place during actual usage. The burn-in board is returned to the first sort step 91 after the burn-in 82. The devices in the burn-in board are then sorted depending on burn-in results. The sorted devices are again loaded in the device tray for transferring to next test step 83. Although the first sort step 91 appears as single block in FIG. 1 for clarity, several
15 processes are actually done such as moving the devices from the device tray to the burn-in board, from the burn-in board to the device tray, scrapping the devices after the DC test, and sorting the devices after the burn-in. In most cases, both steps of the first sort 91 and of the DC test 81 are carried out at the same stage.

The step next to the burn-in 82 is the room/cold test 83. The good devices stored in
20 the device tray are provided to a room/cold tester, a handler of which shifts the devices from the device tray to a test tray for the room/cold test 83. The room/cold test 83 is carried out at about 25°C, i.e., room temperature or below 0°C, so that DC failures or function failures can be checked. As the room/cold test 83 operation is completed, the devices in the test tray are sorted depending on test results and simultaneously shifted again to the device tray which
25 will carry the devices to next test step 84. The second sort step occurs at step 92, which is carried out by the handler of the room/cold tester. As described above, the test tray which is

- 3 -

equipped in the tester is used to carry the devices to and from the contact parts of the tester, while the device tray carries the devices between two testers.

The room/cold-tested devices on the device tray are transferred to the hot sort test step 84 which is performed under high temperature conditions approaching about 83°C. The hot sort test 84, as widely known in the art, checks the electrical or functional characteristic of the devices and determines the speed thereof. Similarly to the room/cold test 83, the hot sort test 84 needs additional step of removing the devices from the device tray and placing them in the test tray and vice versa. Moving the devices from tray to tray is carried out by the handler (that is, a handling equipment) of the tester. The third sort step 93 associated with the hot sort step 84 is carried out together with the shifting of the devices by the handler after the hot sort test 93 is done.

Such conventional testers require, in general, additional equipment for handling the devices to be tested and which have been tested, such being the handler. However, the vexatious shifts of the devices between two trays every test step do not add any value in the performance of the tests. In other words, the complicated processes by the handler, per se, have no meaning for the purposes of the tests. Moreover, the handlers require space and time for moving the devices. Therefore, increasing space and time due to the handlers make it difficult to systematize in-line back-end process and further drop productivity. Also the devices may be faced with considerable damage during movement between two trays. Accordingly, the improvement in the back-end process is required in the light of a desire for more throughput to lower costs.

Meanwhile, it is desirable to combine a sort step of the devices after every test step into only one step, if possible. In relation to this, when a new material arrives at this area, this is handled by lot ID number. Human operator needs to input this ID to generate test result and to count output out of input accordingly. From the process of device loading to unloading, there are general steps inside handler regardless test function itself. Test tray

- 4 -

index time, soaking hot or cold temp process time, and sorting time must be included in device loading/unloading time between trays' transfer. It is worse when the rework is required following main process. Because total processing time between start and end in the handler needs lots of time to be prepared before real test, and combine the output
5 accordingly. Besides, human operator has to count the total output and record test result on every lot traveller card. The prior retest is a serial type on same machine at different test steps whenever it happens.

In addition, typically burn-in testers have capability of a slow test rate and a low test accuracy, as well known in the art. Furthermore, typical burn-in testers have a long serial
10 scanning time compared with normal testers. For example, MBT P1700S model of JEC Co., which has a long cycle (i.e., the test rate of 4MHz maximum and the transition time of approximately 50ns), is capable of performing some tests such as a gross function test or a long cycle test, in addition to the burn-in. It is, however, not able to perform the room/cold test or the hot sort test requiring more short cycle testing. The reason why the test rate of
15 typical burn-in testers is slow is that test signals are applied in parallel to the devices in every row or every column through circuit patterns on the burn-in board. This further raises another problem which is that it is difficult to apply test signals to the specific device. Meanwhile, there exists another significant problem that a long time is required in the current burn-in testers. Furthermore, the excessive test time is compounded by the time it takes to
20 load/unload the devices between the burn-in board and the device tray, the time it takes to load/unload the burn-in board, the time it takes to raise/drop the test temperature, and/or the time it takes to check the burn-in process or signals. In addition, the burn-in board and its test sockets are high-priced expendables. Accordingly, all of the above-discussed steps which are required for every semiconductor device impose a heavy cost burden on the end-
25 consumer.

Summary of the Invention

It is therefore an object of the present invention to provide an improved testing apparatus for semiconductor devices, which allows various tests including a burn-in test at the same platform

5 It is another object of the present invention to provide an in-line system throughout back-end process, employing less space-occupying apparatuses.

It is still another object of the present invention to provide an improved testing method including burn-in with reduced steps, requiring less time and less space.

10 It is still another object of the present invention to provide a directly transferable testing system employing test trays, eliminating the unnecessary moving of the devices between different trays

It is still another object of the present invention to provide the single composite sort step for various tests and burn-in, and a parallel type retest which is independent of machine by previous test result with test tray maps and data automation.

15 These and other objects are attained by a test and burn-in apparatus for semiconductor devices in accordance with the present invention. In particular, the test and burn-in apparatus in accordance with the present invention includes at least one rail for transferring plural test trays, each of which containing a plurality of semiconductor devices to be tested. The apparatus also includes at least one loader for loading the plural test trays
20 onto the rails and at least one unloader for unloading the test trays from the rails.

Furthermore, the apparatus comprises at least one chamber where the rails traverse. The test trays are provided in the chambers along the rails, so that the plurality of semiconductor devices contained in the test trays may be subjected to a test or/and burn-in process. In addition, a plurality of test heads are formed in the chambers so that each test head is
25 electrically connected to a respective one of the test trays, thereby the test or/and burn-in

- 6 -

process for the semiconductor devices can be performed

The apparatus may further include at least one main frame which includes a control unit electrically connected to a plurality of test heads, and the main frame may further include a coolant refrigerator unit for cooling down the test head. The number of the test heads is preferably four or eight, each of which may perform the test or/and burn-in process for sixty-four semiconductor devices in a single test tray. Preferably, devices to be tested are semiconductor chip packages with gull-wing leads, or chip scaled packages.

According to an alternate aspect of the present invention, an in-line system is provided for semiconductor devices. This in-line system includes a plurality of test and burn-in apparatuses, transferring equipment, and a sorting unit. Each test and burn-in apparatus performs a different test or/and burn-in process from the other. An apparatus includes at least one rail for transferring plural test trays for holding a plurality of semiconductor devices; at least one loader for loading the plural test trays to the rail; at least one unloader for unloading the test trays from the rail; at least one chamber through which the rail lies, whereby the test trays travel in the chambers along the rails, and the plurality of semiconductor devices contained in the test trays are subjected to the test or/and burn-in process; and a plurality of test heads formed in the chambers, such that each of the test heads corresponds to and are electrically connected to a respective one of the test trays in the chambers, where the test or/and burn-in process for the semiconductor devices is performed. The equipment for transferring the test trays from the one apparatus to another, includes the transferring equipment which receives the test trays from the unloader of the apparatus and supplies them to the loader of the apparatus, whereby the apparatuses are linked in-line by the transferring gear. The semiconductor devices which pass all tests and burn-in processes in the apparatuses are transferred to device trays from the test trays in the sorting unit

Each test and burn-in apparatus in the in-line system further includes at least one main frame which includes a control unit electrically connected to the test heads. Every control

- 7 -

unit of each apparatus and the sorting unit may be electrically connected to each other. The main frames may further include a coolant refrigerator unit for cooling down the test heads. In the in-line system, preferably, it has four or eight test heads, each of which may perform the test or/and burn-in process for sixty-four semiconductor devices in the one test tray. The devices are preferably semiconductor chip packages with gull-wing leads.

In particular, the in-line system includes a first apparatus performing a DC test and burn-in, a second apparatus performing a room/cold test, and a third apparatus performing a hot sort test. Moreover, the sorting unit may preferably perform two operations, one of which is to move the devices, which have been tested already, from the test tray to the device trays, while the other is to provide new devices, which have not tested yet, from new device trays to the test tray.

According to still another aspect of the present invention, a method is provided for testing semiconductor devices. This method includes: a step of providing plural test trays to a first test and burn-in apparatus, each of the test trays containing the semiconductor devices; a first step of testing the semiconductor devices contained in the test trays in the first test and burn-in apparatus, a step of transferring the test trays from the first apparatus to a second test and burn-in apparatus; a second step of testing the semiconductor devices contained in the test trays in the second apparatus; a step of transferring the test trays from the second apparatus to a third test and burn-in apparatus; a third step of testing the semiconductor devices contained in the test trays in the third apparatus; a step of transferring the test trays from the third apparatus to a sorting unit; and a step of sorting the semiconductor devices contained in the test trays to device trays.

The above-described test and burn-in apparatus and the in-line system preferably can be employed for this method, each apparatus performing the three testing steps. Each of the transferring steps may be conducted by a transferring equipment which receives the test trays from the unloader of the apparatus and supplies to the loader of the apparatus, so that all

- 8 -

apparatuses can be linked to in-line transferring equipment.

In the method, each apparatus may further include at least one main frame which includes a control unit electrically connected to the test heads, and the control units may be electrically connected to each other and to a unit where the sorting step for the devices in the test trays is conducted. In particular, the processing for the sorting step is preferably based on maps which are recorded as a result of the three testing steps which are then transmitted to the sorting step via the control units.

In addition, the method may further comprise a step of loading new semiconductor devices contained in another device trays to the test trays in which the devices have been sorted, and then again providing the test trays to the first test and burn-in apparatus for the start of testing of new semiconductor devices. Alternating, the three steps of first, second and third testing may include a burn-in step, a room/cold test step and a hot sort test step. The third testing step preferably is the hot sort test step.

Brief Description of the Drawings

FIG. 1 is a flow chart illustrating a conventional overall back-end process for semiconductor devices.

FIG. 2 is a perspective view of a test tray which may be used in accordance with this invention.

FIG. 3 is an exploded view of an insert of the test tray shown in FIG. 2

FIG. 4 is a schematic view of one embodiment of a test and burn-in apparatus in accordance with the present invention.

FIG. 5 is a schematic view of an in-line system in accordance with the present invention, employing the apparatus shown in FIG. 4.

FIG. 6 is a flow chart illustrating an overall back-end process comprising one

- 9 -

embodiment of a test process, using the in-line system of FIG 5, in accordance with the present invention.

FIG. 7 is a view illustrating test tray maps employed in the test process of the present invention.

5 FIG. 8 is a schematic view of another embodiment of the test and burn-in apparatus in accordance with the present invention.

FIG. 9 is a schematic view of another in-line system employing the apparatus shown in FIG. 8.

Detailed Description of the Present Invention

10 The present invention will now be described more fully below with reference to accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth in this description; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the
15 scope of the invention to those skilled in the art. In the drawings, like numbers refer to like elements throughout.

Various tests required for the semiconductor devices are performed by using one or more testing apparatus in accordance with the present invention. In particular, the testing apparatus of the present invention enables burn-in as well as typical tests such as DC test,
20 room/cold test, and hot sort test. Thus, such apparatus of the invention will be referred as a test and burn-in (TABI) apparatus below.

FIG. 2 is a perspective view of a test tray 10; and FIG. 3 is an exploded view of an insert 12 of the test tray 10 shown in FIG. 2. Referring to FIGS 2 and 3, the test tray 10 includes a plurality of inserts 12 provided with a tray frame 14. FIG. 2 illustrates the half

- 10 -

portion of the test tray 10 which has sixty-four inserts 12. Although the test tray 10 having sixty-four inserts 12 is preferably used for the present invention, other trays, such as those having one hundred twenty-eight or five hundred twelve inserts can be alternatively used as will be apparent to those skilled in the art. Each insert 12 which is fixed (removably or permanently) to the tray frame 14 by fasteners 11 accommodates the one semiconductor device. The test tray 10 depicted in FIG. 2 is preferably applied to carrying of semiconductor chip packages with gull-wing leads such as, for example, QFP(quad flat package) or TSOP(thin small outline package). In the meantime, CSP(chip scaled package) such as μ -BGA, which has been recently developed and proposed in the art, can be employed in the test tray 10. The test tray 10 can be designed to hold any type of chip device. Reference numeral 14a in FIG. 2 refers to tray ID holes which are used to generate the tray ID number. The description about this will follow later.

The insert 12 is made of a body 15 and a pushing element 17. The pushing element 17 is elastically joined above the body 15 by springs 18. A pad 13 here, positioned in the center of the body 15 is formed for receiving and supporting the device such as QFP. The pad 13 is connected to the body 15, for example, at its corners, forming four slits 19 at its edges. Four latches 16 corresponding the corners of the pad 13 have hooks 16a, each of which is pivoted at lower end of the latch 16. Pushing the top of the element 17, the latch 16 which is contacted with the bottom surface of the element 17 moves down and the hook 16a rotates upwardly. Therefore, the insert 12 can receive the device on the pad 13. After the device is positioned, the element 17 and the latches 16 reverse by the springs 18 being free of a pushing force, and at the same time the hooks 16a rotate downwardly again so that the device on the pad 13 can be secured by the hooks 16a. Furthermore, the leads of the device are exposed downwardly through the slit 19, so that the device can be tested by contact between its leads and tester.

FIG. 4 is a schematic view of one embodiment of the test and burn-in (TABI)

- 11 -

apparatus 100 in accordance with the present invention. FIG. 4 shows for easy of description and illustration, the test and burn-in apparatus 100. As shown in FIG. 4, the TABI apparatus 100 includes a rail 38 for transferring plural test trays 10. Each test tray 10 contains a plurality of semiconductor devices to be tested. The TABI apparatus 100 further includes a loader 34 and unloader 36 which are located, respectively, at both ends of the rail 38. The trays 10a holding devices to be tested are loaded onto the rail 38 by the loader 34, and the trays 10b of tested devices are unloaded from the rail 38 by the unloader 36. A chamber 32 is provided to at least partially enclose the traversing rail 38, and four test heads 23 are formed in the chamber 32. When four trays 10 are supplied to the test heads 23 one by one along the rail 38, all devices in every tray are subjected to a test or/and burn-in process, being electrically connected to the test heads 23 in the chamber 32. The chamber 32 applies heat or cooling to the test heads 23 for a proper test and burn-in temperature.

The test heads 23 are connected to a main frame 21 which includes a control unit 25, a coolant refrigerator unit 27 and a power source 29. The control unit 25 controls the function and sequence of the testing operation of the test heads 23, and the power source 29 supplies electrical power to the test heads 23. The control unit 25 and the power source 29 are electrically connected to the test heads 23 via cables 24. The coolant refrigerator unit 27 is connected to the test heads 23 by hoses 26 to supply chilled water for cooling down the test heads 23 (particularly a high speed board). Reference numeral 40 in FIG. 4 designates a transferring member such as a cart which receives one or more test trays 10 from the unloader 36, or supplies them to the loader 34.

The TABI apparatus 100 permits the test of two hundred fifty-six devices at a time since the apparatus 100 has four test heads 23, each of which, corresponding to one test tray 10, holding sixty-four devices. However, the apparatus 100 can test much more or less devices at a time by modifying the number of the test heads 23 and/or the number of devices per tray. While the TABI apparatus 100 of this embodiment has one main frame 21 and one

- 12 -

chamber 32, other configurations are also possible, for example, two main frames and two chambers, or one main frame and two chambers.

The TABI apparatus 100 of this embodiment operates as follows. First of all, the test trays 10a holding devices to be tested are loaded in turn to the rail 38 from the transferring member 40 by the loader 34. And then, each tray 10a moves along the rail 38 and stands on each test head 23. Thereafter, the test or/and burn-in process is performed in the chamber 32 when the devices in the trays 10 and the contact parts in the test head 23 are electrically connected to each other. The trays 10b of tested devices move again toward the unloader 36 along the rail 38 and then transferred to next process, being unloaded with the transferring members 40.

As described so far, to depend on the test trays alone, without transferring the devices to and from prior device trays, is one of specific features of the TABI apparatus of the invention. Furthermore, the absence of prior device trays results in less space which the apparatus occupies (that is, the space is as reduced as the prior handler occupied) and less time which it takes to handle the trays. Another feature is that the TABI apparatus of the invention allows burn-in as well as other kinds of electrical tests, being caused by test signals independently transmitted to the devices. These features are also factors that make it possible to realize in-line systems throughout back-end process and to reduce the testing steps. As regarding these, it will be described in detail later.

A case where the TABI apparatus 100 is used for testing under high temperatures such as burn-in or hot sort test, the TABI apparatus 100 of the invention may further include a pre-heater 35 which applies heat to the devices that are being loaded to the rail 38 by the loader 34. On the other hand, the apparatus 100 may further include a pre-cooler 37 for low temperature test. The pre-heater 35 and the pre-cooler 37 can be alternately located in each test head 23.

In particular, the TABI apparatus 100 in accordance with the present invention can

- 13 -

employ the well-known tester made by the Schlumberger Co. The tester is basically equipped to accommodate four test heads, and able to allow sixty-four parallel fan-out in each pin slice board, i.e., a set of timing boards. Therefore, it is possible to perform the test and/or burn-in process of two hundred fifty-six devices at the same time. Meanwhile, the algorithmic
5 pattern generator integrated circuit (APGIC) has been developed for attaining the test rate in 200MHz level, and a high speed timing module with overall timing accuracy has been also developed. Moreover, the capability of the simultaneous parallel test increases to two hundred fifty-six parallel from sixty-four parallel. Accordingly, one may expect an increase in the number of the devices which are tested at once in single test and burn-in apparatus.

10 A plurality of TABI apparatuses of the invention may form the in-line system 200, as illustrated in FIG. 5. FIG. 5 depicts the in-line system 200 in an overall back-end station. As seen from FIG. 5, the in-line system 200 is composed of three TABI apparatuses 100a, 100b and 100c, and only one sorting unit 51. Each TABI apparatus 100a, 100b or 100c is substantially the same apparatus as shown in FIG. 4, however each apparatus 100a, 100b or
15 100c in the in-line system 200 performs a different testing process, respectively and independently. The sorting unit 51 provides the stage where the devices in each test tray 10b are sorted to a separate device tray 60b according to test results. The in-line system 200 can cover the other units in the back-end station such as a marking unit 52 and a visual inspection unit 53, due to the similar UPH (unit per hour) among them. These units 51, 52 and 53 can
20 be preferably provided with one machine 50 as shown in FIG. 5.

The in-line system 200 further includes at least one transferring member 40 such as a cart, a transfer rail, a conveyer belt, or an automated guide vehicle (AGV) which is well known in the art. The transferring member 40 receives one or more test trays 10 from one apparatus or supplies to another apparatus, whereby plural apparatuses are linked as in-line
25 by the transaction of the transferring member 40. The prior device trays are therefore not required since the test trays 10 are directly transferred by the member 40. The in-line system

- 14 -

may have the configuration shown in FIG. 5, however other configurations can be alternatively adapted. For instance, all apparatuses can stand in a row.

Three TABI apparatuses 100a, 100b and 100c of the in-line system 200 perform different test steps; for example, a DC test and burn-in, a room/cold test, and a hot sort test.

5 Although any apparatus can perform any test step, it is preferable to proceed in order as follows: the DC test and burn-in, the room/cold test, and the hot sort test. Other sequences are also possible, for example, the room/cold test in the first place, the DC test and burn-in the second place, and the hot sort test finally. Even the final burn-in is possible, provided the same test items as the room/cold test or the hot sort test are tested in the burn-in step. The
10 test results or information obtained from each individual and different test step are sent to a host computer 45 through network and transmitted to the sorting unit 51. Test tray maps 120 illustrated in FIG. 7 are the form of computer file which enables every test result or information to be recorded, stored and transmitted, and thus they may be referred as link-chained test tray maps. The description regarding the map will follow later.

15 After the devices pass all tests and burn-in processes, the sorting unit 51 proceeds off-line sorting while all test devices on the test tray 10b move to device trays 60b, so that all devices can be sorted to the respective device trays 60b. The sort is done according to the test results or information recorded in the maps. The sorting unit 51 can perform two operations contrary to each other. One is to move the devices, which have tested already,
20 from the test tray 10b to the device trays 60b, that is to say, the above-described sort. The other is to provide new devices, which have not tested yet, from new device trays 60a to the test tray 10a. In FIG. 5, dotted arrows in the sorting unit 51 represent the movement of the devices. Meanwhile, the device tray 60b is supplied to the marking unit 52 by a conveyer belt, a transfer rail, or other transport member, while the test tray 10a is supplied to the first
25 TABI apparatus 100a by the transferring member 40. In the present invention, the loading/unloading of the devices between two trays is done only at the sorting unit 51,

- 15 -

contrary to the prior art in which loading/unloading is performed at every tester.

Although the sorting unit 51 is illustrated as single unit in FIG. 5, two or more sorting units can be selectively adapted for adjusting throughput to the TABI apparatus

Furthermore, the loading of new devices can be alternatively done in another place separate from the sorting unit 51. The separation of sorting and loading is more preferable in case of large sized lot having a great number of devices.

One of several advantages of the in-line system 200 is to save time to raise or drop testing temperature. Also, the in-line system 200 can save time in sorting the devices since the prior sort steps can be reduced to the one. Besides, the reduction of the number of processes and the automation of the overall test process may not only eliminate the possibility of damage during management of the devices, but also prevent problems associated with electrostatic discharge (ESD) caused when workers or equipment come into contact with devices.

FIG. 6 shows a flow chart which illustrates an overall back-end process 70 including one embodiment of test process using the in-line system 200 of FIG. 5. With reference to FIG. 5 again, as well as FIG. 6, the devices which have been already assembled and are ready to be tested, are provided to the back-end station at step 79 by being loaded with the test trays. Then, the first TABI apparatus 100a performs the DC test and burn-in step 71 for the devices 79. In succession, the room/cold test at step 72 and the hot sort test at step 73 are continued by the second apparatus 100b and the third apparatus 100c, respectively, with the devices 79 contained in the test trays 10.

When each test step 71, 72 and 73 is done, the test trays 10 are transferred to next test step 72 or 73, or sort step 74 by the transferring member 40. Reference numeral 61, 62 and 63 in FIG. 6 represent the transfer pathway of the test trays 10. That is, the transferring member 40 receives the test trays 10 from the unloader of the apparatus 100a, 100b or 100c and then supplies to the loader of the next apparatus.

- 16 -

Meanwhile, all control units 21a, 21b and 21c of every apparatus 100a, 100b or 100c are electrically connected to each other and to the sorting unit 51 by the host computer 45 through a network, so that the test results or information can be transmitted to the sorting unit 51 from every apparatus via each control unit. As previously described, the test results or information produced at every test step 71, 72 or 73 have been recorded on the maps 120 in FIG. 7. Therefore, the sort step 74 of all devices can be carried out according to the maps, namely all devices in the test trays 10b are shifted to device trays 60b.

After the sort step 74, empty test trays 10a on the sorting unit 51 receive new devices (i.e., new lot) contained in another device trays 60a, and are then provided to the DC test and burn-in step 71 again for the start of new lot. To the contrary, the device trays 60b receiving the devices are provided to a marking step 75 in FIG. 6 or the marking unit 52 in FIG 5. The former operation is indicated by solid line 64 in FIG. 6, while the latter operation is indicated by dotted line 65. For the arrows in FIG. 6, all of which represent transferences of two kinds of the trays, solid arrows indicate the movement of the test trays 10, 10a or 10b, while dotted arrows indicate that of the device trays 60a or 60b.

One of the reasons why the invented process can proceed successively and directly, namely, as an in-line process and why the invented single composite sort step can be possible, is that device trays are not required to the invented test process itself except for the test trays. Another reason is data automation using the link-chained test tray maps feature of this invention. Referring to FIG. 7 which illustrates a group of maps 120; subgroups of maps 122 and 124 employed in the test process of the present invention, the test results or information obtained from every test step are transmitted to the host computer via each control unit of the apparatuses, and then recorded to the maps 120.

Normal generation and assignment of these maps 120 start to input a lot ID number and to sense the tray ID holes 14a or bar code of the test tray 10 of FIG 2. The tray ID holes, each of which is punched or not respectively, are converted into a decimal tray ID

number by the computer. For example, twelve holes from per tray can represent the decimal tray ID number from 0000 to 4095. Once the tray ID number is recognized, the computer generates the tray map and a map file name. The map file name comes from the combination of the tray ID number and the lot ID number. When the device is loaded into test tray, the blank test tray is supposed to receive the lot ID by operator with the prescribed tray ID by the hole or bar code. Therefore, although same test tray is repeatedly used for different lot, every map file is distinguished from the others by different lot ID number. Examples of the map file name in relation to the tray ID holes are shown in Table 1.

Table 1. Examples of the map file name

Tray ID Holes	Tray ID Number	Lot ID Number	Map File Name
○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○	T0000	Lot123	Lot123.T0000
● ● ● ● ● ● ● ● ● ● ● ● ● ●	T4095	Lot456	Lot456.T4095
○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ●	T0001	Lot100	Lot100.T0001
○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ● ●	T0003	Lot100	Lot100.T0003
○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ● ○	T0002	Lot100	Lot100.T0002

Now return to FIG. 7, when a first map 122 and a second map 124 are created from two test steps, corresponding test results of both maps 122 and 124 are combined and generate final sorting map by a linked algorithm. Therefore, the off-line sorting is proceeded by calling composite test results of the final map. For example, when the room/cold (or ambient) test is performed first and the hot sort test later, each map file is named Lotxxx.TxxxxA, Lotxxx.TxxxxH (here, xxx or xxxx represents lot or tray ID number). And the final composite map file for sorting is named Lotxxx.TyyyS (here, yyy represents the number of test trays in one lot). This can be done in the rework (retest) process in a same manner. The final map file name is associated with a name of retest composite map files

Each of the maps 120, having eight rows and eight columns which form sixty-four

- 18 -

cells, corresponds to the respective one of the test trays in which sixty-four devices are stored. Further, two sheaves of the maps 122 and 124 in the FIG. 7 separately contain the individual test results obtained from two different apparatuses. In this example, one sheaf (or group) of the maps 122 or 124 consists of four individual maps corresponding to four test heads in the single apparatuses. Numerals entered in the map 120 represent corresponding testing results or information. To give a full explanation, 'φ' stands for socket-off, '1~3' for good devices, '4~7' for fail devices, '8' for open/short, and '21' for soft bin device for special customer. All cells formed by any column and any row in the first map 122 will be designated below '(C, R)I', while those in the other second map 124 will be designated '(C, R)II'. Thus, several test results of the single device are recorded at the same position in every map 120. The annotation in parentheses of the second map 124 composes the final sorting map into which the first and the second maps are combined for off-line sorting. In other words, the final map which comes from the first and the second maps can normally be created by link map algorithm by combining two test results.

The sorting step utilizing the maps 120 is carried out by test programs according to the characteristic of the devices. If the numeral of any cell (C, R)I equals that of corresponding cell (C, R)II, the test result of the corresponding device comes to a definite decision to that which the numeral stands for. For example, when both numerals in (3, 5)I and (3, 5)II are '1', the device which is located at third column and fifth row of the test tray is confirmed to the good device. Furthermore, when both numerals in (4, 2)I and (4, 2)II are '8', the corresponding device is opened/shorted and will be then scrapped or retested at both first and second test steps, which stands for 'R₃' in the final map. Similarly, '4' in (5, 3), '5' in (5, 6) and '6' in (8, 3) are also same.

Meanwhile, if the numeral of any cell (C, R)I differs with that of corresponding cell (C, R)II, the corresponding device comes to either a decision to retest, good device, or bin grade down (BGD) well known in the art. For example, when the numeral in (5, 1)I is '5'

- 19 -

which stands for fail of specific item but that in (5, 1)II is '3' which stands for a good device, the device will be retested by the first test as specified 'R₁'. And, when the numeral in (2, 1)I is 'φ' which stands for socket-off while that in (2, 1)II is '2' which stands for a good device, the device will be retested by the first test too. The other way around, if (6, 5)I as a good part becomes fail part in the (6, 5)II as a '8', then it will be retested by the second test which will stand for 'R₂' in the final map. (3, 8) is the same case like 'R₂'. If (1,3)I which is a special fail bin for a specified customer becomes good like '2' of (1,3)II, this part is sorted to good as 'T_{III}' to any customers other than the specified customer. For example, when the numeral in (6, 1)I is '5' but that in (6, 1)II is '2', the device will be sorted as BGD.

Differently from the prior retest process which is repeatedly done on a same tester and handler after sorting in every individual test step, the retest process according to the present invention is done to same failed part after the sorting step. Alternatively, the invented retest process can be done at a time against all kinds of failed devices (i.e., R₁, R₂ and R₃ devices). Failed devices are shifted into the device trays for retest during the sorting step. And, they are loaded into retest trays with previous test result such as R₁, R₂ and R₃ from the separated device trays and then provided again to the invented testing apparatus after testing process of one lot is finished. The retest tray is the same shape as the test tray, preferably with different color for distinction between both. When the retest tray is supplied, the invented test process is repeated for retest regardless of fail type of the devices. Respective retest map files are named Lotxxx.Rxxxx, Lotxxx.RxxxxA, Lotxxx.RxxxxH, and Lotxxx.RzzzS (here, zzz represents the number of retest trays in one lot). Once retest final map file (Lotxxx.RzzzS) is generated, two final map files (Lotxxx.TyyyS and Lotxxx.RzzzS) is automatically combined into cumulative map file (Lotxxx.F***S, here, * equals y plus z) and stored as test data file (Lotxxx.F***F). This test data file contains twice test information including cumulative yield data.

FIG. 8 is a schematic view of another embodiment of the test and burn-in (TABI)

- 20 -

apparatus 300 in accordance with the present invention. As shown in FIG. 8, the TABI apparatus 300 has nearly same structure as the apparatus 100 in FIG. 4. However, differently from the above-described embodiment, the number of the test heads 23 is eight, the main frame 21 is two, and the chamber 32 is two. In addition, the position of both a loader 134 and an unloader 136 also differs from the above-described embodiment, namely, the loader 134 and the unloader 136 are formed at the upper and lower parts at the only end of the rail 38. In FIG. 8, both the loader 134 and the unloader 136 are illustrated side by side, however, they are actually stacked. Therefore, the rail 38 in the chamber 32 is formed as double layers, each layer of which is connected to the loader 134 or the unloader 136. Reference numeral 140 represents the moving direction of the test trays 10a or 10b in the double-layered rail 38. The loader 134 and the unloader 136 may change their positions.

An in-line system 400 which employs the above-described apparatus 300 of FIG. 8 is schematically depicted in FIG. 9. As seen from FIG. 9, the in-line system 400 of the back-end station includes three sub-in-line systems each of which is composed of three TABI apparatuses 300a, 300b and 300c, and the one sorting unit 351 which stand in a row. Test process can be proceeded independently in every sub-in-line system. The in-line system 400 further includes at least one transferring member 40 which goes and returns at the same side of the test apparatuses due to the same position of their loader and unloader. The sorting unit 351 can be composed of double units, as illustrated in FIG. 9. The in-line system of the invention can be maximized through appropriate modification of the configuration of several units including the sorting unit, by adjusting throughput to all apparatuses and units. In FIG. 9, reference numeral 355 and 356 in the sorting unit 351 refer to the unloading part of the tested devices and the loading part of new devices. This has been set forth hereinbefore referring to FIG. 5, so then the description here is omitted.

As previously described, the prior burn-in tester of JEC Co. is not able to perform several test items with a short cycle such as pattern sensitivity, Vcc margin, refresh, or speed

- 21 -

sorting. Therefore, the room/cold test and the hot sort test have been carried out separately from the burn-in. But, the TABI apparatus and the in-line system of the invention permit to perform the room/cold test, the hot sort test, and the burn-in at the same platform. One of the reasons why this improvement is possible is that the test rate of the burn-in step can be improved up to the order of that of the room/cold test or the hot sort test. This improvement also enables an employment of the test trays instead of the burn-in board. In particular, in the case where the present invention uses the tester of the Schlumberger Co., it is possible to perform the testing of test items requiring more short cycle such as a 200MHz test rate and 1ns transition time. Moreover, the present invention can reduce the cycle period in the burn-in as shown in Tables 2 and 3.

Table 2. Information List of Conventional Burn-in

Device	Burn-In Time (hours)	Vcc (V)	Temperature (°C)	Cycle Period (ns)
16M DRAM	2	5.5	125	500
64M DRAM	12	6.3	125	2000
16M Sync DRAM	2	5.5	125	900
64M Sync DRAM	12	5.5	125	900
1M Sync SRAM	2	5.5	125	1000
2M Sync SRAM	2	5.5	125	1000

Table 3. Information List of Invented Burn-in

Device	Burn-In Time (sec)	Vcc (V)	Temperature (°C)	Cycle Period (ns)	The Rate of Reduction
16M DRAM	600	5.5	125	90	1/5.5
64M DRAM	360	6.3	125	90	1/22
16M Sync DRAM	240	5.5	125	30	1/30

- 22 -

64M Sync DRAM	1440	5.5	125	30	1/30
1M Sync SRAM	72	5.5	125	10	1/100
2M Sync SRAM	72	5.5	125	10	1/100

Tables 2 and 3 set forth only burn-in time itself at 125°C. Accordingly, if incidental time such as the time taking in the sorting step is also considered, the actual process time of the conventional burn-in of Table 2 will be much longer. Contrary to this, the actual process time of the invented burn-in of Table 3 does not increase so much since there is not a separate sorting step.

As described so far, the apparatus, the system and the method according to the present invention result in excellent outcome in the overall back-end process for the semiconductor devices, namely: an apparatus and system occupying less space, a short turn around time (TAT), a reduction of transaction and movement, a low test cost and handler cost, a high yield and quality, less man-power for maintenance and operator, the removal of human error, improvement of work in process (WIP), part-to-part corresponding failure analysis by data tracking and comparisons, accurate data feed back to other divisions, and so on.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

- 23 -

CLAIMS

1. A test and burn-in apparatus, comprising:
a rail for transferring a plurality of test trays, each test tray configured to contain a plurality of semiconductor devices;

a loader for loading the test trays onto the rail;

an unloader for unloading the test trays from the rail;

a chamber through which the rail traverses, so that the semiconductor devices contained in the test trays loaded onto the rail can be subjected to a test and/or burn-in process within the chamber; and

a plurality of test heads associated with the chamber, wherein each test head is electrically connected to a corresponding test tray within the chamber in order to perform the test and/or burn-in process.

2. The test and burn-in apparatus according to claim 1, further comprising:

a main frame comprising a control unit which is capable of being electrically connected to the test heads.

3. The test and burn-in apparatus according to claim 2, wherein the main frame further comprises a coolant refrigerator unit configured to cool down the test heads for the test and/or burn-in process.

4. The test and burn-in apparatus according to claim 1, wherein the number of

- 24 -

said test heads is four.

5. The test and burn-in apparatus according to claim 4, wherein each of said test heads is configured to perform said test or/and burn-in process for sixty-four semiconductor devices in one of said plurality of test trays.

5 6. The test and burn-in apparatus according to claim 1, wherein said semiconductor devices comprise semiconductor chip packages with gull-wing leads, or chip scaled packages.

7. An in-line system comprising:

10 (I) a plurality of test and burn-in apparatuses, said each apparatus configured for performing a different test or/and burn-in process from the other apparatuses, and said each apparatus including respectively:

(I-I) at least one rail being configured for transferring a plurality of test trays, each of said test trays configured for containing a plurality of semiconductor devices;

15 (I-ii) at least one loader being configured for loading said plural test trays to said rail;

(I-iii) at least one unloader being configured for unloading said test trays from said rail;

(I-iv) at least one chamber through which said rail lies, in a manner which provides said chambers along said rail, so that said plurality of semiconductor devices when contained in said test trays said devices are subjected to the test or/and burn-in process;
20 and

(I-v) a plurality of test heads housed in said chambers, wherein each of said test heads corresponds to and is electrically connected to a respective one of said test

- 25 -

trays when said test trays are in said chambers, for a test or/and burn-in process of said semiconductor devices to be performed;

(II) transferring member being configured to transfer said test trays from said one apparatus to another, wherein said transferring member receives said test trays from said unloader and supplies to said loader, whereby said apparatuses are linked as in-line by said transferring member; and

(III) a sorting unit configured to sort said semiconductor devices passing all tests and burn-in processes to device trays from said test trays.

8. The in-line system according to claim 7, wherein each of said test and burn-in apparatuses further comprises at least one main frame including a control unit electrically connected to said test heads.

9. The in-line system according to claim 8, wherein said control units of said apparatuses and said sorting unit are electrically connected to each other.

10. The in-line system according to claim 8, wherein said main frames further include a coolant refrigerator unit configured for cooling down said test heads

11. The in-line system according to claim 7, wherein the number of said test heads included in one of said apparatuses is four.

12. The in-line system according to claim 11, wherein each of said test heads performs the test or/and burn-in process for sixty-four semiconductor devices in one of said plurality of test trays.

- 26 -

13. The in-line system according to claim 7, wherein said semiconductor devices comprise semiconductor chip packages with gull-wing leads, or chip scaled packages.

14. The in-line system according to claim 7, wherein said apparatuses include a first apparatus being configured for performing a DC test and burn-in, a second apparatus
5 being configured for performing a room/cold test, and a third apparatus being configured for performing a hot sort test.

15. The in-line system according to claim 7, wherein said sorting unit is configured to perform a first and a second operation, said first operation being to move the devices, which have been already tested, from the test tray to the device trays, and the second
10 operation being to provide untested devices which have been not tested yet from new device trays to the test tray.

16. The in-line system according to claim 7, wherein said sorting unit is linked to a marking unit and a visual inspection unit for said sorted devices in the device trays.

17. A method for testing semiconductor devices, comprising steps of:
15 (I) providing a plurality of test trays to a first test and burn-in apparatus, each of said test trays containing said semiconductor devices;
(II) first testing said semiconductor devices contained in said test trays in said first test and burn-in apparatus;
(III) automatically transferring said test trays from said first apparatus to a
20 second test and burn-in apparatus;
(IV) second testing said semiconductor devices contained in said test trays in said second apparatus;

- 27 -

(V) automatically transferring said test trays from said second apparatus to a third test and burn-in apparatus,

(VI) third testing said semiconductor devices contained in said test trays in said third apparatus;

5 (VII) automatically transferring said test trays from said third apparatus to a sorting unit; and

(VIII) sorting said semiconductor devices contained in said test trays to device trays.

10 18. The method according to claim 17, wherein each of said three test and burn-in apparatuses performing one of said three steps of testing, includes:

at least one rail being configured for transferring said test trays when said test trays contain said devices;

at least one loader being configured for loading said test trays to said rails;

15 at least one unloader being configured for unloading said test trays from said rails;

at least one chamber through which said rails lie, so that said test trays when positioned on said rail are provided to said chambers, so that said devices when contained in said test trays are subjected to one step of said three testing steps; and

20 a plurality of test heads housed in said chambers, wherein each of said test heads corresponds to and is configured to be electrically connected to a respective one of said test trays in said chambers, performing one of said testing steps of said semiconductor devices.

19 The method according to claim 18, wherein each of said three transferring steps is conducted by a transferring member being configured to receive said test trays from

- 28 -

said unloader of said apparatus and supply said test trays to said loader of said apparatus, whereby said apparatuses are in-line linked by said transferring member.

20. The method according to claim 18, wherein each of said test and burn-in apparatuses further comprises at least one main frame including a control unit electrically
5 connected to said test heads.

21. The method according to claim 20, wherein said control units of said apparatuses are electrically connected to each other and to a sorting unit for carrying out said sorting step for said devices in said test trays.

22. The method according to claim 21, wherein said sorting step is based on maps
10 which are recorded in a memory to a host computer as a result of said testing steps and then transmitted to said sorting unit via said control units.

23. The method according to claim 17, further comprising the step of:
loading new semiconductor devices contained in device trays to said test trays,
and then providing said test trays to said first test and burn-in apparatus.

15 24. The method according to claim 17, wherein the first and second testing steps include a burn-in step and, a room/cold test step, respectively.

25. The method according to claim 17, wherein said third testing step is a hot sort test step.

26. The method according to claim 24, wherein said burn-in step further includes

- 29 -

a DC test step.

27. A semiconductor device testing apparatus, comprising:

a host computer;

a plurality of test trays, each of which being configured to hold a plurality of semiconductor devices;

a plurality of test heads configured to make electrical connection with said semiconductor devices when they are held by said test trays, said test heads configured to be in communication with said host computer;

an automated transport member configured to receive said test trays and transport said test trays for alignment with said test heads so that said test heads perform a test on said devices; and

wherein said test heads, upon testing a plurality of semiconductor devices, sends mapping signals to said host computer, said mapping signals providing data for processing the results of said test performed on said devices by said test heads.

28. An apparatus as recited in Claim 27, wherein said host computer is configured to receive said mapping signals and process said data into maps representing the devices in said tray to identify the results of the test performed on said devices by said test head.

29. An apparatus as recited in Claim 28 wherein said test heads are connected to said host computer via a network.

30. An apparatus as recited in Claim 28, wherein each of said test trays has a plurality of holes to identify a tray ID number, so that said tray ID numbers are used to automatically generate file names of said maps.

- 30 -

31. An apparatus as recited in Claim 27, further comprising:
a sorting unit in communication with said host computer, said sorting unit
being configured to receive signals representing a composite map.

32. An apparatus as recited in Claim 31 wherein said apparatus further comprises
5 device trays and wherein said sorting unit is configured to move tested devices, which include
good devices and fail devices, from said test trays to device trays in response to the
composite map.

33. An apparatus as recited in Claim 32 wherein said apparatus further comprises
retest trays and wherein said sorting unit is further configured to move the fail devices from
10 said device trays to said retest trays or to move untested devices from another device trays to
said test trays.

34. An apparatus as recited in Claim 32, further comprising:
a marking unit and a visual inspection unit linked to said sorting unit, wherein
said device trays containing the good devices are transferred to said marking unit and said
15 visual inspection unit.

35. An apparatus as recited in Claim 27 wherein different ones of said plurality of
test heads perform different types of tests.

36. A semiconductor device testing method performed on a semiconductor testing
apparatus including a host computer, a plurality of test trays being configured to hold a
20 plurality of semiconductor devices and a plurality of test heads being configured to make
electrical connection with said semiconductor devices when they are held by one of said test

- 31 -

trays, said test heads being configured to be in communication with said host computer via a network system; said method comprising the steps of:

automatically transporting said plurality of test trays for alignment with said test heads so that said test heads perform a test on said devices; and

5 upon testing a plurality of semiconductor devices, sending mapping signals to said host computer, said mapping signals providing data for processing the results of said test performed on said devices by said test head.

37. A method as recited in Claim 36, further comprising the steps of:

10 said host computer receiving said mapping signals and processing said data into maps representing the devices in the trays to identify the results of the tests performed on said devices by said test heads.

38. A method as recited in Claim 37 wherein each of said test trays has a plurality of holes to identify a tray ID number, and wherein said method further comprises the steps of:

15 recognizing the tray ID number from sensing the holes of each test tray, and generating a file name of each map from the combination of the tray ID number and a lot ID number.

39. A method as recited in Claim 38 wherein said testing step includes different types of tests performed by different ones of said test heads, and wherein said maps representing the different test types are distinguished from the others by different file names
20 having predetermined format.

40. A method as recited in Claim 39 wherein said apparatus further comprises a sorting unit and device trays, and wherein said method further comprises the steps of

- 32 -

said sorting unit receiving signals representing a composite map from said host computer said maps, wherein the composite map is created by automatically combining said maps of different tests;

5 said sorting unit moving said tested devices, which include good devices and fail devices, from said test trays to device trays in response to the composite map.

41. A method as recited in Claim 40, wherein said apparatus further comprises retest trays, and wherein said method further comprises the step of:

 said sorting unit moving the fail devices from said device trays to said retest trays or moving untested devices from said device trays to said retest trays.

10 42 A method as recited in Claim 41, further comprising the steps of:

 automatically transporting said retest trays for alignment with said test heads so that said test heads perform a retest on the fail devices; and

 upon retesting the fail devices, sending mapping signals to said host computer, said mapping signals providing data for processing the results of said retest performed on the
15 fail devices by said test head.