

ABSTRACT

A package substrate includes wirings on a substrate body. Each wiring includes a substrate pad in a bonding finger region of the substrate body and a connected trace extending into a chip mounting region of the substrate body. Plating layers are respectively disposed on the substrate pads. Disposed on the substrate body are first and second residual sections of a first plating inlet line respectively connected to first and second traces. An insulating layer covers the first and second traces and residual sections. The insulating layer includes a first opening through which the first and second plating layers are exposed and includes a second opening separating the first residual section from the second residual section. The first trace includes a recessed section on a side facing the second trace, and the second opening is disposed within the recessed section.

FIG.1