

ABSTRACT

A nonvolatile memory device includes a first cell region, a second cell region and a peripheral circuit region. The first cell region includes first normal bitlines and first redundant bitlines. The second cell region is disposed in a vertical direction above the first cell region and includes second normal bitlines and second redundant bitlines. The peripheral circuit region is disposed in the vertical direction below the first cell region and includes a page buffer circuit and a page buffer decoder. The page buffer circuit includes page buffers connected to the first normal bitlines, the second normal bitlines, the first redundant bitlines and the second redundant bitlines. The page buffer decoder is configured to integrate defective bitlines occurring among the first normal bitlines and the second normal bitlines and replace the defective bitlines with the first redundant bitlines and the second redundant bitlines.

FIG. 1