

HORIZONTAL LINE COUNTER INSENSITIVE TO
LARGE PHASE SHIFTS OF VIDEO

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Field of the Invention

The present invention relates to detection of information that may be present in a video signal during 10 vertical blanking intervals.

Background of the Invention

A video signal typically includes vertical display 15 intervals that comprise a plurality of horizontal line intervals, e.g. 525 lines per vertical interval in NTSC video systems. A portion of each vertical interval is usually designated as a vertical blanking interval. The vertical blanking interval may span a plurality of horizontal line intervals, e.g. in excess of 20 20 horizontal line intervals. The beginning of each vertical and horizontal interval is identified by respective vertical and horizontal sync pulses that are included in a composite video signal.

The content of the video signal during blanking 25 intervals is usually not intended for display as part of the normal video image. The lack of image information in blanking intervals makes it possible to insert auxiliary information, e.g. teletext and closed caption data, into blanking intervals. The standards for each type of auxiliary 30 information specify the positioning of the information within a vertical blanking interval. For example, the present closed captioning standard (see e.g. 47 CFR §§ 15.119 and 73.682) specifies that digital data corresponding to ASCII characters for closed captioning must be in line 21 of vertical blanking.

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An approach to recovery of auxiliary information is to accurately identify a specific line interval, e.g. line 21, containing auxiliary information during a vertical blanking interval by counting horizontal sync pulses. For example, a horizontal line counter could be initialized by a vertical sync pulse and clocked by horizontal sync pulses. Ideally, the count value would then represent the line number.

A video receiver may produce various versions of horizontal and vertical sync signals that might be used to control a line counter. For example, a sync separator may produce sync signals directly from the received composite video signal. FCC requirements specify precise timing limits for composite video signals. These timing limits might suggest that the output of a sync separator would be a reliable source of control signals for a line counter. However, weak signals combined with the occurrence of equalization pulses during vertical blanking may produce an irregular horizontal sync pulse waveform at the sync separator output that is not a reliable source of clock pulses for a line counter. Thus, it may be desirable to use a more regular horizontal sync waveform to clock a line counter. For example, the output of a horizontal phase-locked-loop (PLL) that is typically included in a video receiver for deflection purposes produces a regular pulse waveform at the horizontal line rate. As a result of FCC specifications, the start of data within any horizontal line is accurately timed with respect to the composite video or sync separator output, but not necessarily with respect to the horizontal PLL output. Minor timing shifts do not adversely affect the display of normal video images. However, significant timing errors may be introduced if the operation of the horizontal PLL is disturbed. For example, switching between the dual video read heads in a video cassette recorder (VCR) may produce an abnormal horizontal line period that differs significantly from the nominal 64 μ s period. The deviation in the line period may produce a



perturbation in the horizontal PLL that is manifested as a substantial phase shift between the composite sync signal at the sync separator output and the horizontal pulse waveform at the horizontal PLL output. The locking action of the PLL
5 gradually corrects the perturbation such that the phase error is substantially eliminated before visible display begins. A significant phase shift may exist, however, for many of the line periods within vertical blanking. Thus, the actual beginning of the information in a horizontal line during
10 vertical blanking as indicated by the sync separator output may differ in time from the beginning of the same line as indicated by the output of a horizontal PLL.

The residual phase shift that remains during line intervals within vertical blanking may preclude retrieving
15 auxiliary video data that occurs during line periods within the vertical blanking interval. For example, consider a closed caption decoder that identifies the beginning of closed caption data in line 21 based on the count value from a line counter that is clocked by the output of a horizontal PLL. If the video
20 signal containing closed caption data originates in a VCR, the horizontal PLL error caused by read head switching may cause the line counter to exhibit the value 21 at a time that is not synchronized to the beginning of data in line 21. Thus, the closed caption decoder would be attempting to extract
25 closed caption data from line 21 either before or after line 21 actually begins. Corrupted closed caption data may be produced.

Summary of the Invention

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A horizontal line counter provides a signal identifying the beginning of video data in a particular horizontal video line. The counter is clocked by multiple clock signals. A first clock signal clocks the counter until the line count value
35 equals a known value that is less than the line number of the



horizontal line that is to be identified. When the count value equals the known value, clocking by a second clock signal is enabled. Although the first clock source provides a regular pulse waveform suitable for clocking the counter reliably, 5 transitions of the first clock signal may not accurately indicate the beginning of information within a horizontal line interval. Transitions of the second clock signal accurately indicate the beginning of the desired information. However, the waveform of the second clock signal may exhibit irregularities 10 prior to the time at which clocking by the second clock signal is enabled that could adversely affect the reliability of the counter value. The combined clocking arrangement advantageously provides significantly higher reliability of the count value and improves the timing of the line identification 15 signal with respect to the beginning of the desired video data.

Brief Description of the Drawing

Figure 1 shows in block diagram form an embodiment 20 of the invention.

Figure 2 and 3 show signal waveforms useful for understanding the operation of the embodiment in Figure 1.

Detailed Description of the Drawing

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Figure 1 shows an exemplary embodiment of the invention in a system for decoding closed caption data that occurs during horizontal line 21. In Figure 1, an input video signal VIDEO is coupled to sync separator 100. Sync separator 30 100 produces a vertical sync signal VRT SYNC and a composite sync signal COMP SYNC. Signal VRT SYNC is coupled to horizontal line counter 110 to reset or clear the counter when a vertical sync pulse occurs on signal VRT SYNC. Composite sync signal COMP SYNC is coupled to horizontal phase-locked 35 loop (PLL) 105.



Horizontal PLL 105 generates a horizontal pulse signal HOR PLS that repeats with a period equal to the horizontal line period. Signal HOR PLS is coupled to the clock input of line counter 110. Horizontal PLL 105 also generates a second
5 signal HOR that also has a period equal to the horizontal line period. However, signal HOR exhibits a greater duty cycle, e.g. 50%, than does signal HOR PLS. The timing of signal HOR is such that one transition of pulses on signal HOR is aligned with the opposite transition of pulses on signal HOR PLS. The
10 alignment of opposite transitions on signals HOR and HOR PLS produces a delay between the same transitions on signals HOR and HOR PLS. For example, if signal HOR exhibits approximately a 50% duty cycle and if the falling edges of signal HOR are aligned with the rising edges of signal HOR PLS,
15 a delay of approximately one-half a horizontal line period exists between the rising edges of signal HOR and the rising edges of signal HOR PLS. This delay is used advantageously as described below.

Signal LINE # 20 in Figure 1 is an output of line counter
20 110 that indicates when line 20 is currently being received. Signal LINE # 20 may be generated, for example, when the count value has been incremented in response to clock signal HOR PLS to a value of 20. Signal LINE # 20 is coupled to the "D" input of D-type register 115. The clock input of register
25 115 is coupled to signal HOR. Counter 110 and register 115 are both triggered on the same transition, e.g. rising-edge triggered. The above-described one-half horizontal line period delay between the same polarity transitions of signals HOR PLS and HOR causes register 115 to be clocked one-half
30 horizontal line period after counter 110 is clocked. Thus, register 115 will be clocked after signal LINE # 20 has stabilized to produce at the output of register 115 a signal DLY that is a delayed version of signal LINE # 20. The delay between signals LINE # 20 and DLY is approximately one-half
35 horizontal line period.



The output of register 115 is coupled to the "D" input of register 120. Register 120 is clocked by composite sync signal COMP SYNC from horizontal PLL 105. When horizontal PLL 105 is operated normally, i.e. stable locked state, transitions on signal COMP SYNC are approximately aligned with corresponding transitions on signal HOR PLS causing register 120 to be clocked at approximately the same time as counter 110. The output of register 120 is a signal LINE # 21 that indicates the beginning of line number 21 of a video field where closed caption data is located. Signal LINE # 21 is coupled to closed caption decoder 125 to initiate the extraction of closed caption data from the video signal VIDEO that is also coupled to closed caption decoder 125.

The operation of the above-described circuit is explained below. The following description may be better understood by referring to the signal waveforms shown in Figure 2. For the purposes of the exemplary embodiment in Figure 1 and the waveforms in Figure 2, the registers and counters are assumed to be positive-edge triggered. It will be apparent to one skilled in the art that negative-edge triggered devices may also be used. One skilled in the art will also realize that the embodiment in Figure 1 may be readily adapted to line numbers other than line 21.

Line counter 110 is reset at the beginning of a field by signal VRT SYNC. Line counter 110 increments in response to pulses on signal HOR PLS to indicate the number of pulses or lines that have been received. If a disturbance is introduced into composite sync signal COMP SYNC, horizontal PLL 105 will be perturbed introducing a significant phase shift between subsequent pulses on signal COMP SYNC and pulses on either signal HOR PLS or HOR until horizontal PLL 105 stabilizes. During the time that horizontal PLL 105 is stabilizing, transitions on signal COMP SYNC continue to accurately indicate the beginning of each horizontal line. However, signal COMP SYNC may exhibit irregular pulse



waveforms until the equalizing pulse interval of vertical blanking has been completed, e.g. by line 20. Thus, counter 110 is clocked by the more reliable waveform of signal HOR PLS even though the clocking is time shifted with respect to 5 signal COMP SYNC and the beginning of video in each line. During this time, changing count values at the output of counter 110 do not accurately indicate the beginning horizontal line periods.

When the count value at the output of counter 110 10 reaches 20, signal LINE # 20 transitions to a new state, e.g. from logic 0 to logic 1. The next rising edge of signal HOR (delayed by one-half cycle with respect to the corresponding rising edge of signal HOR PLS) clocks the new value on signal LINE # 20 through register 115 causing a transition on signal 15 DLY. By the time that line 20 has been reached, the transitions on signal COMP SYNC are adequate to clock a register. Thus, the next rising edge of signal COMP SYNC, which corresponds to the beginning of video in line 21, clocks the changed state of signal DLY through register 120 causing a 20 change in the state of signal LINE # 21. The alignment of signal LINE # 21 with the transition on signal COMP SYNC differs by the negligible clock-to-output delay of register 120. Therefore, an accurate indication of the beginning of the video information on line 21 is communicated to closed caption 25 decoder 125 via signal LINE # 21.

Signal LINE # 21 will provide an accurate indication of the beginning of line 21 despite a phase shift between signals HOR PLS and COMP SYNC that may be almost as large as one-half horizontal line period. The phase shift may be such that 30 signal HOR PLS is shifted either before or after signal COMP SYNC by an amount approaching one-half line period without affecting the validity of signal LINE # 21. The flexibility in the relative positioning of signal HOR PLS with respect to signal COMP SYNC is provided by the one-half line period 35 delay introduced by using signal HOR rather than signal HOR



PLS to clock register 115. For example, consider the timing situations shown in Figures 3A and 3B. In Figure 3A, the rising edges of signal HOR PLS are phase shifted prior to corresponding edges of signal COMP SYNC by slightly less than 5 one-half line period. In this case, register 115 is clocked by signal HOR to produce signal DLY (indicating line 20) slightly after the rising edge of signal COMP SYNC. Thus, the next rising edge of signal COMP SYNC (indicating the beginning of line 21) will reliably clock register 120 to generate signal 10 LINE #21. Figure 3B shows rising edges of signal HOR PLS phase shifted after corresponding rising edges of signal COMP SYNC by slightly less than one-half a horizontal line period. In this case, register 115 is clocked by signal HOR to produce signal DLY slightly before the pulse on signal COMP SYN that 15 indicates the beginning of line 21. Thus, signal LINE # 21 transitions in response to the correct pulse on signal COMP SYN. The delay between signals HOR and HOR PLS may be modified to other values less than one-half a horizontal line period by, for example, selecting a duty cycle for signal HOR 20 other than the 50% duty cycle that is described above and shown in Figure 2. In addition to modifying the duty cycle, the circuit shown in Figure 1 should be changed to ensure that the pulse on signal DLY remains symmetrical with respect to the pulse on signal HOR PLS corresponding to line 25 21 as shown in Figures 3A and 3B.

As shown in Figure 1, signals VRT SYNC and HOR PLS may be coupled to deflection circuits if the video receiver includes means for displaying the video information, e.g. a cathode ray tube. However, the invention may also be useful 30 in the context of a video receiver in a VCR where deflection circuits are not present.



CLAIMS

1. In a system for processing a video signal having vertical and horizontal display intervals, each of said
5 vertical display intervals including a plurality of said horizontal display intervals, apparatus comprising:
means for producing a first signal indicative of the occurrence of each of said horizontal display intervals, and a second signal indicative of the beginning of video information
10 during each of said horizontal display intervals;
means for counting including a first input for counting in response to said first signal during a first period of each of predetermined ones of said vertical display intervals, and a second input for counting in response to said
15 second signal during a second period of each of said predetermined ones of said vertical display intervals.
2. Apparatus according to Claim 1, wherein said first period extends from a first one of said
20 horizontal display intervals in each of said predetermined ones of said vertical display intervals to a twentieth one of said horizontal display intervals in each of said predetermined ones of said vertical display intervals.
- 25 3. Apparatus according to Claim 1, wherein desired information is contained in a predetermined horizontal display interval in said predetermined ones of said vertical display intervals, and
said first period extends from a first one of said
30 horizontal display intervals in said predetermined ones of said vertical display intervals to a horizontal display interval penultimate to said predetermined horizontal display interval containing said desired information.





4. Apparatus according to Claim 1, wherein said means for producing said first and second signals comprises a phase locked loop circuit responsive to said video signal for producing said first signal, and a sync separator circuit responsive to said video signal for producing said second signal.

5. In a system for processing a video signal having vertical and horizontal display intervals, each of said vertical display intervals including a plurality of said horizontal display intervals, apparatus comprising:

means for producing a first signal indicative of the occurrence of each of said horizontal display intervals, and a second signal indicative of the beginning of video information during each of said horizontal display intervals;

means responsive to said first signal for counting said horizontal display intervals occurring during each of predetermined ones of said vertical display intervals to produce an output signal indicating when a predetermined one of said horizontal display intervals occurs; and

means for delaying said output signal in response to said second signal to produce a synchronized output signal exhibiting a known timing relationship to the beginning of video information in said predetermined one of said horizontal display intervals.

6. Apparatus according to Claim 5, wherein said means for producing said first and second signals comprises a phase locked loop circuit responsive to said video signal for producing said first signal, and a sync separator circuit responsive to said video signal for producing said second signal.



7. Apparatus according to Claim 5, wherein said delay means comprises a D-type register having a data input for receiving said output signal of said counting means, a clock input for receiving said second signal, 5 and an output for producing said synchronized output signal.

8. A method of synchronizing a control signal to video information in a video signal having vertical and horizontal display intervals, each of said vertical display 10 intervals including a plurality of said horizontal display intervals, comprising the steps of:

producing a first signal indicative of the occurrence of each of said horizontal display intervals, and a second signal indicative of the beginning of said video 15 information during each of said horizontal display intervals; counting said horizontal display intervals occurring during each of said vertical display intervals in response to said first signal to produce an output signal indicating when a predetermined one of said horizontal 20 display intervals occurs; and

delaying said output signal in response to said second signal to produce a synchronized output signal exhibiting a known timing relationship to the beginning of said video information in said predetermined one of said 25 horizontal display intervals.



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