



162162



G00002

ABSTRACT
INDUCTOR-LESS RF/IF CMOS BUFFER FOR 50 Ω OFF-CHIP LOAD DRIVING

A buffer amplifier comprising a source follower-common drain circuit with a feedback path from the output of the drain follower to the input gate of the source follower. The feedback circuit is designed such that the output of the drain follower can be guaranteed to be at a voltage midway between the positive and the negative voltage supply of the circuit. This is the optimum operating point since it allows the largest signal swing. A small transconductance is realized by biasing the transistors of the feedback amplifier with very low currents; preferably by operating them in their weak inversion region. Feedback through the feedback amplifier is only present at DC (direct current) and at very low frequencies. This stabilizes the DC voltage at the drain of the common drain transistor, which, via an output capacitor, is also the output of the buffer amplifier.

(Fig.1 is suggested for publication.)