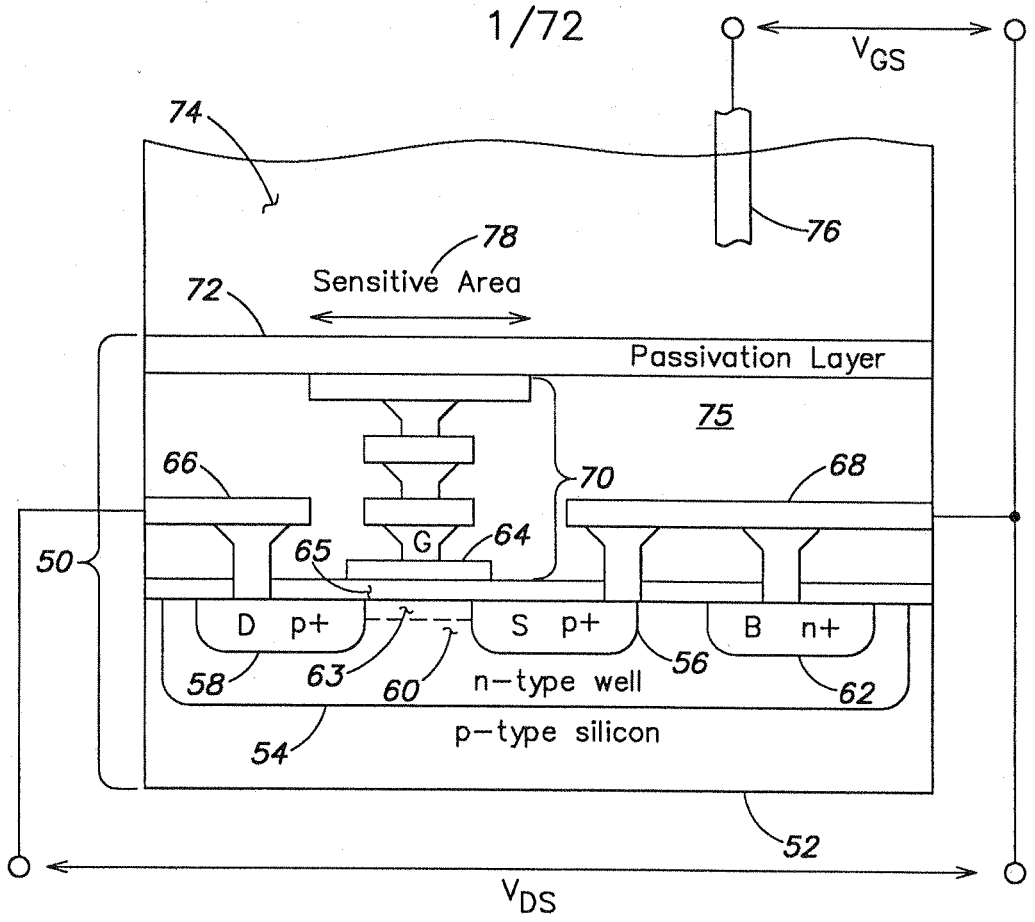

V_{GS}
74
76
78
Sensitive Area
72
Passivation Layer
75
66
70
68
G
64
65
50
D p+
S p+
B n+
58
63
60
56
62
n-type well
p-type silicon
54
52
V_{DS}

FIG. 1

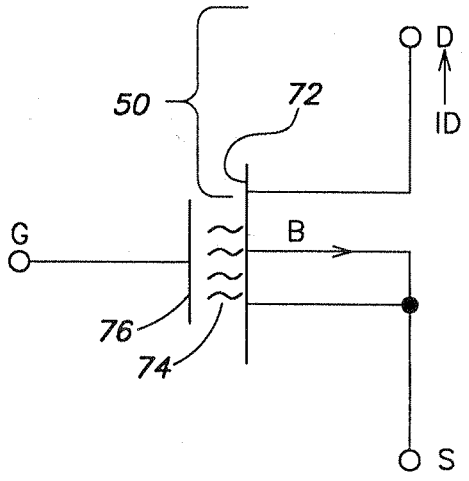

D
ID
50
72
G
B
76
74
S

FIG. 2

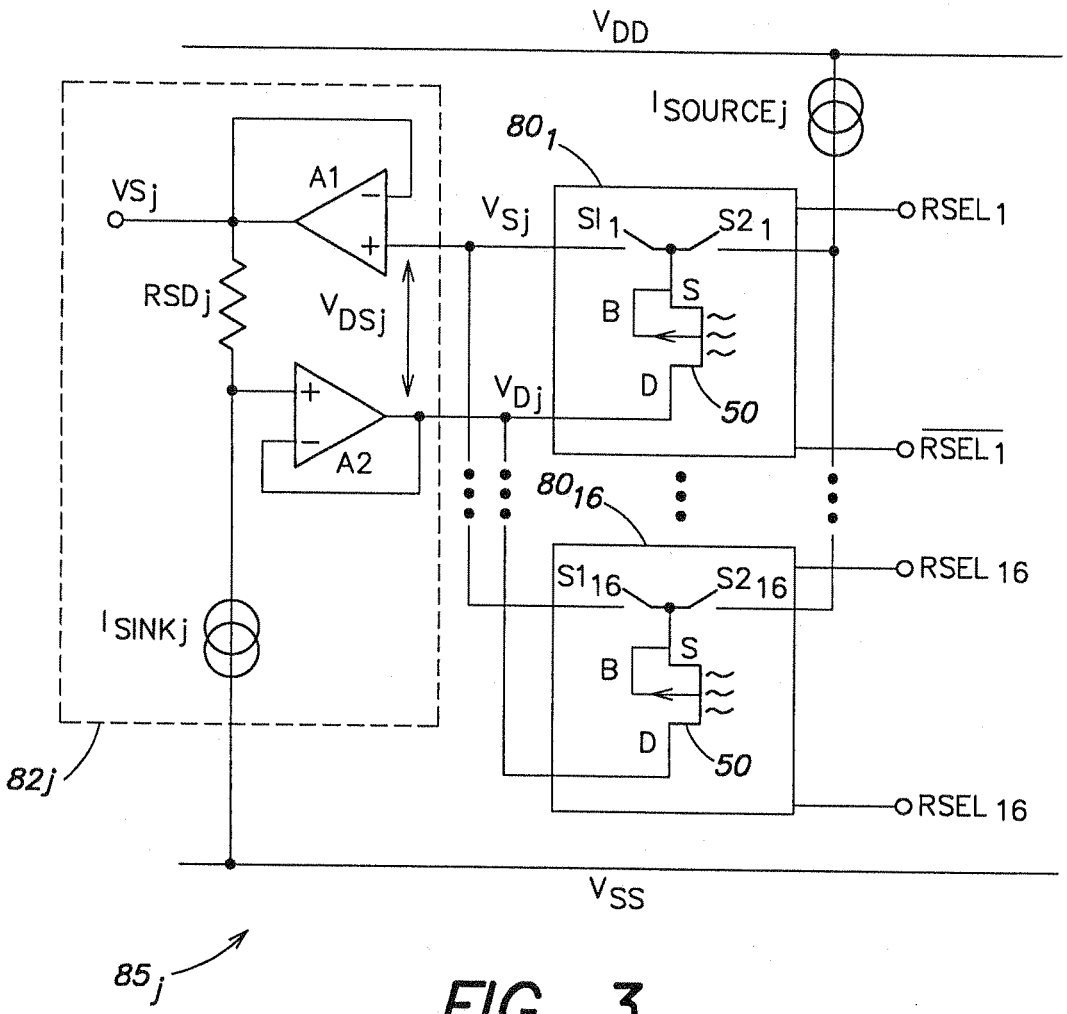

VDD
ISOURCEj
801
VSj
A1
VSj
SI 1
S2 1
RSEL 1
RSDj
VDSj
S
B
D
50
VDj
A2
RSEL 1
8016
S116
S216
RSEL 16
ISINKj
S
B
D
50
RSEL 16
82j
VSS
85j

FIG. 3

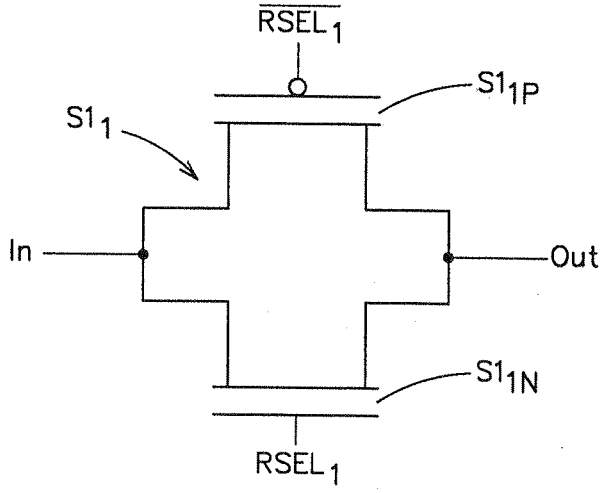

RSEL 1
S11P
S11
In
Out
S11N
RSEL 1

FIG. 4

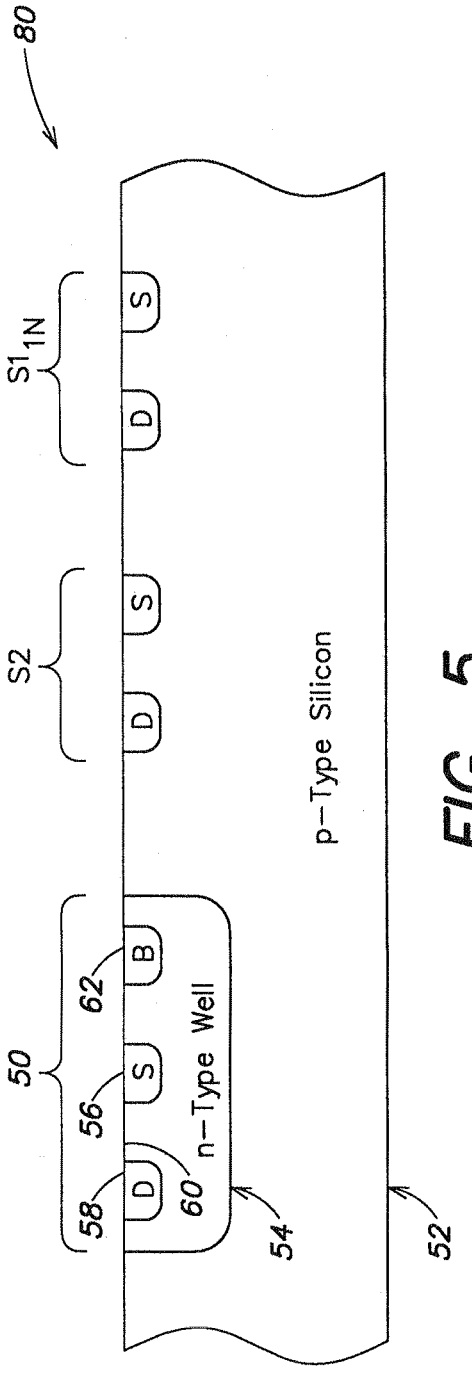

80
S1 1N
S2
50
D
S
B
62
56
58
60
n-Type Well
54
52
p-Type Silicon

FIG. 5

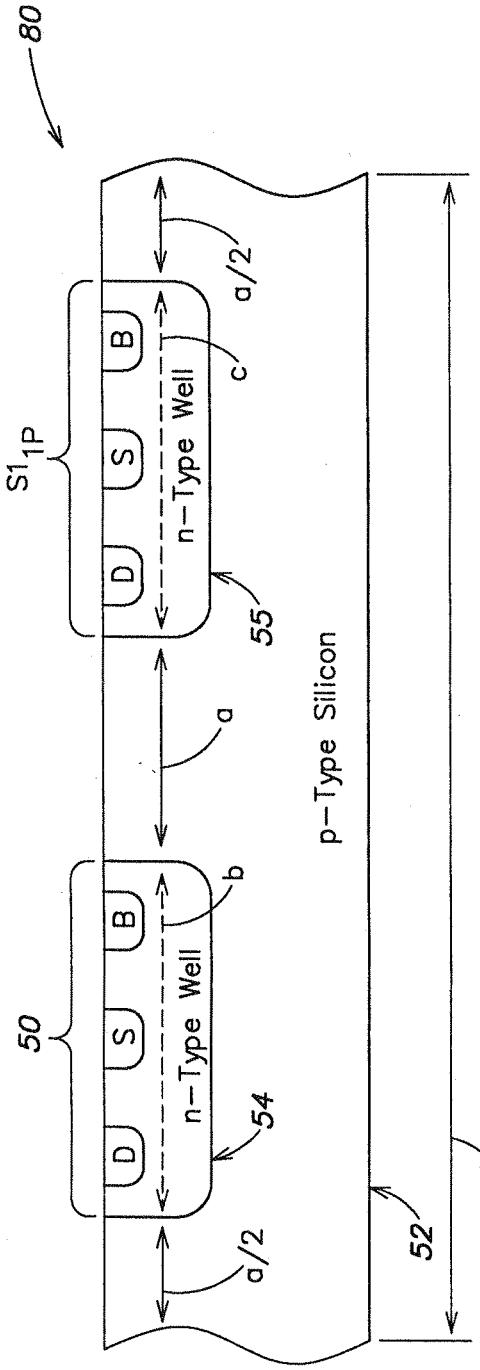

80
S1 1P
50
D
S
B
n-Type Well
a/2
c
55
a
b
54
a/2
52
d
p-Type Silicon

FIG. 6

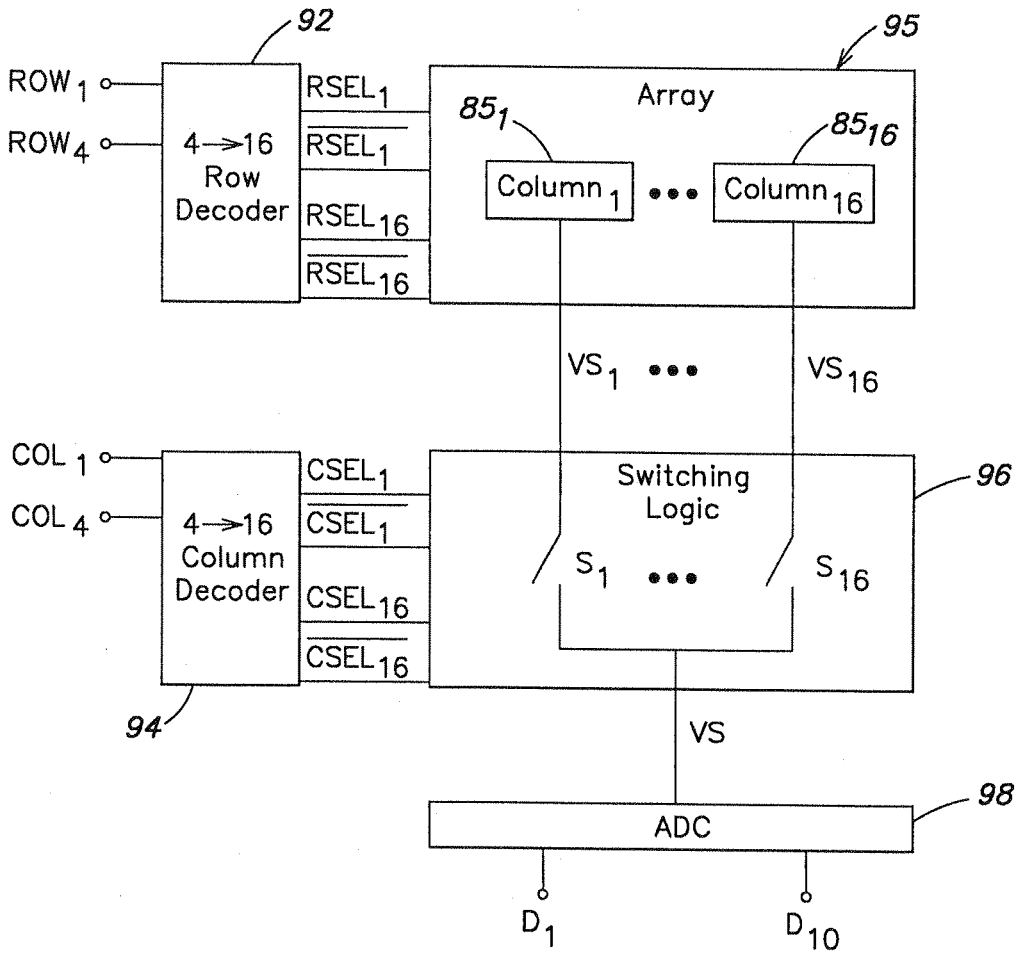

92
95
ROW 1
ROW 4
4→16
Row
Decoder
RSEL1
RSEL1
RSEL16
RSEL16
Array
851
8516
Column 1
Column 16
VS1
VS16
COL 1
COL 4
4→16
Column
Decoder
CSEL1
CSEL1
CSEL16
CSEL16
Switching
Logic
96
S1
S16
94
VS
98
ADC
D1
D10

FIG. 7

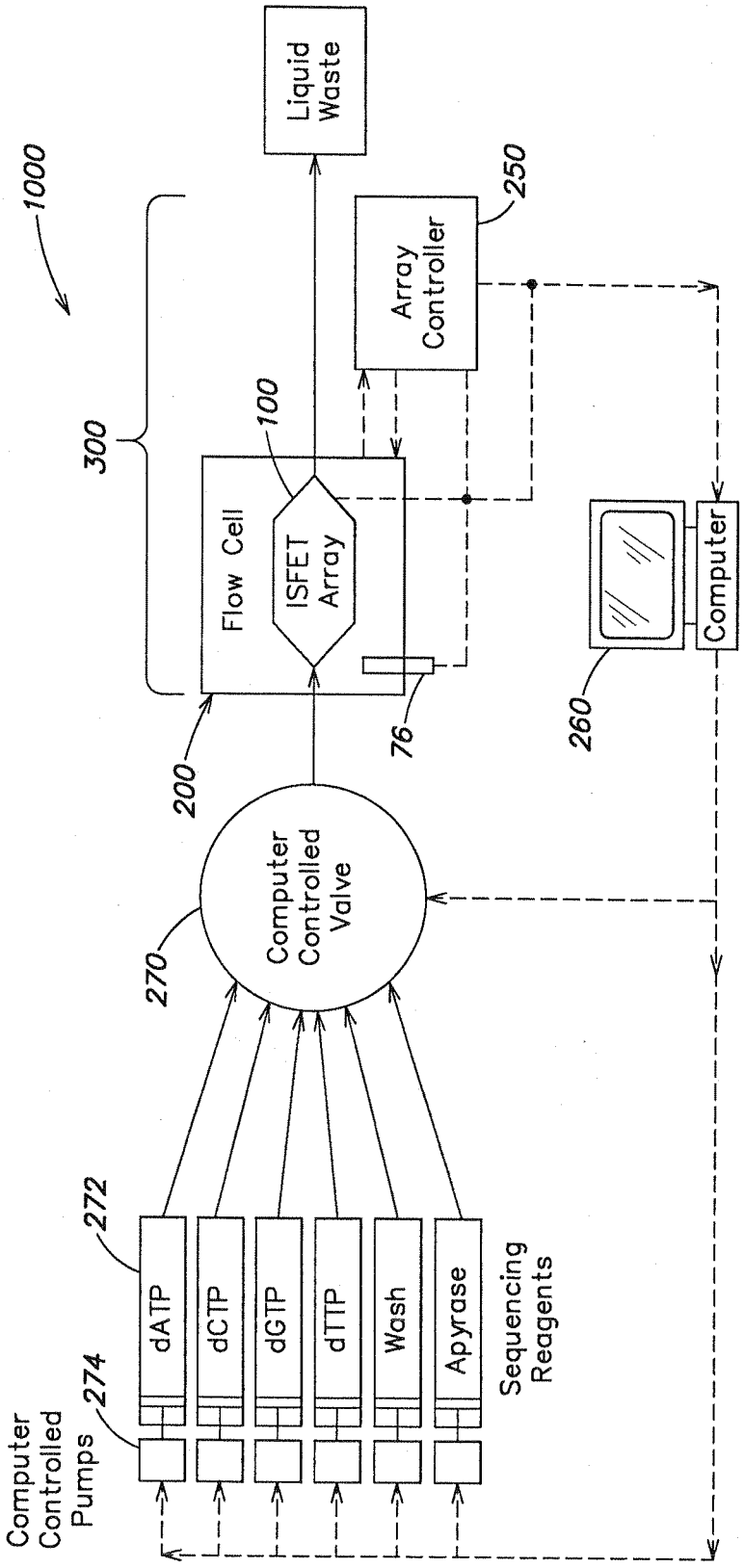

1000
Liquid Waste
250
Array Controller
300
100
Flow Cell
ISFET Array
Computer
260
76
200
Computer Controlled Valve
270
272
dATP
dCTP
dGTP
dTTP
Wash
Apyrase
Sequencing Reagents
274
Computer Controlled Pumps

FIG. 8

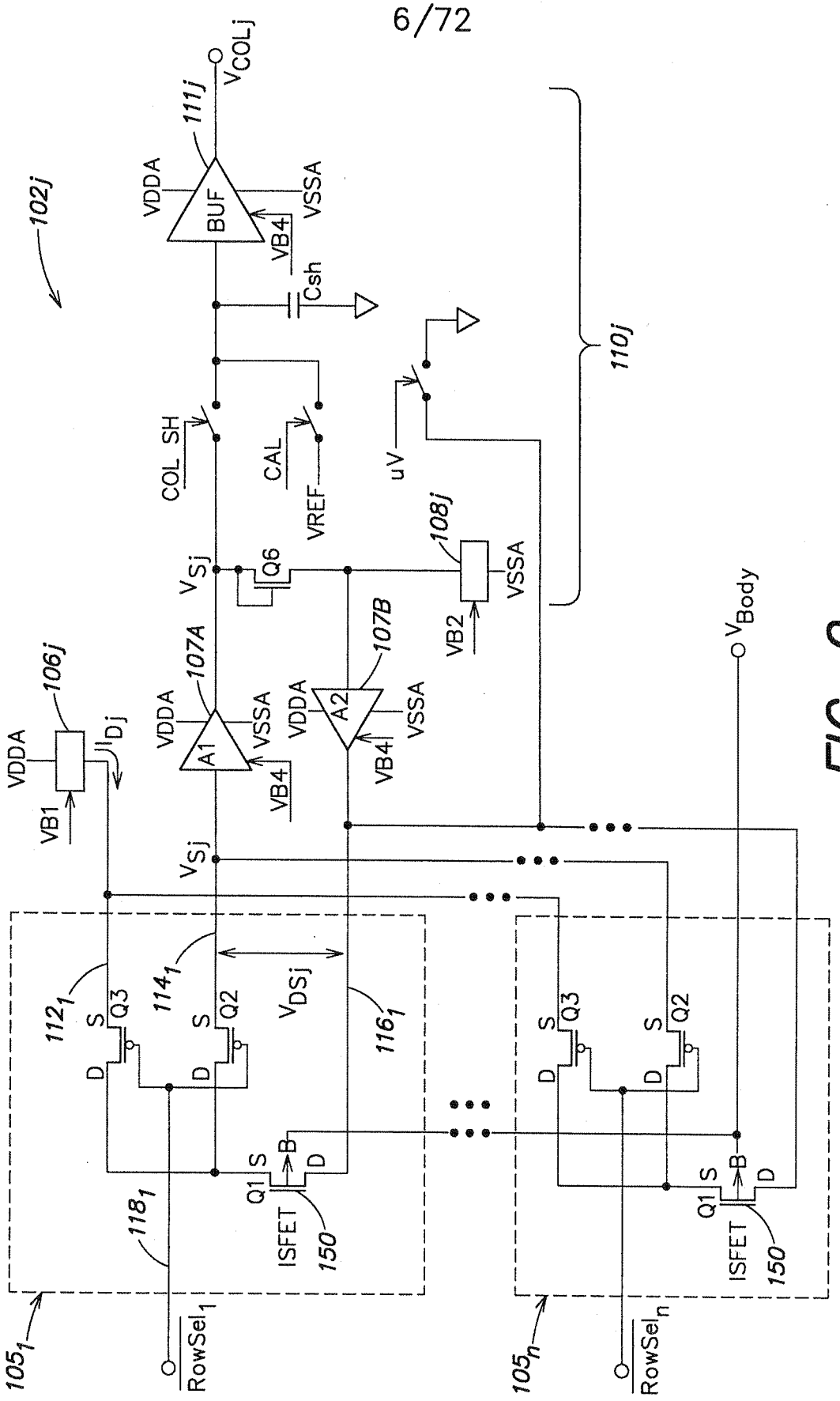

102j
111j
V_{COLj}
VDDA
BUF
VSSA
VB4
Csh
COL SH
CAL
VREF
uV
110j
108j
VB2
VSSA
V_{Sj}
Q6
107A
107B
106j
VDDA
A1
A2
VSSA
VB4
VB1
I_{Dj}
V_{Body}
112_1
114_1
V_{DSj}
116_1
118_1
Q3
Q2
Q1
S
D
B
ISFET
150
105_1
105_n
$\overline{RowSel_1}$
$\overline{RowSel_n}$

FIG. 9

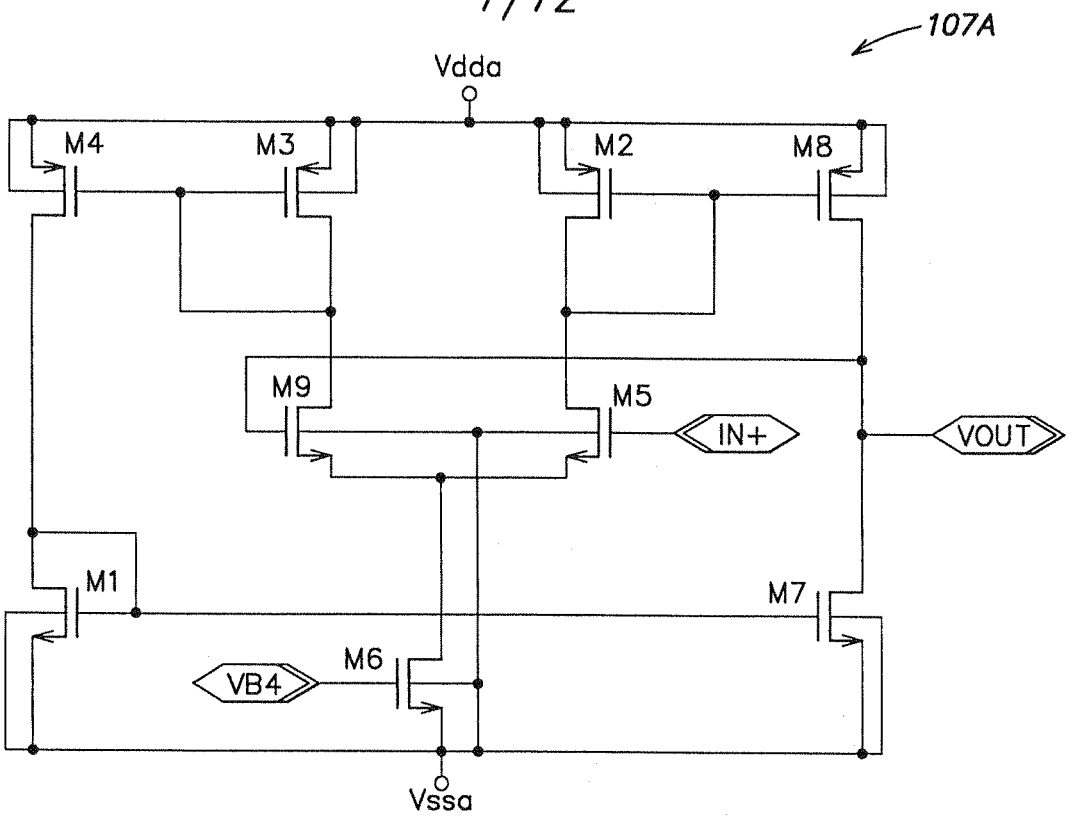

107A
Vdda
M4
M3
M2
M8
M9
M5
IN+
VOUT
M1
M7
M6
VB4
Vssa

FIG. 9A

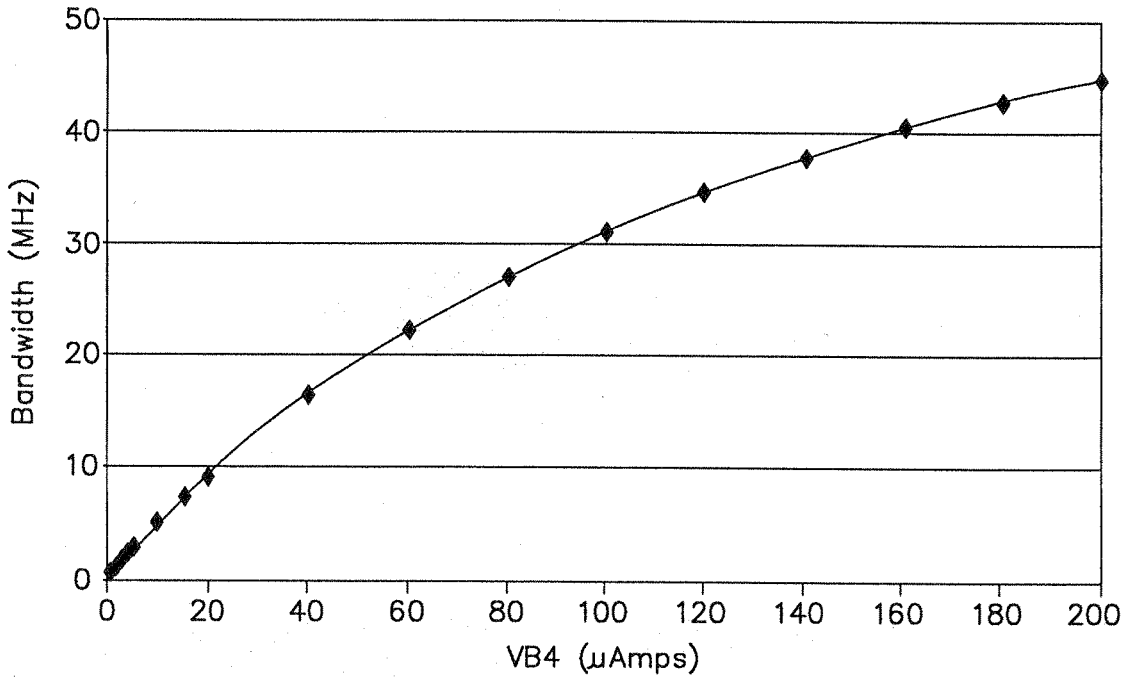

Bandwidth (MHz)
50
40
30
20
10
0
0
20
40
60
80
100
120
140
160
180
200
VB4 (μAmps)

FIG. 9B

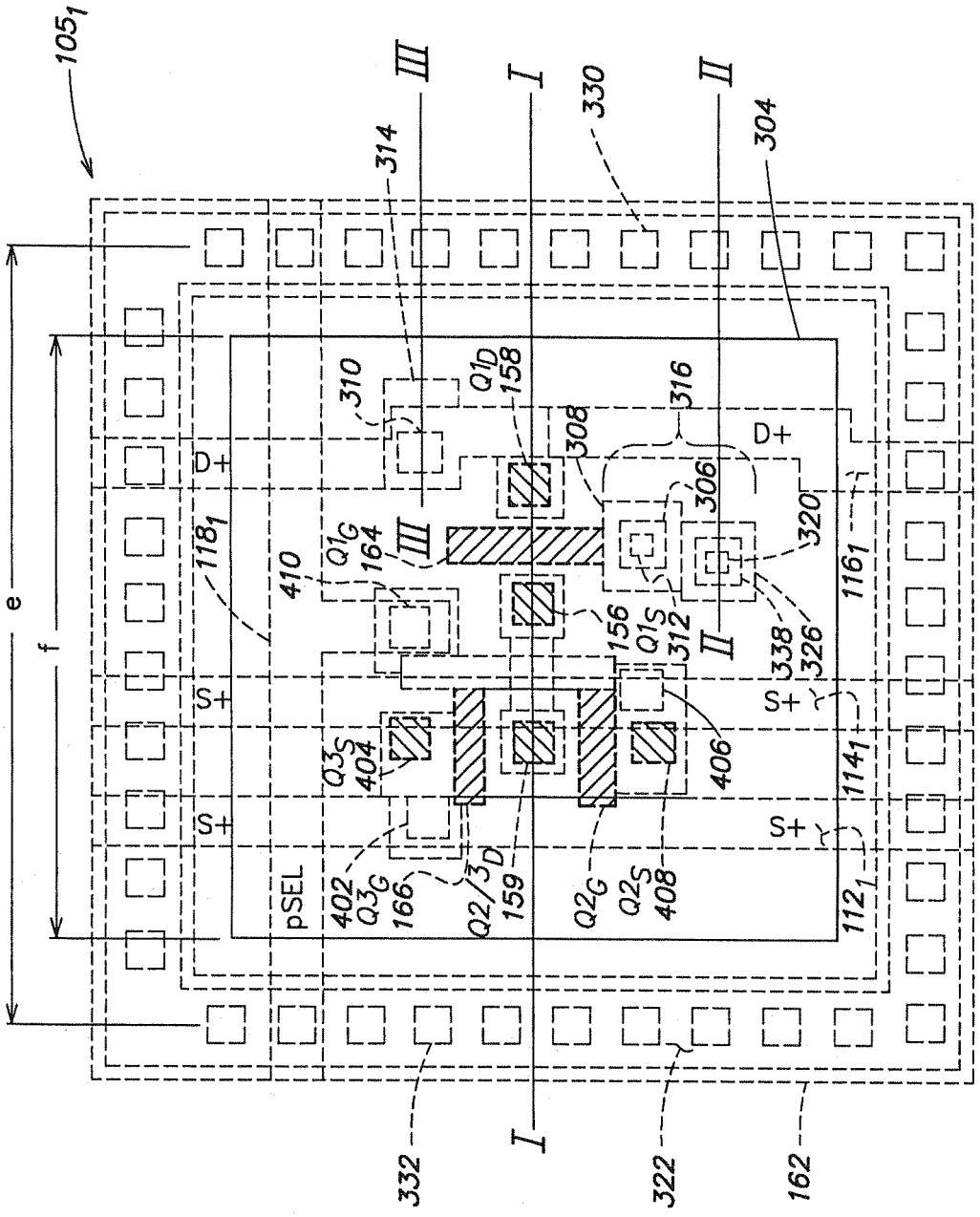

105₁
III
I
330
II
304
314
310
Q1D
158
316
308
D+
306
320
Q1G
164
III
410
118₁
156
Q1S
312
II
338
326
1161
S+
Q3S
404
406
1141
pSEL
402
Q3G
166
Q2/3D
159
Q2G
Q2S
408
112₁
e
f
332
I
322
162

FIG. 10

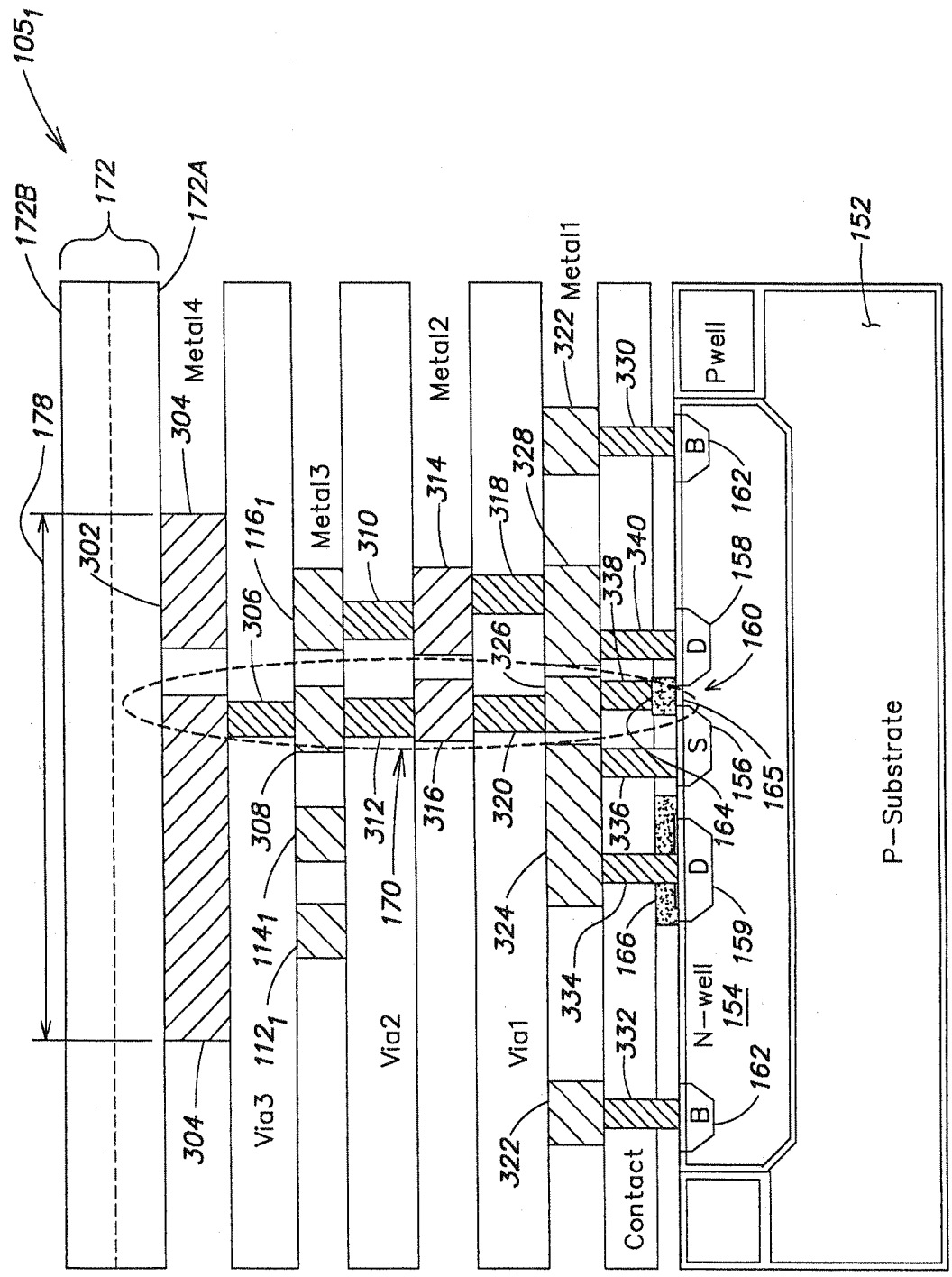
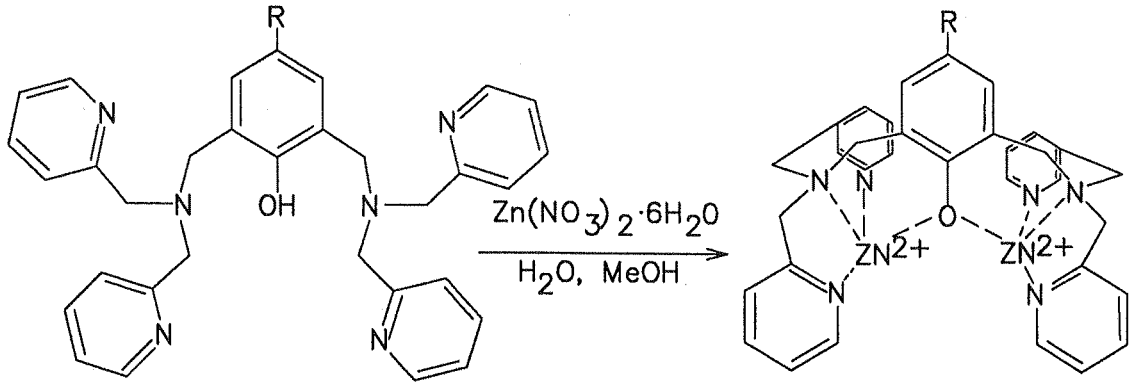
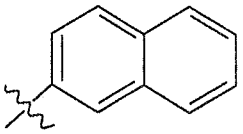
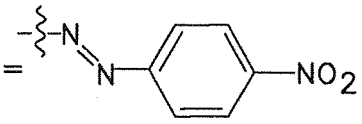
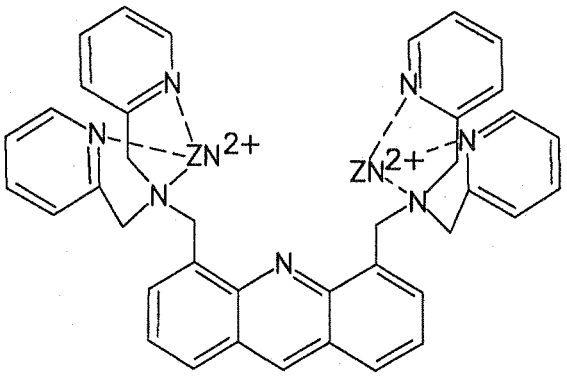

105_1
172B
172
172A
178
304
Metal4
302
116_1
306
Metal3
310
314
Metal2
318
328
322
Metal1
330
Pwell
152
B
162
158
D
160
338
340
326
S
156
165
164
336
308
312
316
320
114_1
170
324
166
112_1
Via3
Via2
Via1
334
159
N–well
154
332
Contact
322
P–Substrate

FIG. 11A

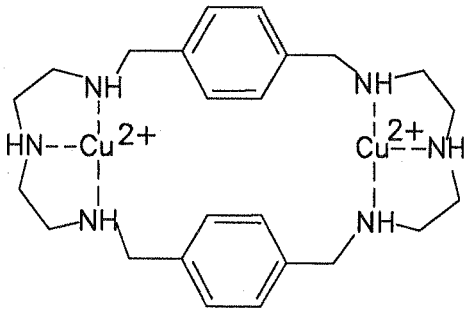


Compound 1 1R= 

Compound 2 2R= 

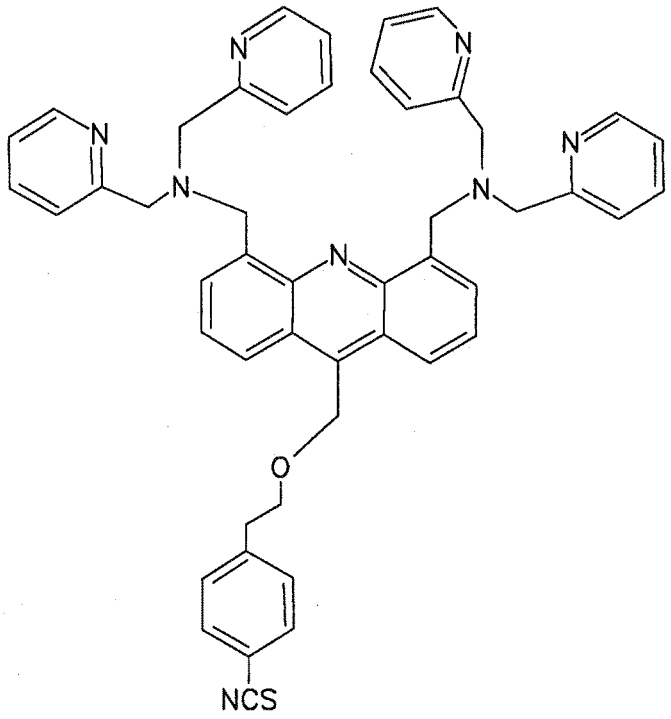


Compound 3



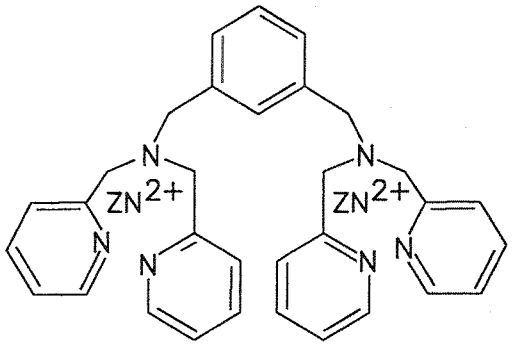
Compound 4

FIG. 11B(1)



Compound 10

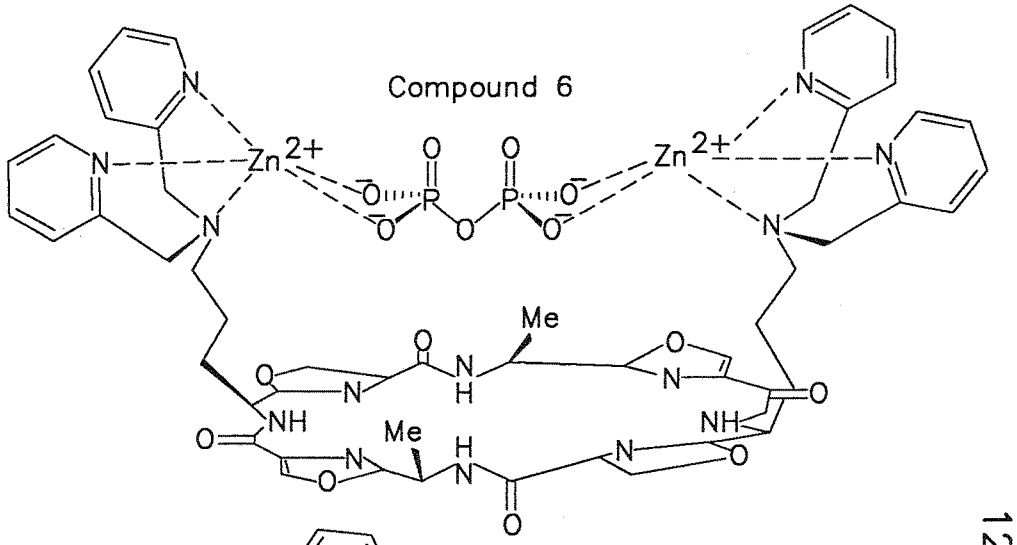
FIG. 11B(2)

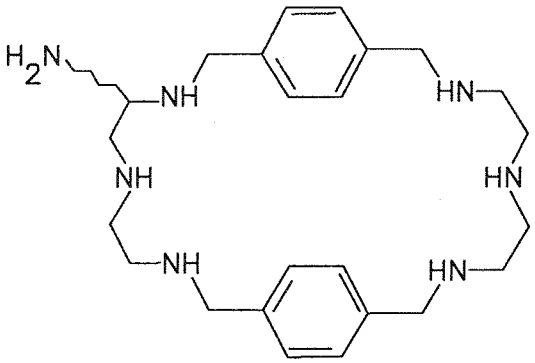


ZN^{2+} –dipicolylamine

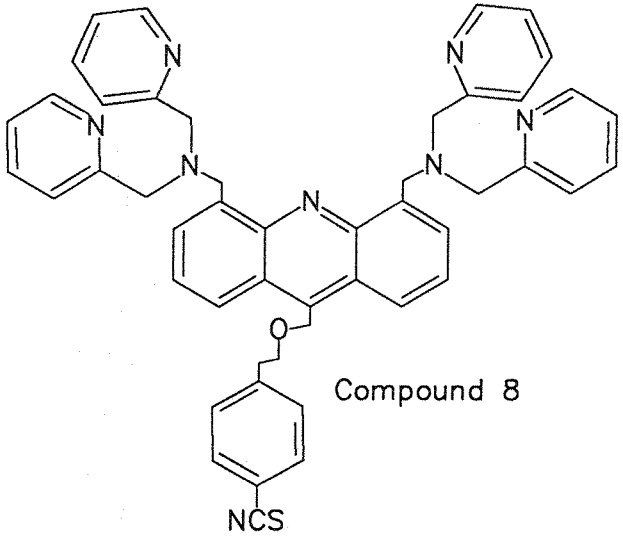
Compound 5

Compound 6

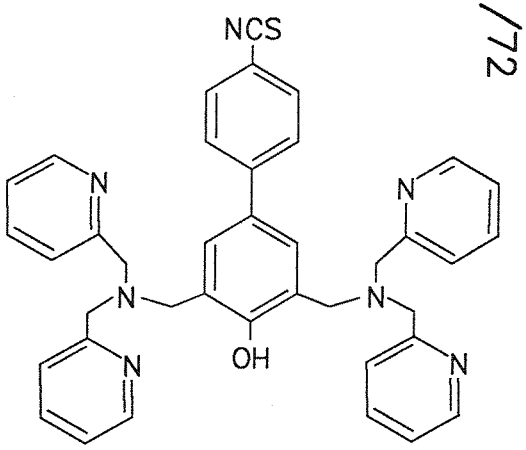




Compound 7



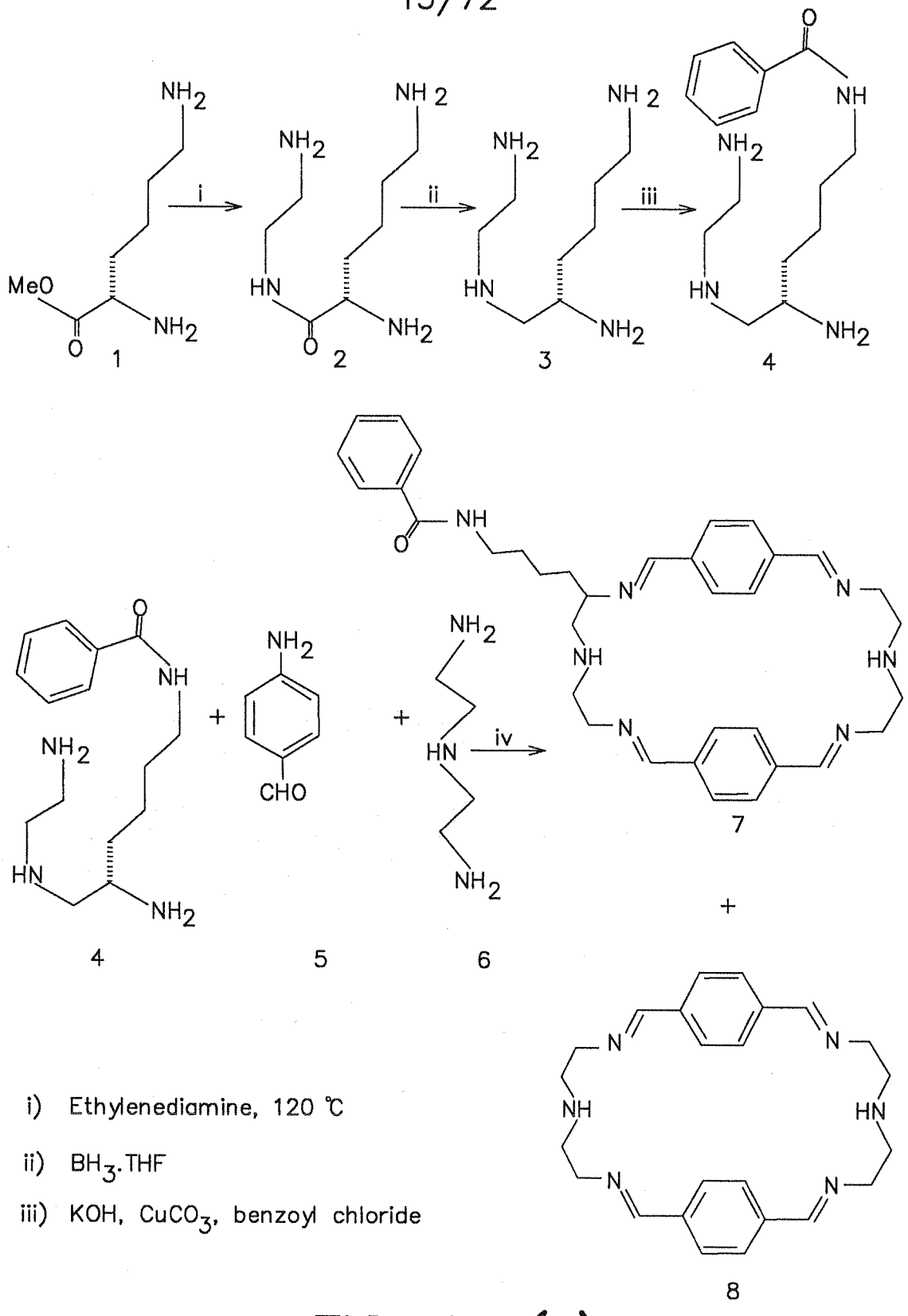
Compound 8



Compound 9

12/72

FIG. 11B(3)



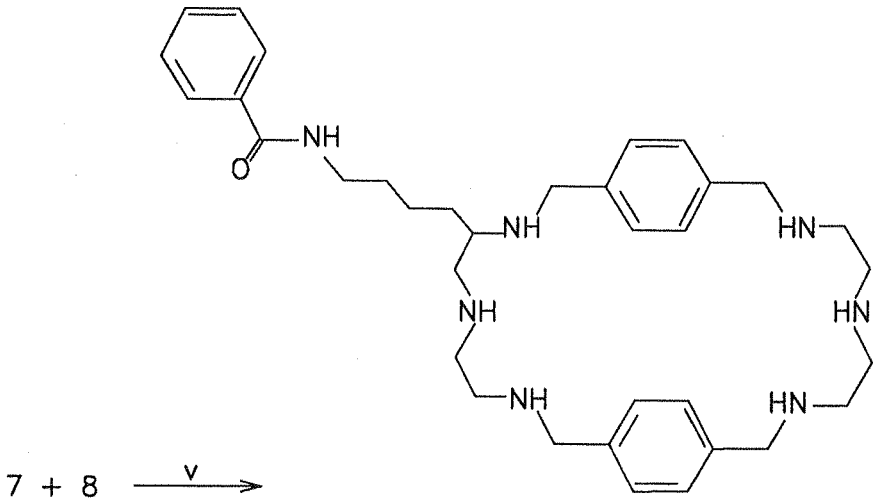
i) Ethylenediamine, 120 ℃

ii) BH_3.THF

iii) KOH, $CuCO_3$, benzoyl chloride

FIG. 11C(1)

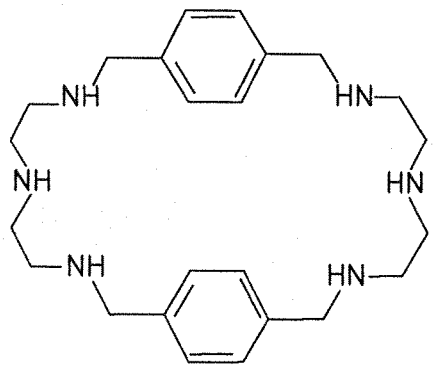
iv) 1:3 ratio of 4:6, MeOH, r.t.



7 + 8 $\xrightarrow{v}$

9

v) $NaBH_3$, MeOH



10

FIG. 11C(2)

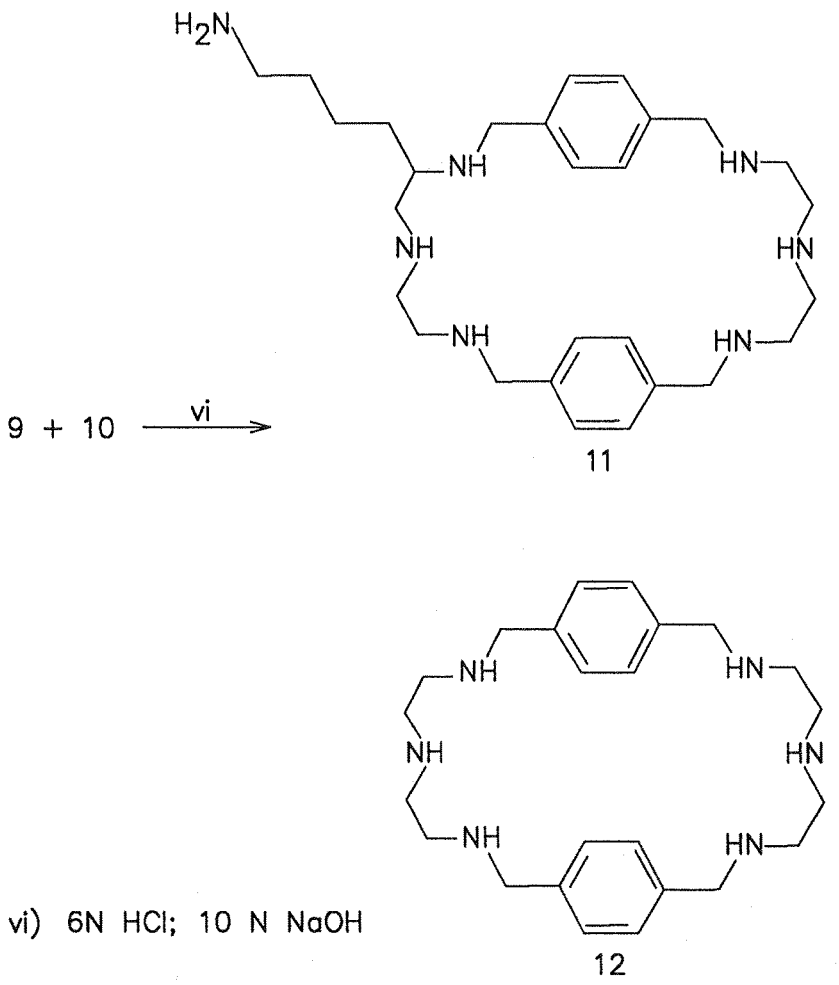

H2N
NH
HN
NH
HN
NH
HN
9 + 10
vi
11
NH
HN
NH
HN
NH
HN
12
vi) 6N HCl; 10 N NaOH

FIG. 11C(3)

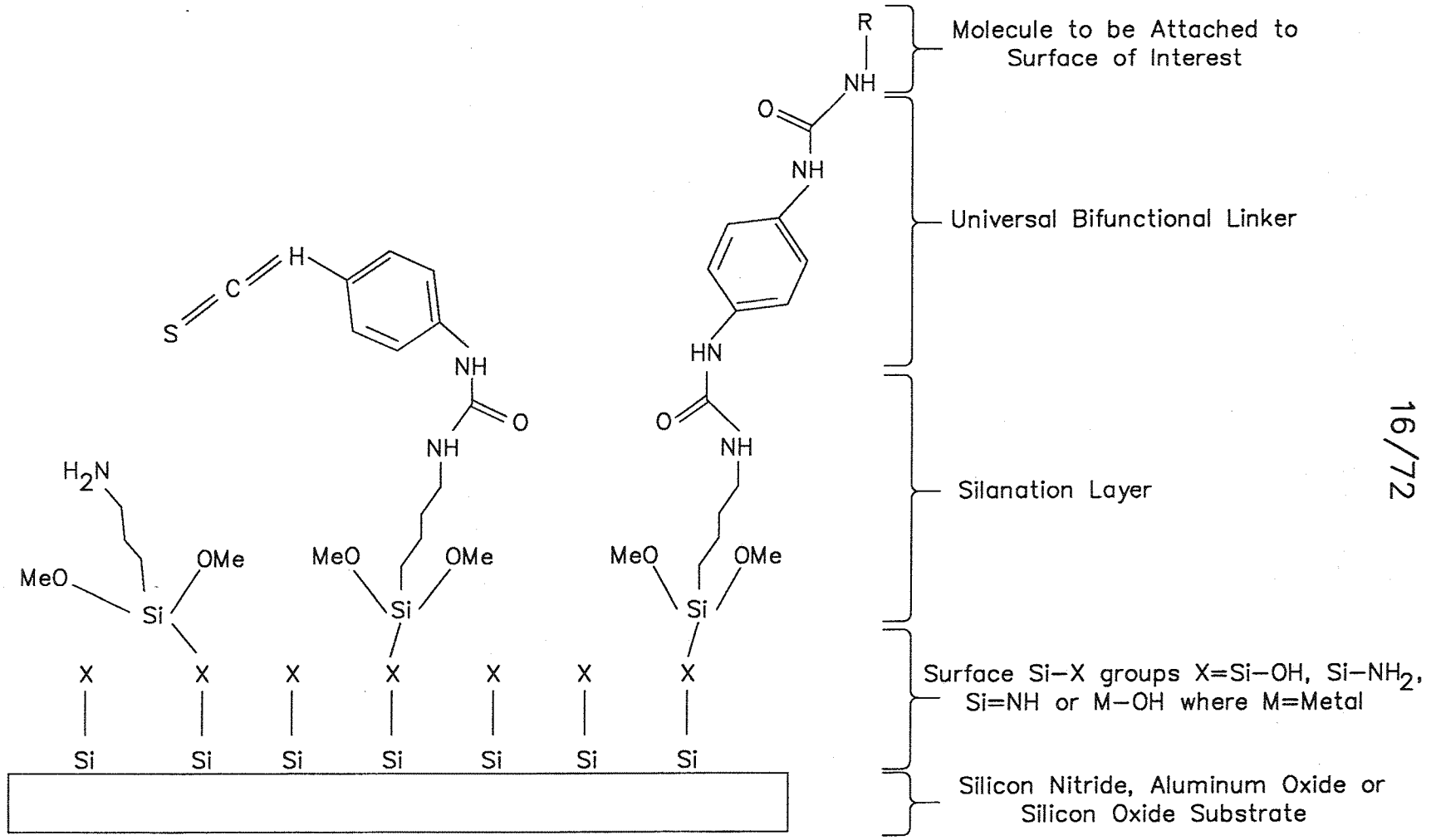

R
NH
O
NH
HN
O
NH
H
C
S
NH
O
NH
H_2N
MeO
OMe
Si
MeO
OMe
Si
MeO
OMe
Si
X
X
X
X
X
X
X
Si
Si
Si
Si
Si
Si
Si
Molecule to be Attached to Surface of Interest
Universal Bifunctional Linker
Silanation Layer
Surface Si–X groups X=Si–OH, Si–NH_2, Si=NH or M–OH where M=Metal
Silicon Nitride, Aluminum Oxide or Silicon Oxide Substrate

FIG. 11D(1)

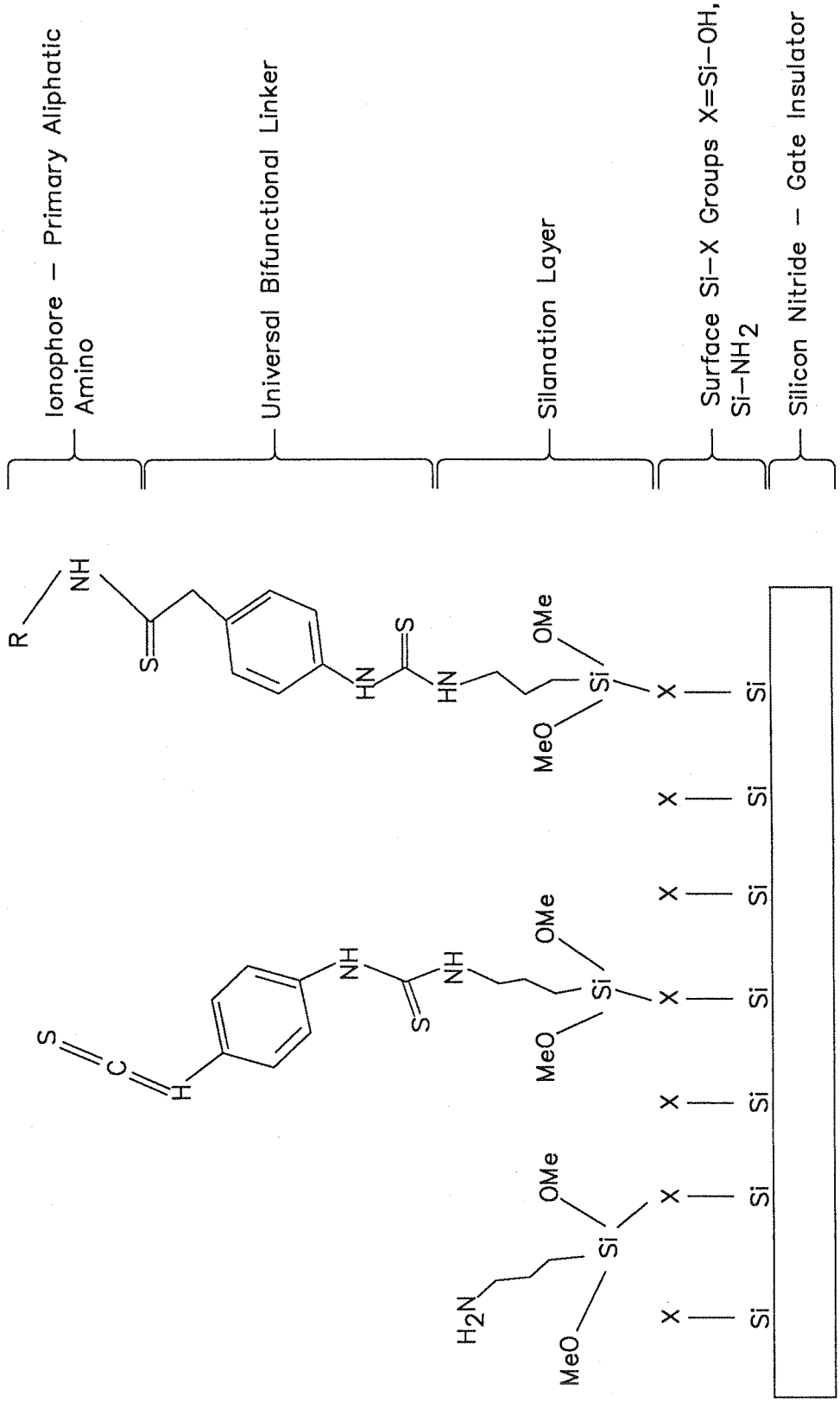

Ionophore – Primary Aliphatic Amino
Universal Bifunctional Linker
Silanation Layer
Surface Si–X Groups X=Si–OH, Si–NH2
Silicon Nitride – Gate Insulator
R
NH
S
HN
S
HN
OMe
Si
MeO
X
Si
S
C
H
NH
S
NH
OMe
Si
MeO
H2N
OMe
Si
MeO

FIG. 11D(2)

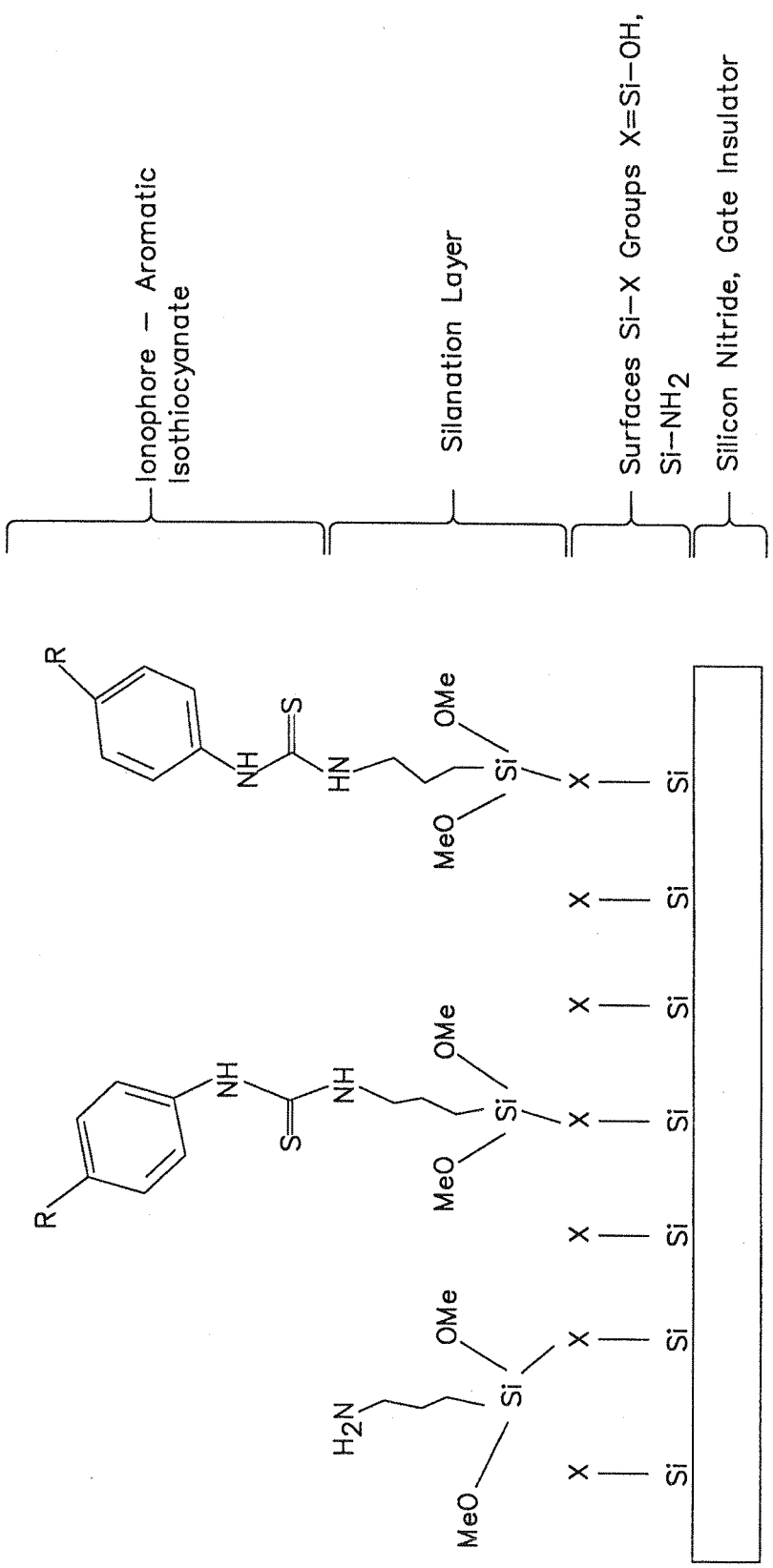

Ionophore – Aromatic Isothiocyanate
Silanation Layer
Surfaces Si–X Groups X=Si–OH, Si–NH2
Silicon Nitride, Gate Insulator
R
NH
S
HN
OMe
Si
MeO
X
Si
H2N

FIG. 11D(3)

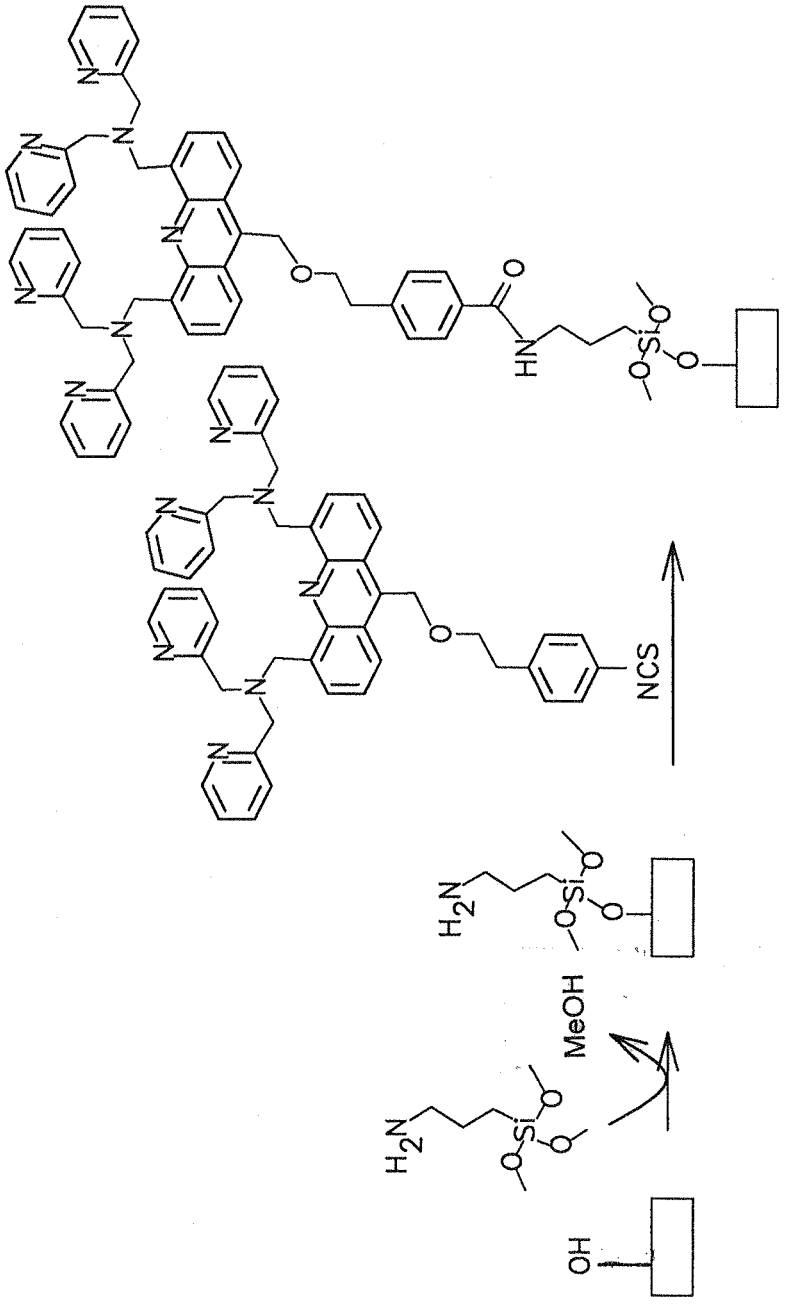


FIG. 11E

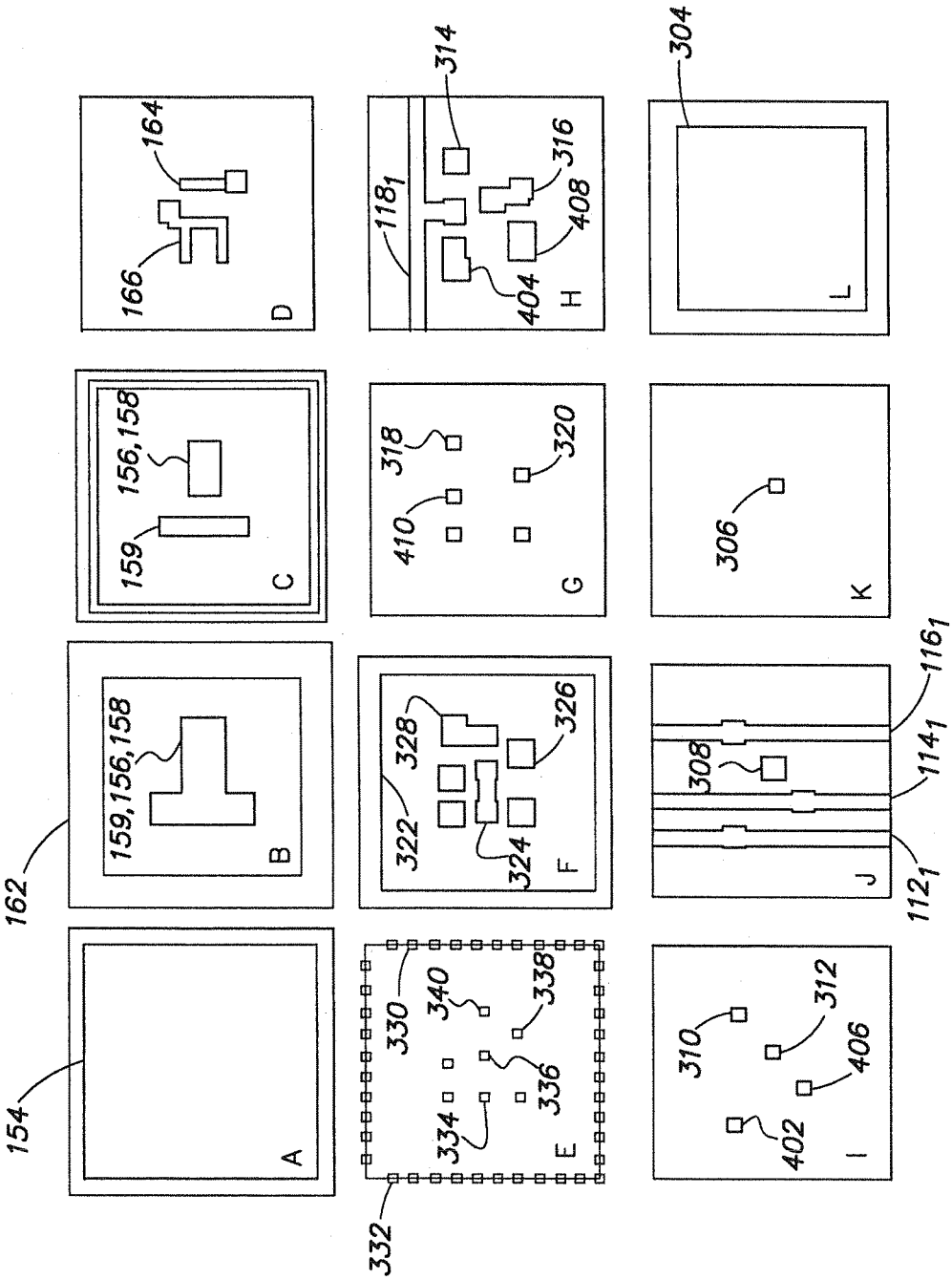

154
162
A
159,156,158
B
156,158
159
C
164
166
D
330
340
338
334
336
E
332
322
328
326
324
F
118₁
314
316
408
404
H
318
410
320
G
310
312
406
402
I
308
1161
1141
1121
J
306
K
304
L

FIG. 12

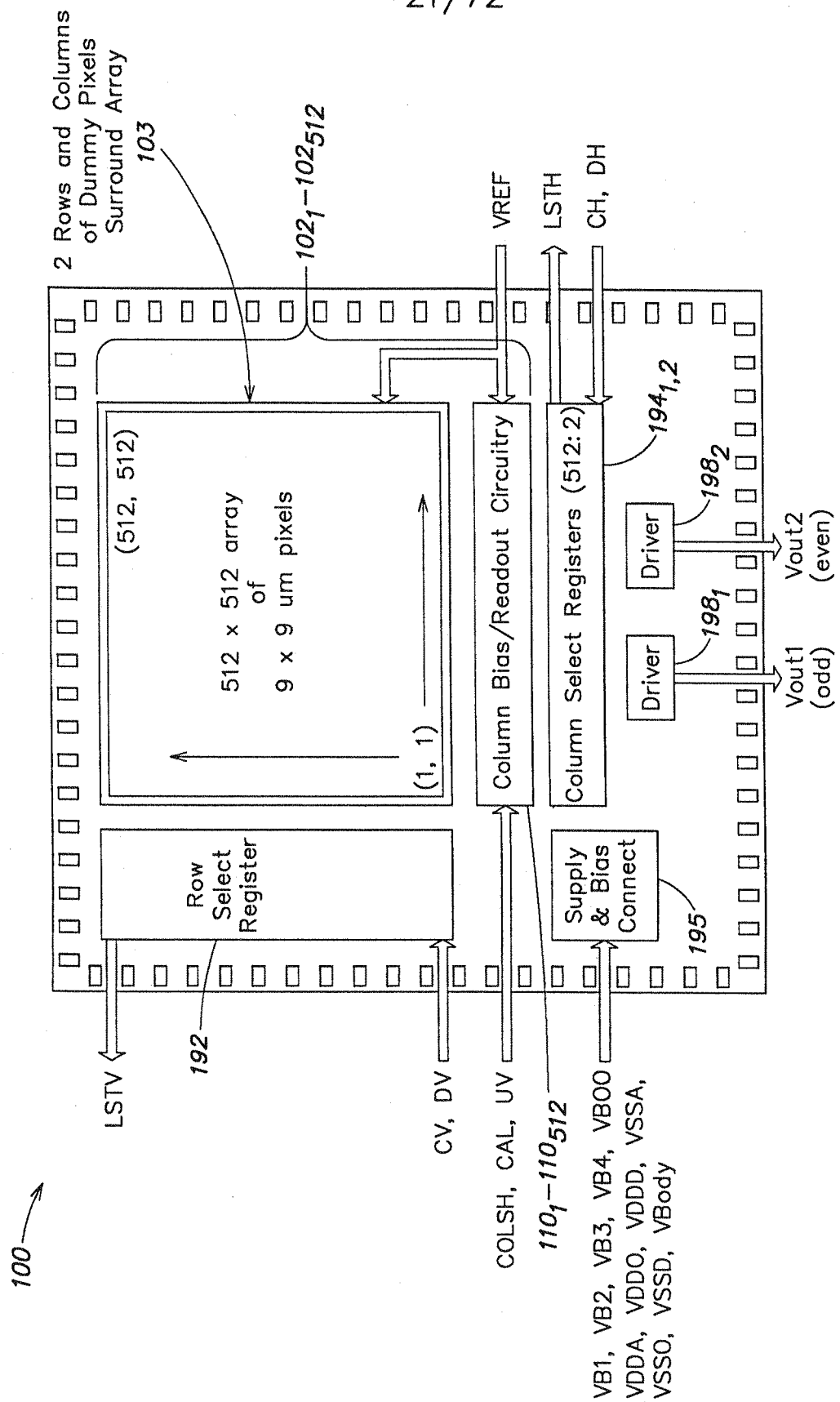

100
2 Rows and Columns of Dummy Pixels Surround Array
103
102_1–102_{512}
VREF
LSTH
CH, DH
(512, 512)
512 x 512 array of 9 x 9 um pixels
(1, 1)
Column Bias/Readout Circuitry
Column Select Registers (512: 2)
$194_{1,2}$
198_2
Driver
Vout2 (even)
198_1
Driver
Vout1 (odd)
Row Select Register
192
Supply & Bias Connect
195
LSTV
CV, DV
COLSH, CAL, UV
110_1–110_{512}
VB1, VB2, VB3, VB4, VBOO
VDDA, VDDO, VDDD, VSSA,
VSSO, VSSD, VBody

FIG. 13

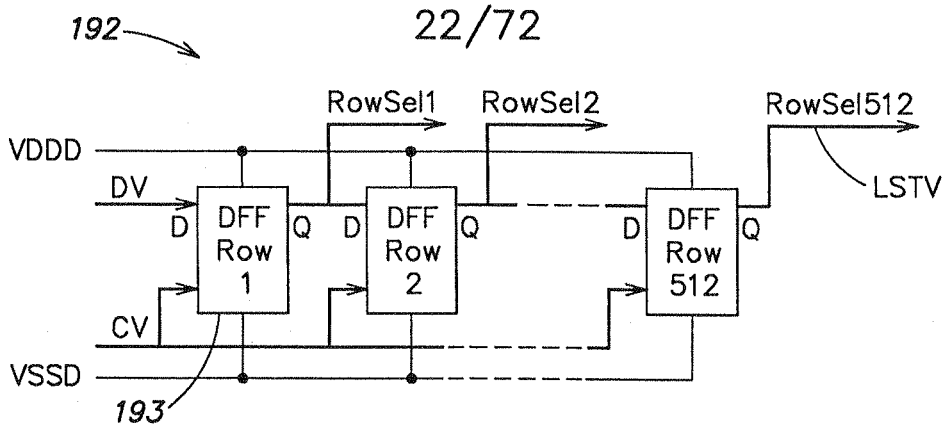


FIG. 14

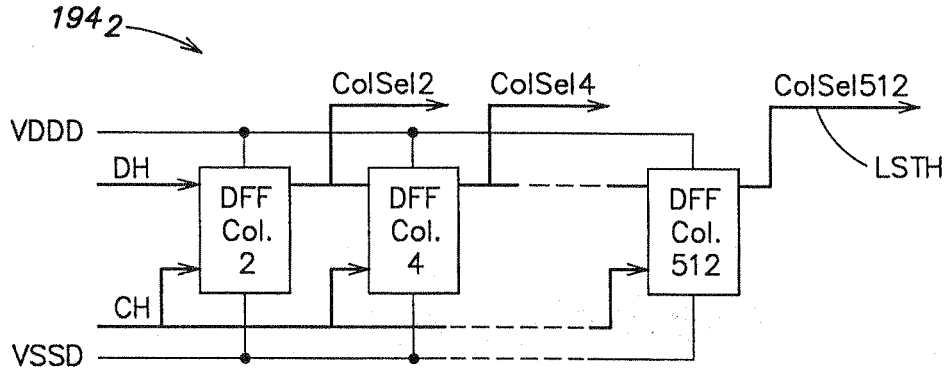


FIG. 15

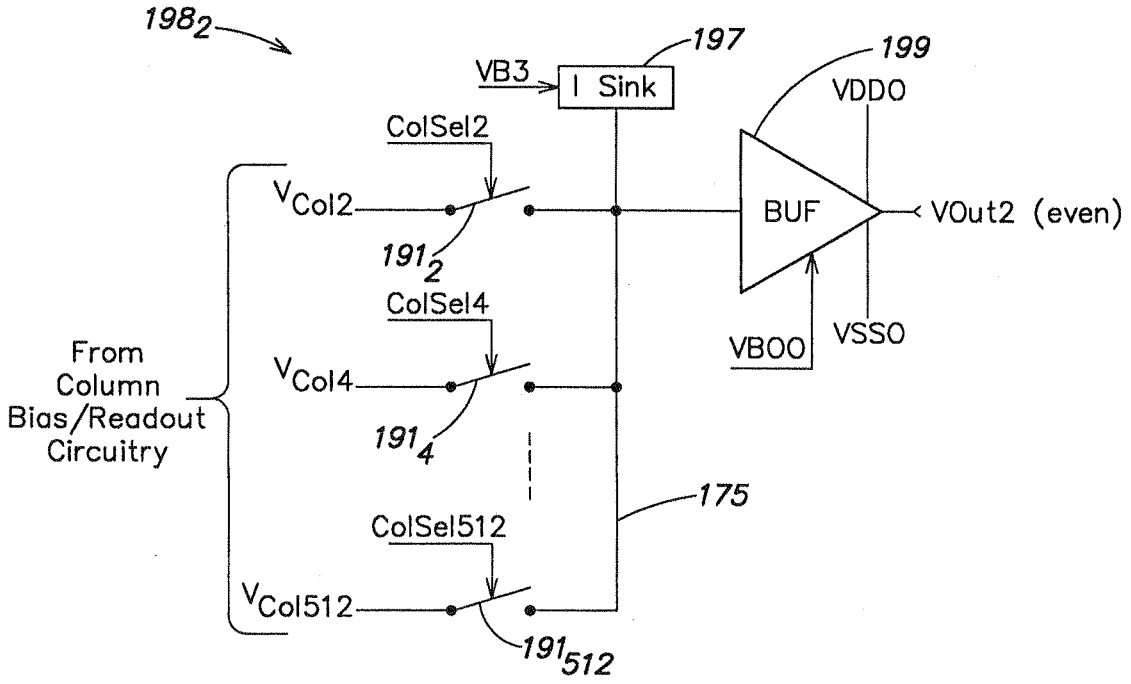


FIG. 16

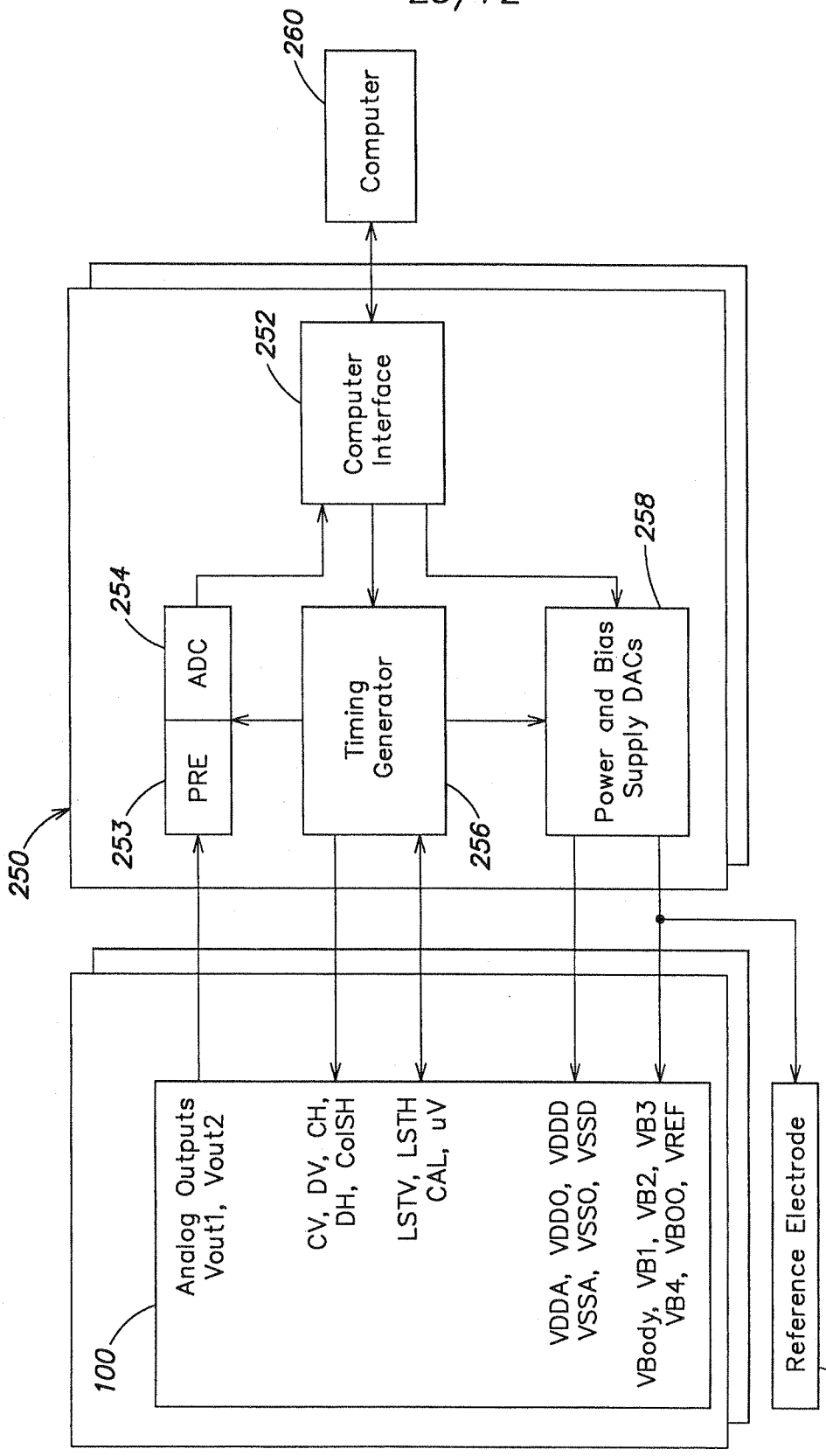

260
Computer
252
Computer Interface
254
ADC
PRE
253
Timing Generator
256
258
Power and Bias Supply DACs
250
100
Analog Outputs Vout1, Vout2
CV, DV, CH, DH, ColSH
LSTV, LSTH CAL, uV
VDDA, VDDO, VDDD VSSA, VSSO, VSSD
VBody, VB1, VB2, VB3 VB4, VB00, VREF
Reference Electrode
76

FIG. 17

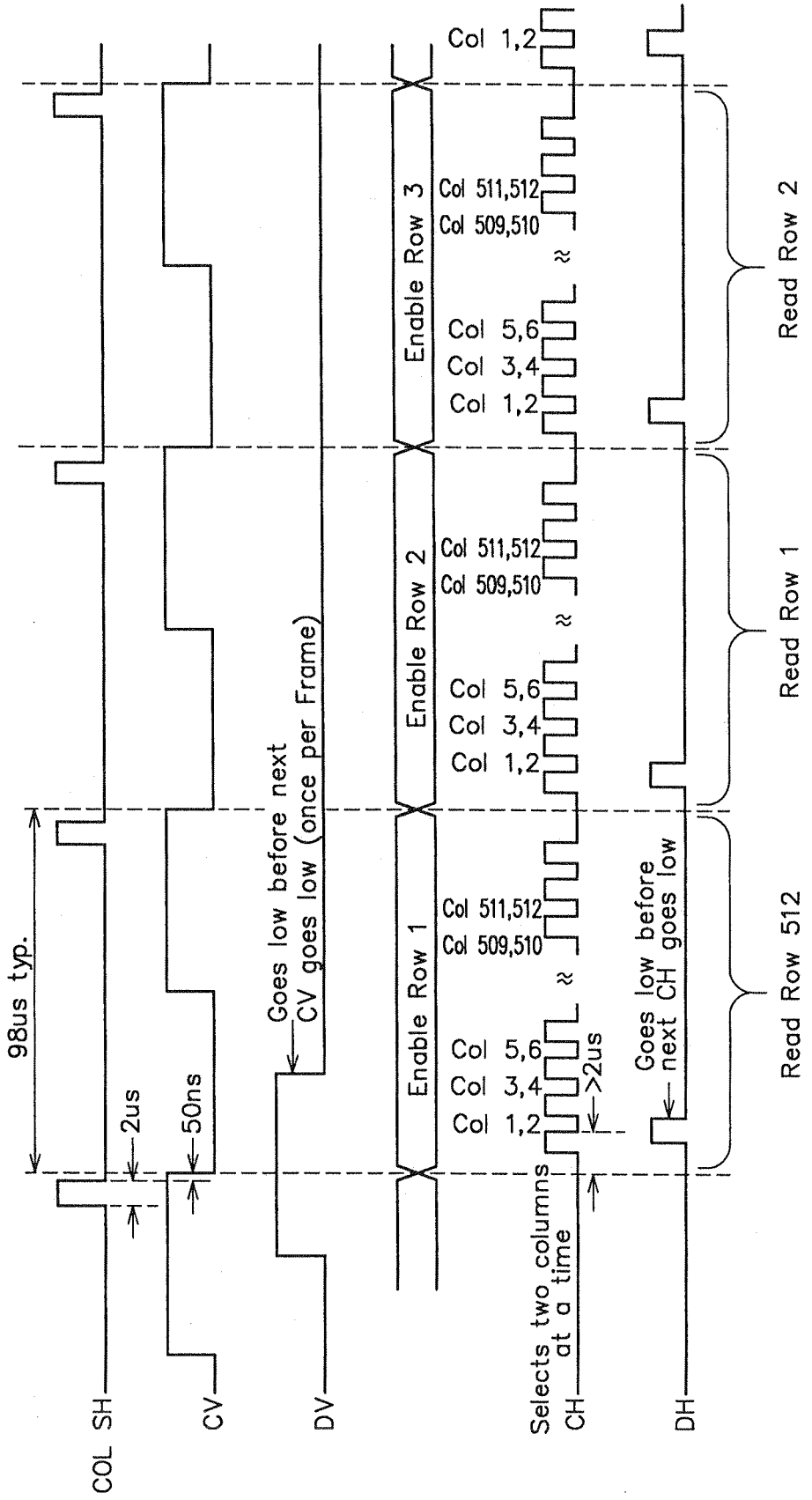

COL SH
CV
DV
CH
DH
98us typ.
2us
50ns
Goes low before next CV goes low (once per Frame)
Selects two columns at a time
>2us
Goes low before next CH goes low
Enable Row 1
Enable Row 2
Enable Row 3
Col 1,2
Col 3,4
Col 5,6
Col 509,510
Col 511,512
Read Row 1
Read Row 2
Read Row 512

FIG. 18

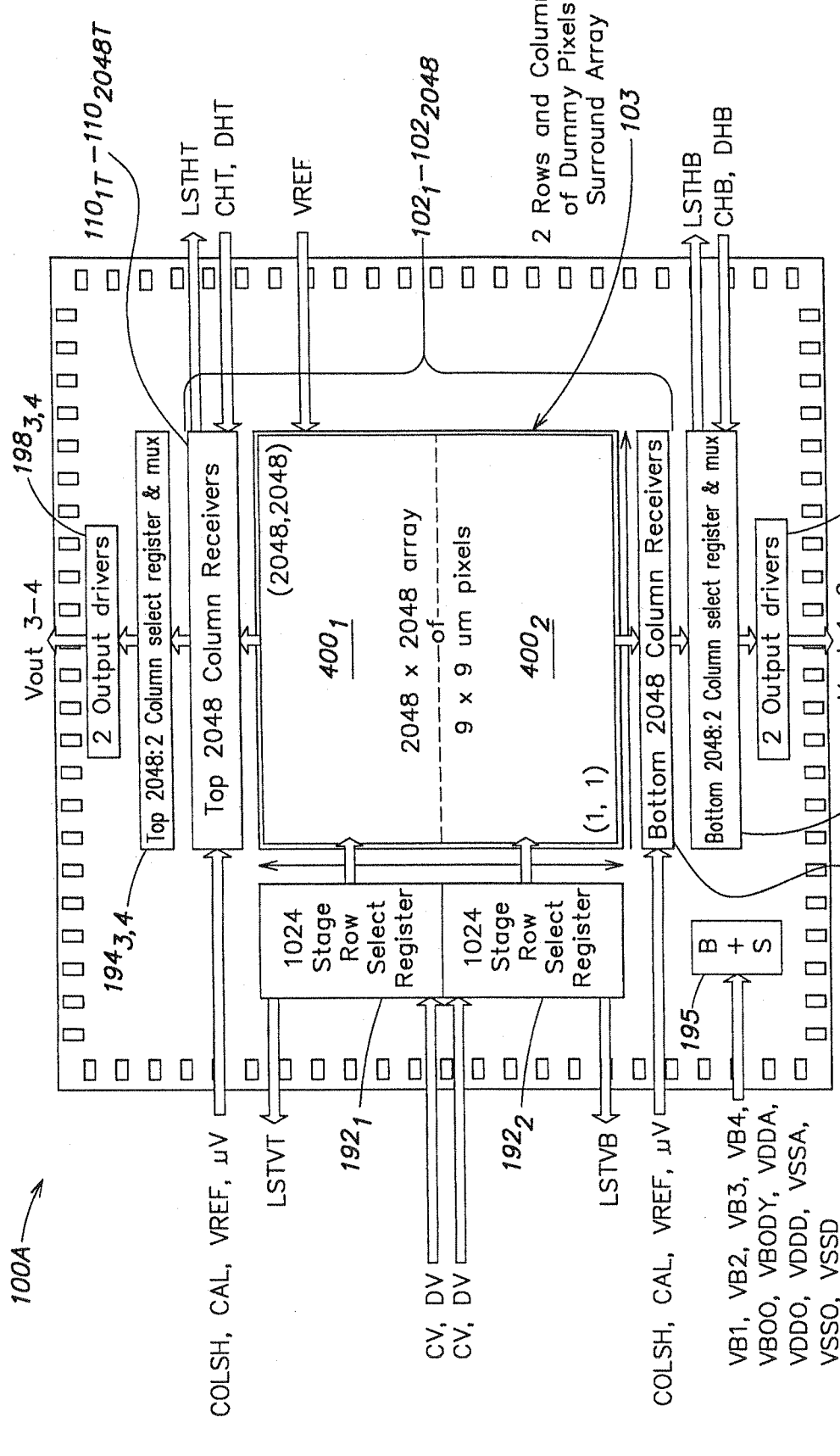

100A
Vout 3–4
2 Output drivers
Top 2048:2 Column select register & mux
Top 2048 Column Receivers
(2048,2048)
400₁
2048 x 2048 array
of
9 x 9 um pixels
400₂
(1, 1)
Bottom 2048 Column Receivers
Bottom 2048:2 Column select register & mux
2 Output drivers
Vout 1–2
LSTHT
CHT, DHT
VREF
2 Rows and Columns of Dummy Pixels Surround Array
LSTHB
CHB, DHB
1024 Stage Row Select Register
1024 Stage Row Select Register
B + S
195
COLSH, CAL, VREF, µV
LSTVT
CV, DV
CV, DV
LSTVB
COLSH, CAL, VREF, µV
VB1, VB2, VB3, VB4,
VBOO, VBODY, VDDA,
VDDO, VDDD, VSSA,
VSSO, VSSD
110_{1T}–110_{2048T}
102_1–102_{2048}
103
$198_{3,4}$
$194_{3,4}$
192_1
192_2
$198_{1,2}$
$194_{1,2}$
110_{1B}–110_{2048B}

FIG. 19

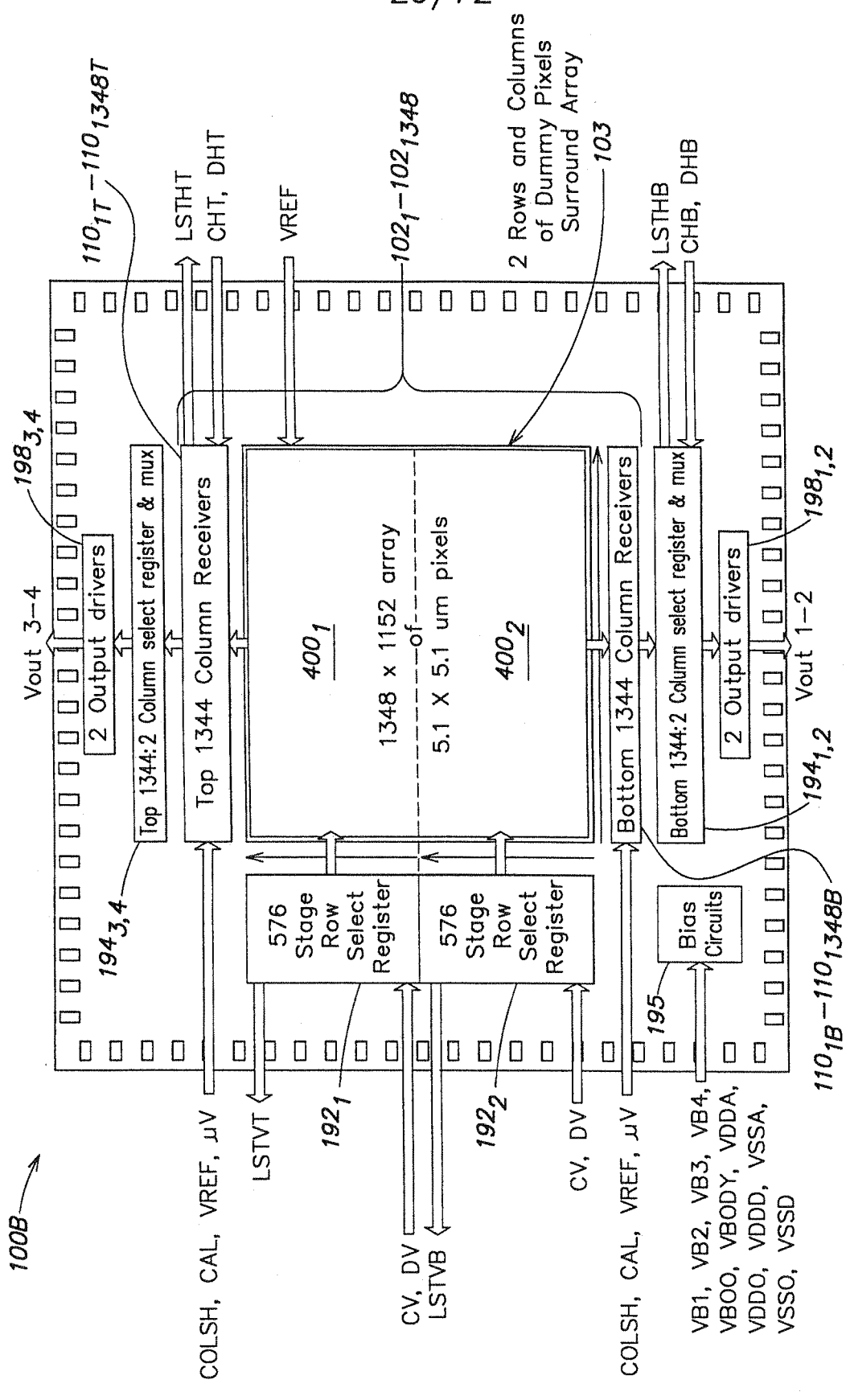

100B
Vout 3–4
Vout 1–2
2 Output drivers
Top 1344:2 Column select register & mux
Top 1344 Column Receivers
Bottom 1344 Column Receivers
Bottom 1344:2 Column select register & mux
1348 x 1152 array
of
5.1 X 5.1 um pixels
400 1
400 2
576 Stage Row Select Register
576 Stage Row Select Register
Bias Circuits
LSTHT
CHT, DHT
VREF
LSTHB
CHB, DHB
2 Rows and Columns of Dummy Pixels Surround Array
103
COLSH, CAL, VREF, µV
LSTVT
CV, DV
LSTVB
CV, DV
COLSH, CAL, VREF, µV
VB1, VB2, VB3, VB4,
VBOO, VBODY, VDDA,
VDDO, VDDD, VSSA,
VSSO, VSSD
195
192 1
192 2
194 3,4
194 1,2
198 3,4
198 1,2
110 1T – 110 1348T
102 1 – 102 1348
110 1B – 110 1348B

FIG. 20

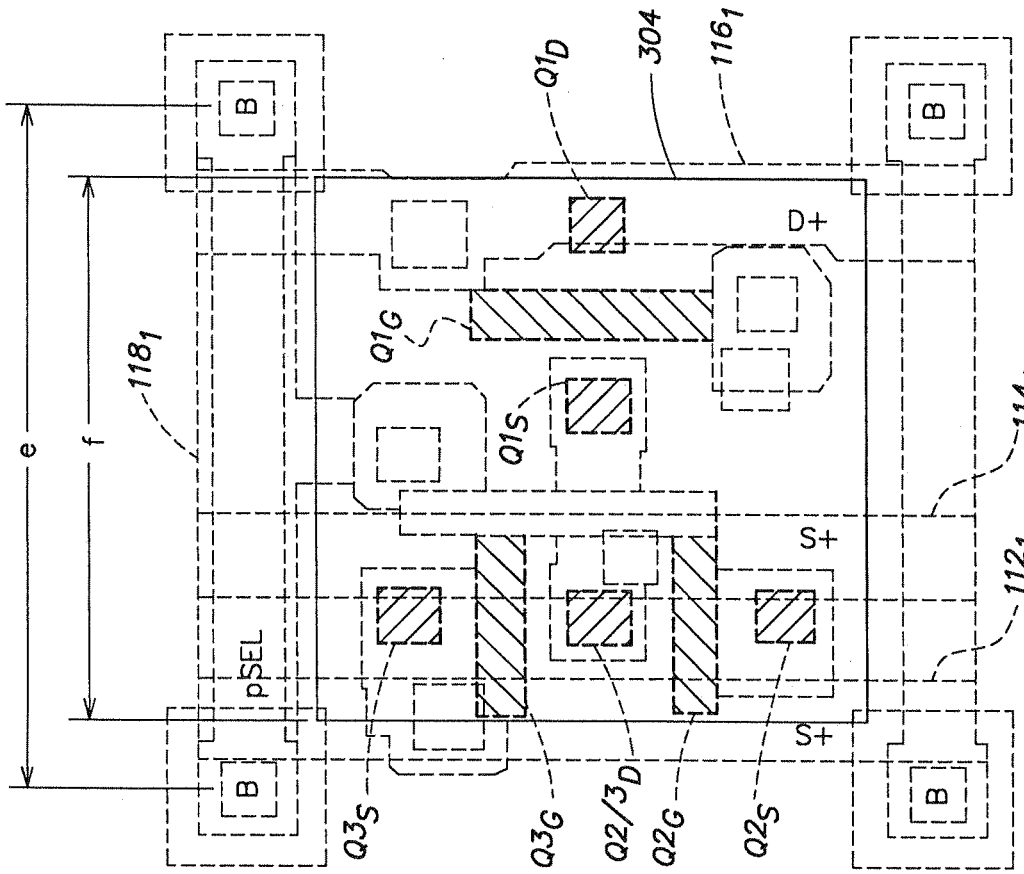

B
B
B
B
$Q1_D$
304
116_1
D+
$Q1_G$
$Q1_S$
118_1
114_1
S+
112_1
S+
pSEL
e
f
$Q3_S$
$Q3_G$
$Q2/3_D$
$Q2_G$
$Q2_S$

FIG. 20A

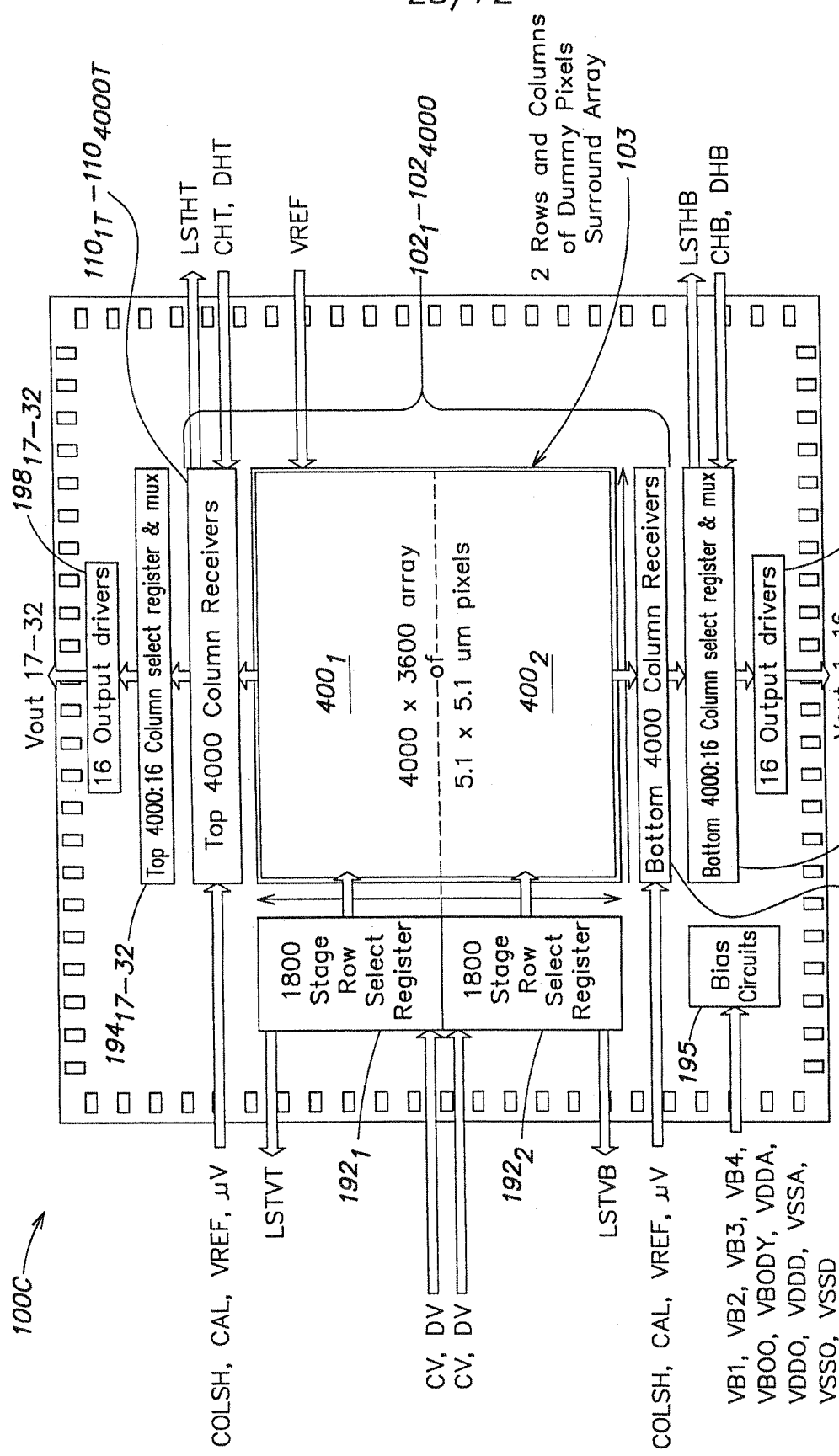

100C
Vout 17–32
16 Output drivers
Top 4000:16 Column select register & mux
Top 4000 Column Receivers
4000 x 3600 array
of
5.1 x 5.1 um pixels
Bottom 4000 Column Receivers
Bottom 4000:16 Column select register & mux
16 Output drivers
Vout 1–16
1800 Stage Row Select Register
1800 Stage Row Select Register
Bias Circuits
LSTHT
CHT, DHT
VREF
2 Rows and Columns of Dummy Pixels Surround Array
LSTHB
CHB, DHB
COLSH, CAL, VREF, µV
LSTVT
CV, DV
CV, DV
LSTVB
COLSH, CAL, VREF, µV
VB1, VB2, VB3, VB4,
VB00, VBODY, VDDA,
VDDO, VDDD, VSSA,
VSSO, VSSD
110_{1T}–110_{4000T}
102_1–102_{4000}
103
$198_{17–32}$
$198_{1–16}$
$194_{17–32}$
$194_{1–16}$
192_1
192_2
195
110_{1B}–110_{4000B}
400_1
400_2

FIG. 21

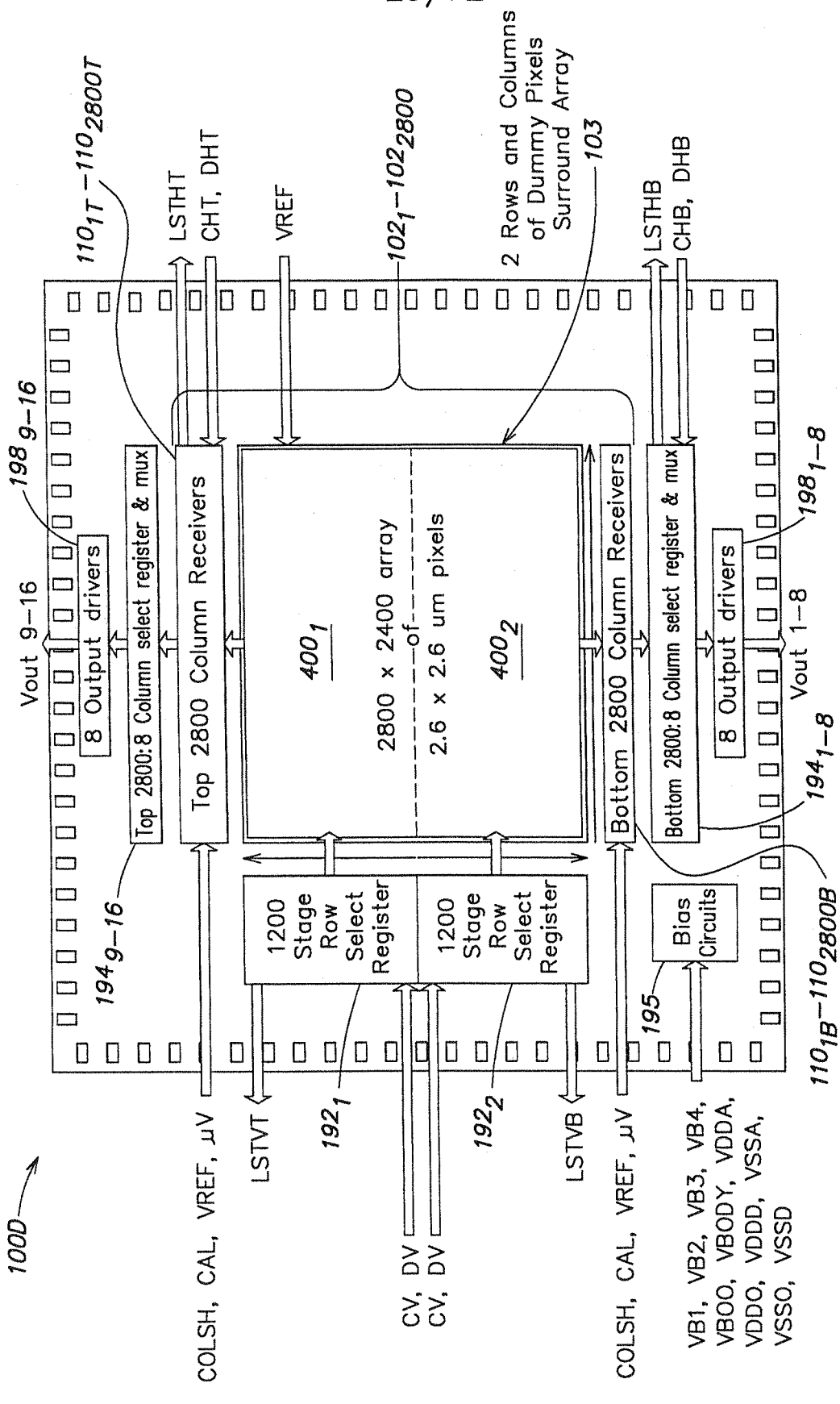

100D
Vout 9–16
198 9–16
8 Output drivers
Top 2800:8 Column select register & mux
194 9–16
Top 2800 Column Receivers
110 1T – 110 2800T
LSTHT
CHT, DHT
VREF
102 1 – 102 2800
2 Rows and Columns of Dummy Pixels Surround Array
103
LSTHB
CHB, DHB
400 1
2800 x 2400 array
of
2.6 x 2.6 um pixels
400 2
Bottom 2800 Column Receivers
Bottom 2800:8 Column select register & mux
8 Output drivers
198 1–8
Vout 1–8
194 1–8
110 1B – 110 2800B
1200 Stage Row Select Register
1200 Stage Row Select Register
192 1
192 2
Bias Circuits
195
COLSH, CAL, VREF, µV
LSTVT
CV, DV
CV, DV
LSTVB
COLSH, CAL, VREF, µV
VB1, VB2, VB3, VB4, VBOO, VBODY, VDDA, VDDO, VDDD, VSSA, VSSO, VSSD

FIG. 22

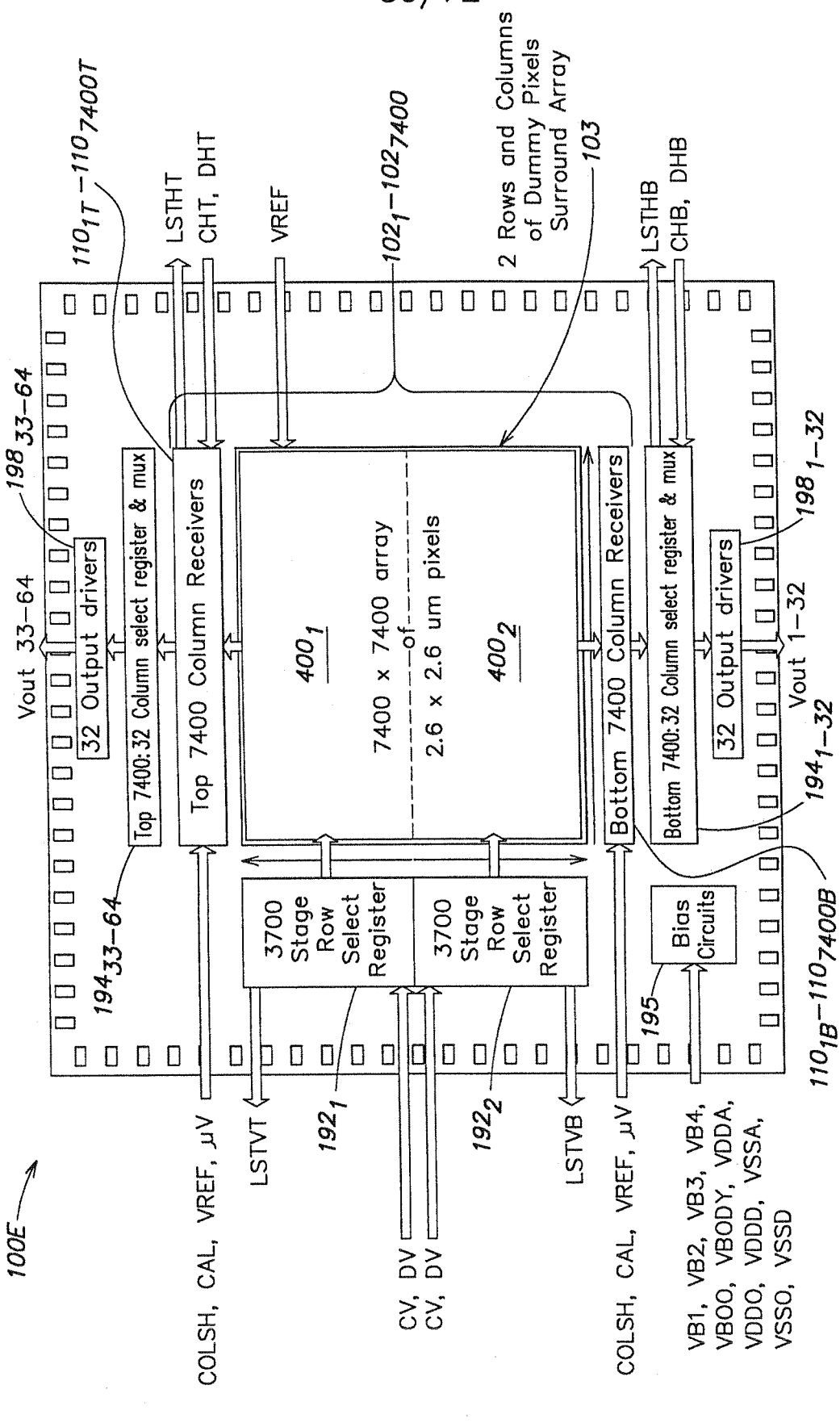

100E
Vout 33–64
32 Output drivers
Top 7400:32 Column select register & mux
Top 7400 Column Receivers
LSTHT
CHT, DHT
VREF
2 Rows and Columns of Dummy Pixels Surround Array
LSTHB
CHB, DHB
Bottom 7400 Column Receivers
Bottom 7400:32 Column select register & mux
32 Output drivers
Vout 1–32
7400 x 7400 array
of
2.6 x 2.6 um pixels
3700 Stage Row Select Register
3700 Stage Row Select Register
Bias Circuits
COLSH, CAL, VREF, µV
LSTVT
CV, DV
CV, DV
LSTVB
COLSH, CAL, VREF, µV
VB1, VB2, VB3, VB4, VBOO, VBODY, VDDA, VDDO, VDDD, VSSA, VSSO, VSSD

FIG. 23

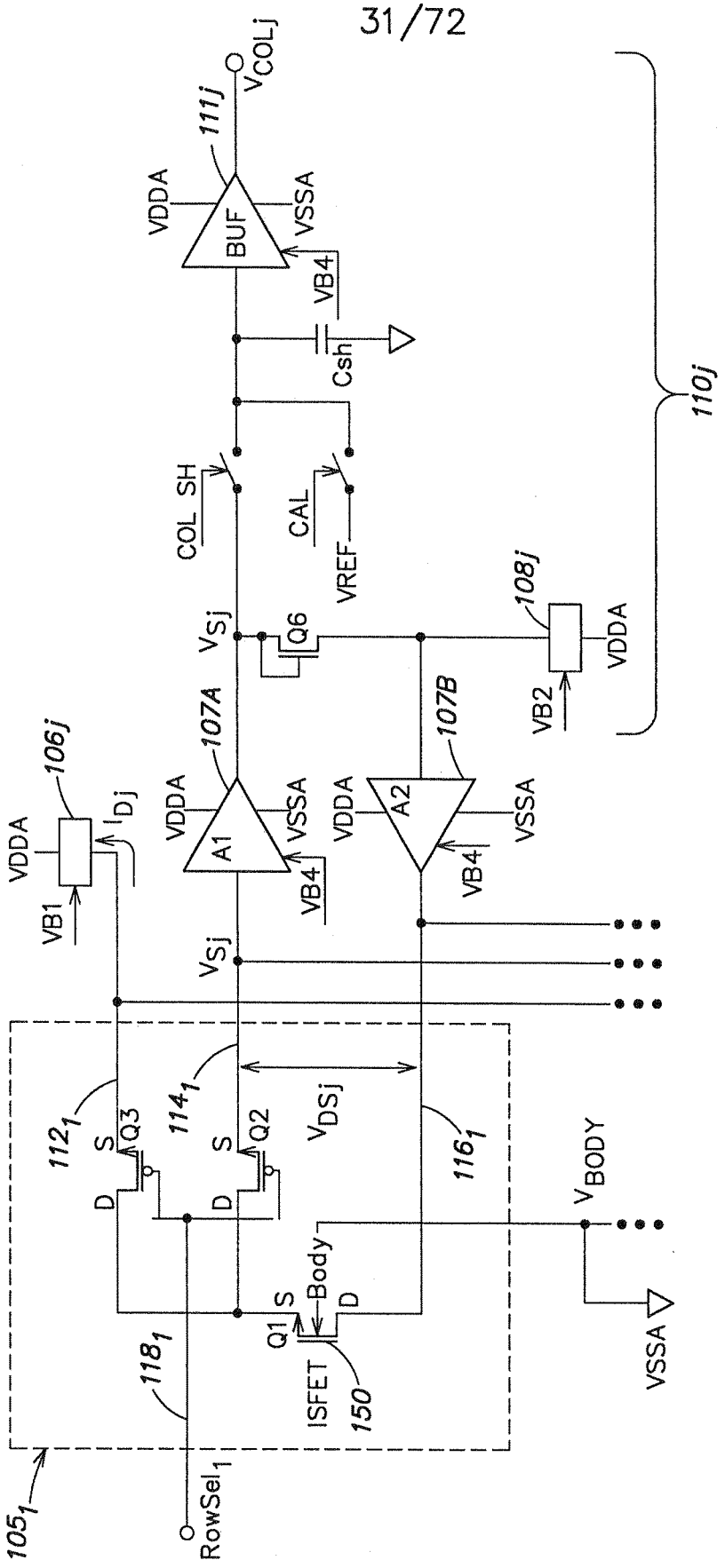

105_1
RowSel$_1$
118_1
ISFET
150
Q1
S
Body
D
116_1
V_{DSj}
114_1
112_1
S
Q3
D
S
Q2
D
V_{BODY}
VSSA
V_{Sj}
V_{Sj}
VB1
VDDA
I_{Dj}
106j
107A
VDDA
A1
VSSA
VB4
107B
VDDA
A2
VSSA
VB4
Q6
V_{Sj}
108j
VDDA
VB2
110j
COL SH
CAL
VREF
Csh
VB4
VDDA
BUF
VSSA
111j
V_{COLj}

FIG. 24

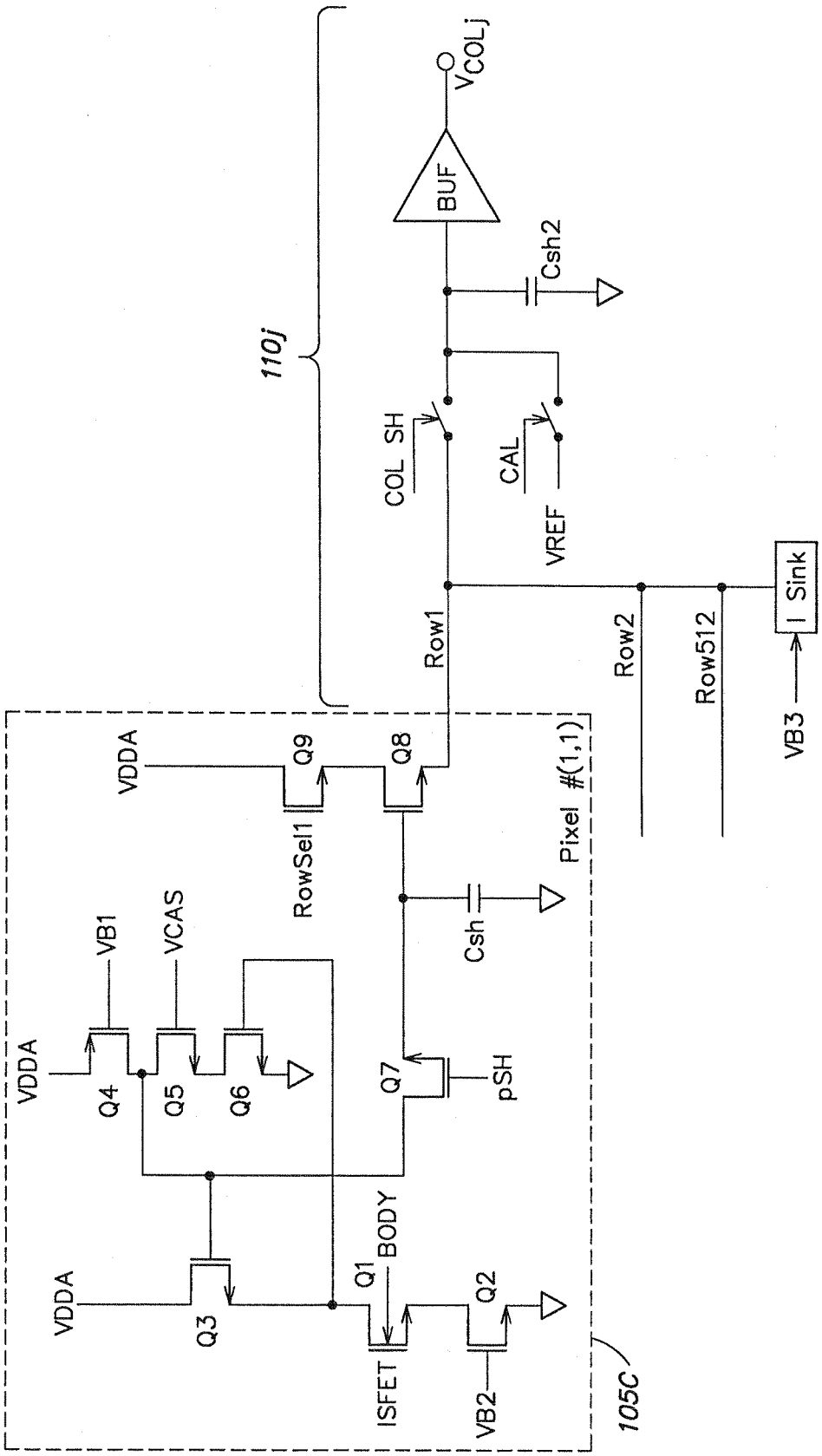

110j
VCOLj
BUF
Csh2
COL SH
CAL
VREF
I Sink
Row1
Row2
Row512
VB3
VDDA
Q9
Q8
RowSel1
Pixel #(1,1)
Csh
VB1
VCAS
Q4
Q5
Q6
Q7
pSH
Q3
Q1
BODY
Q2
ISFET
VB2
105C

FIG. 25

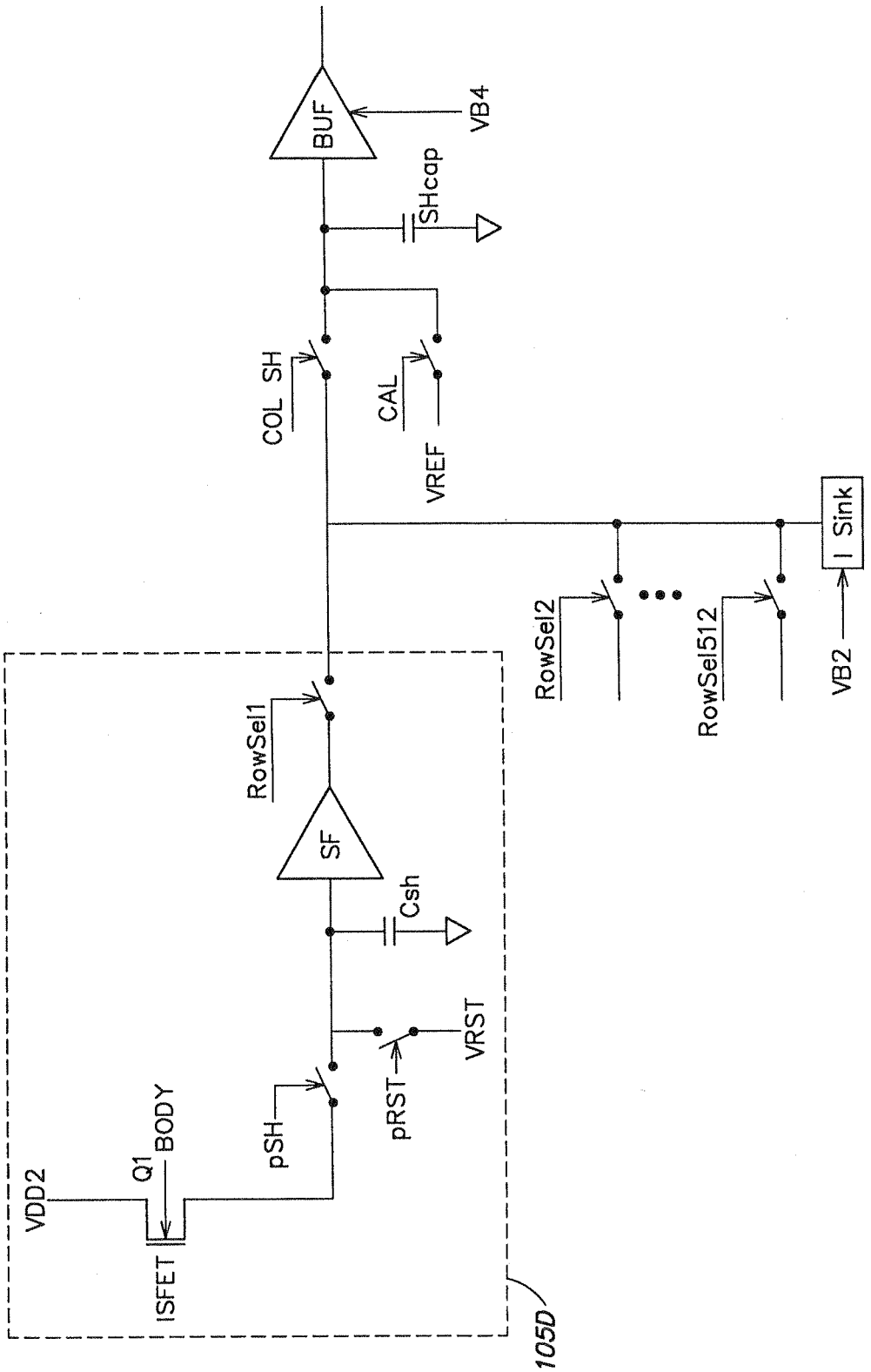

BUF
VB4
SHcap
COL SH
CAL
VREF
I Sink
RowSel2
RowSel512
VB2
RowSel1
SF
Csh
VRST
pRST
pSH
BODY
Q1
VDD2
ISFET
105D

FIG. 26

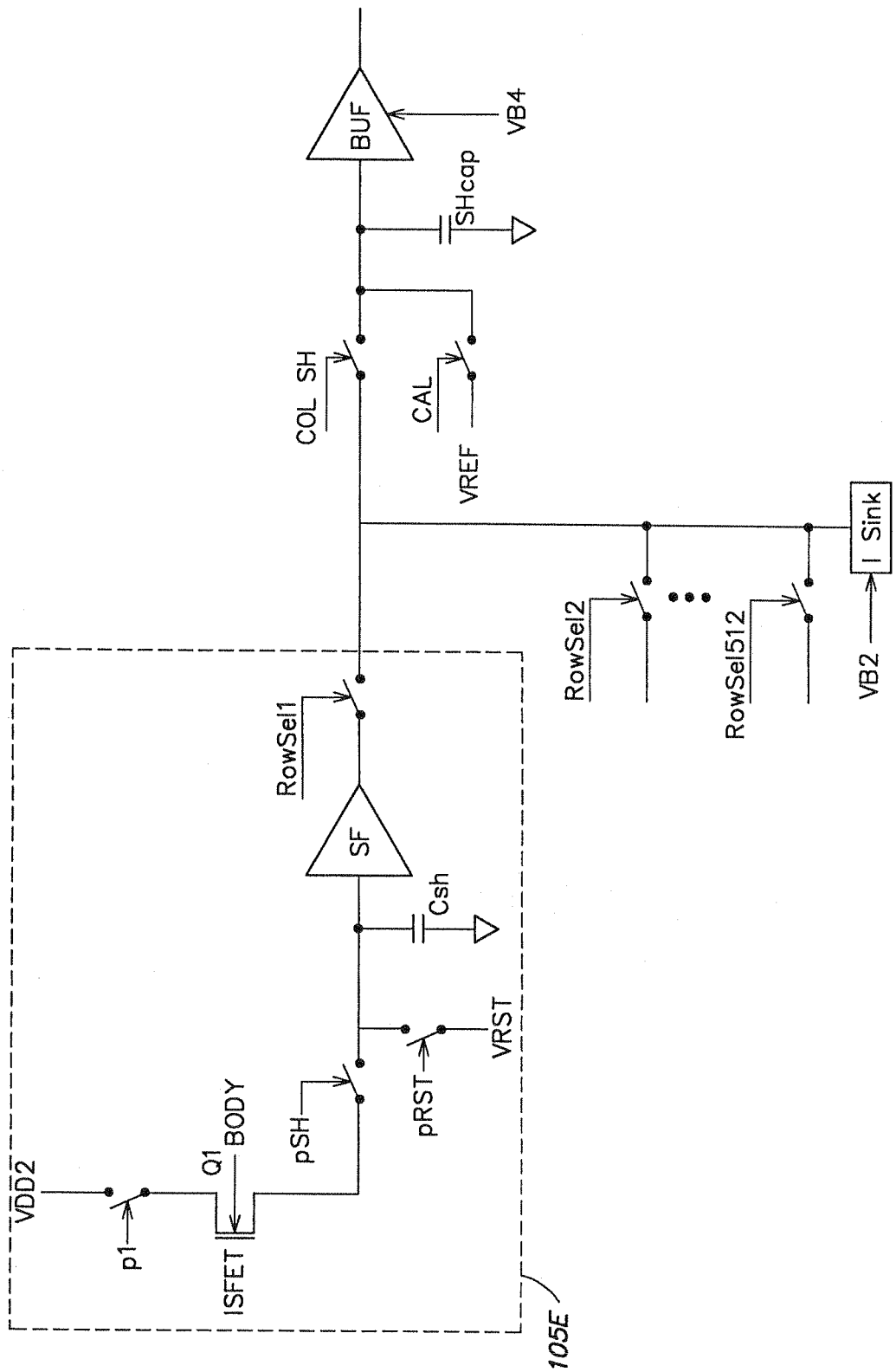

VDD2
p1
ISFET
Q1
BODY
pSH
pRST
VRST
RowSel1
SF
Csh
105E
COL SH
CAL
VREF
BUF
VB4
SHcap
RowSel2
RowSel512
I Sink
VB2

FIG. 27

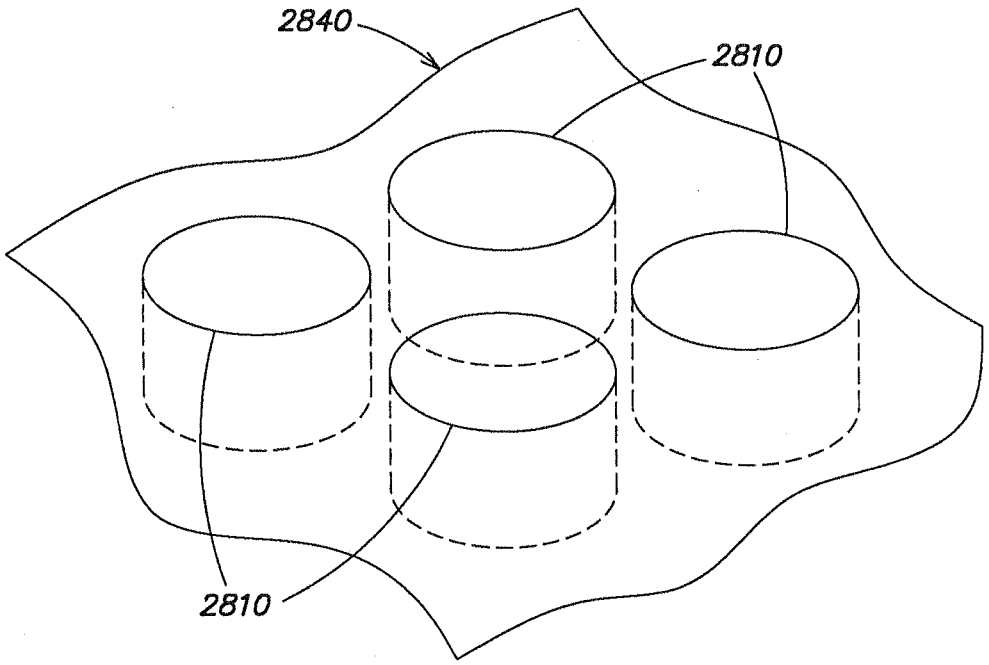


FIG. 28A

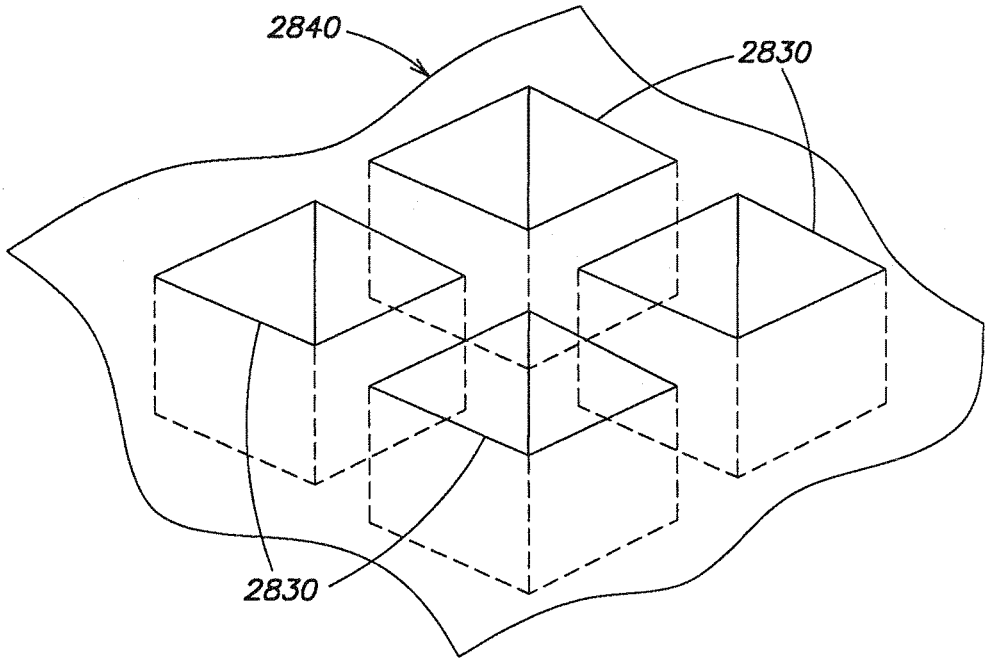


FIG. 28B

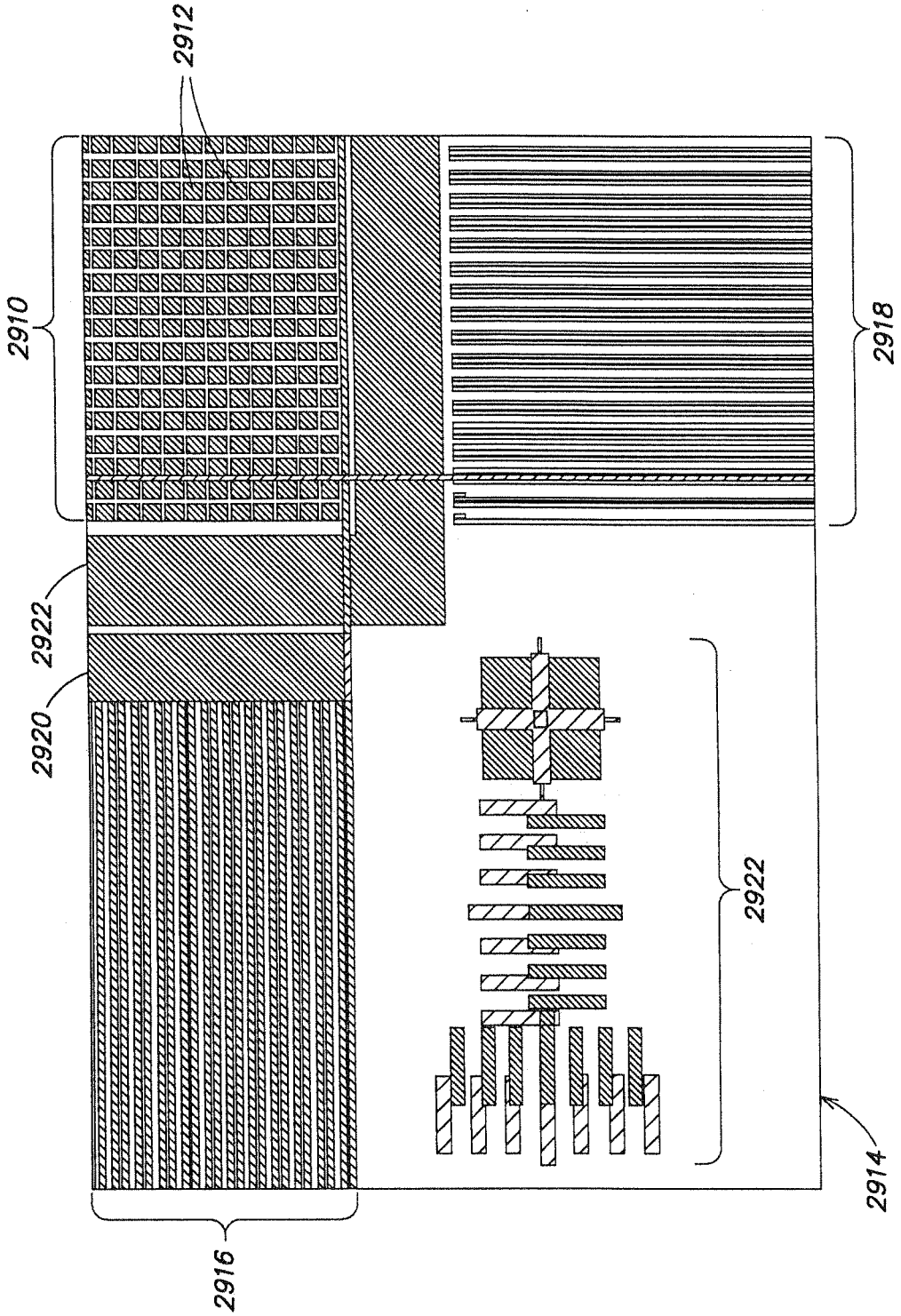


FIG. 29

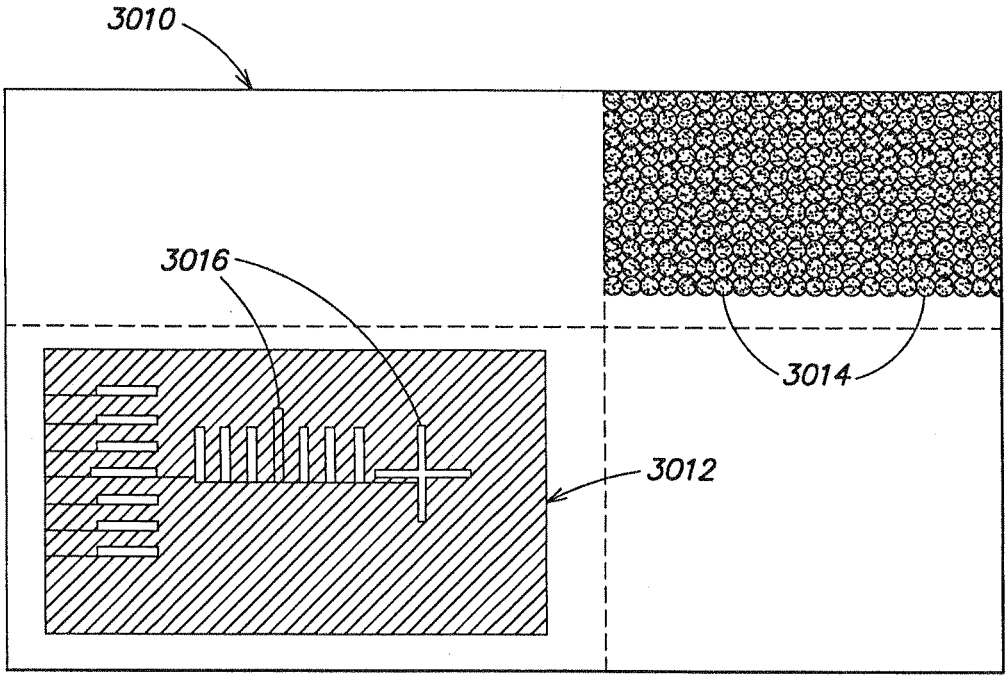


FIG. 30

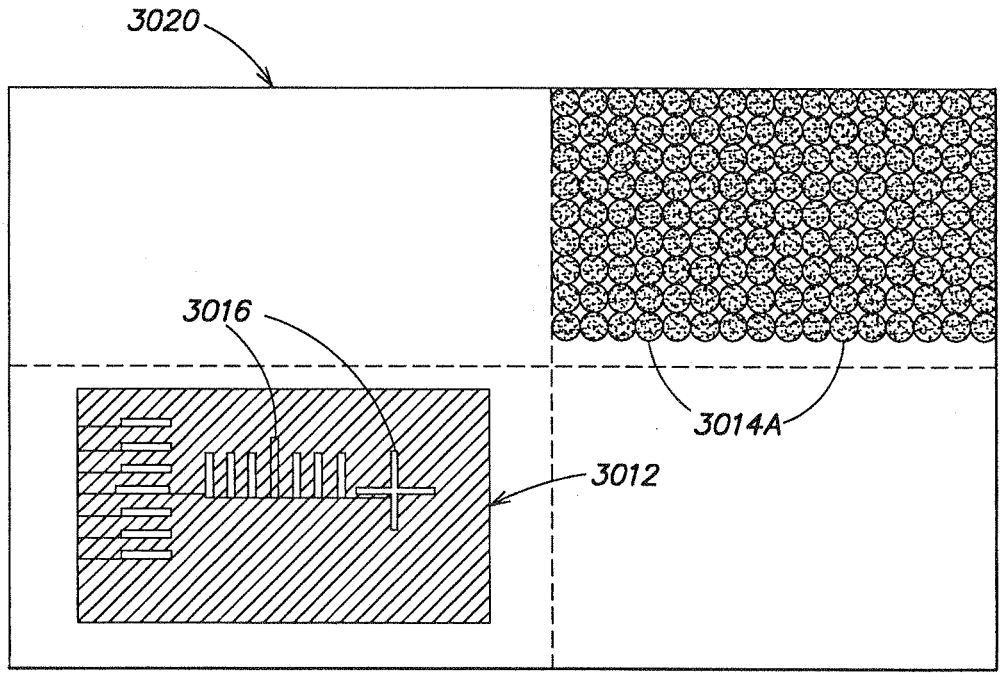


FIG. 31

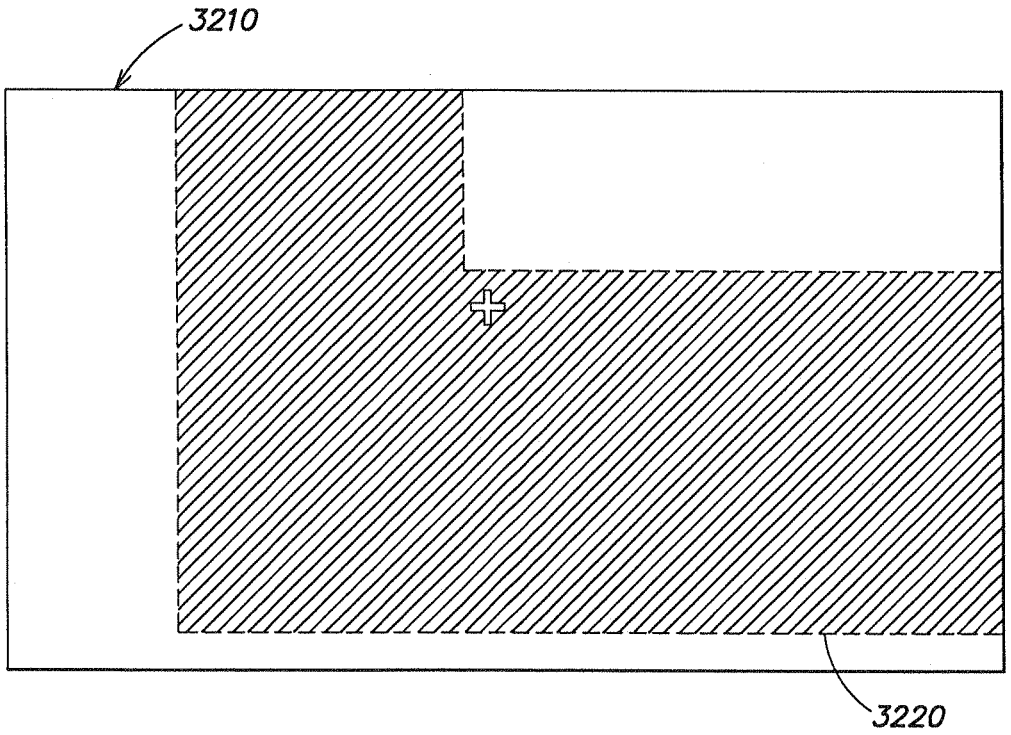


FIG. 32

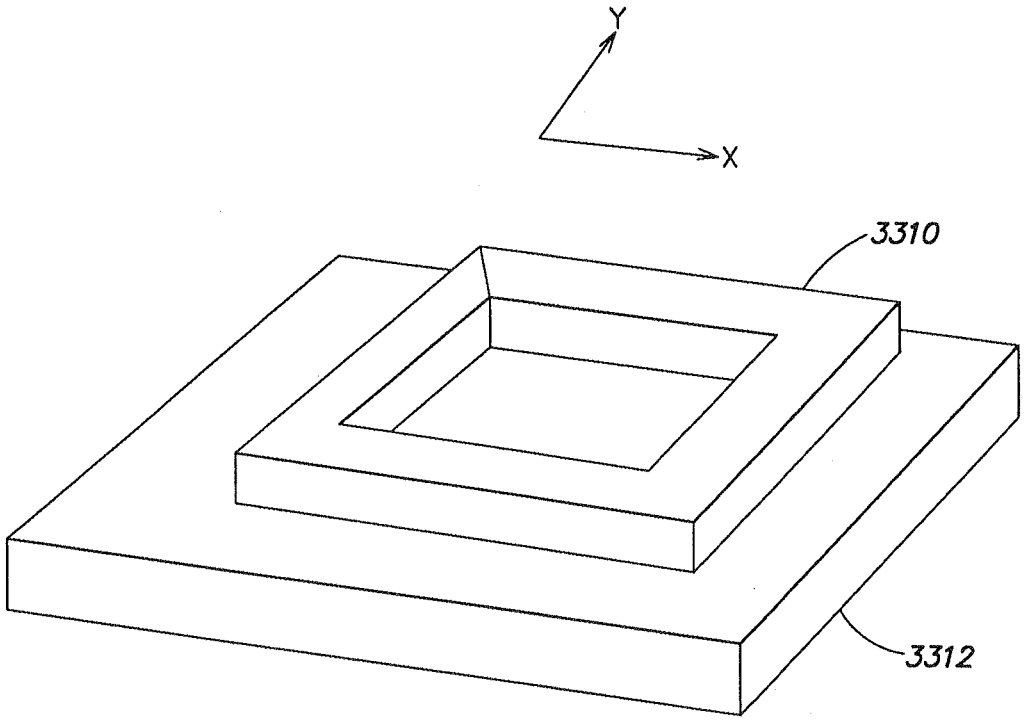


FIG. 33

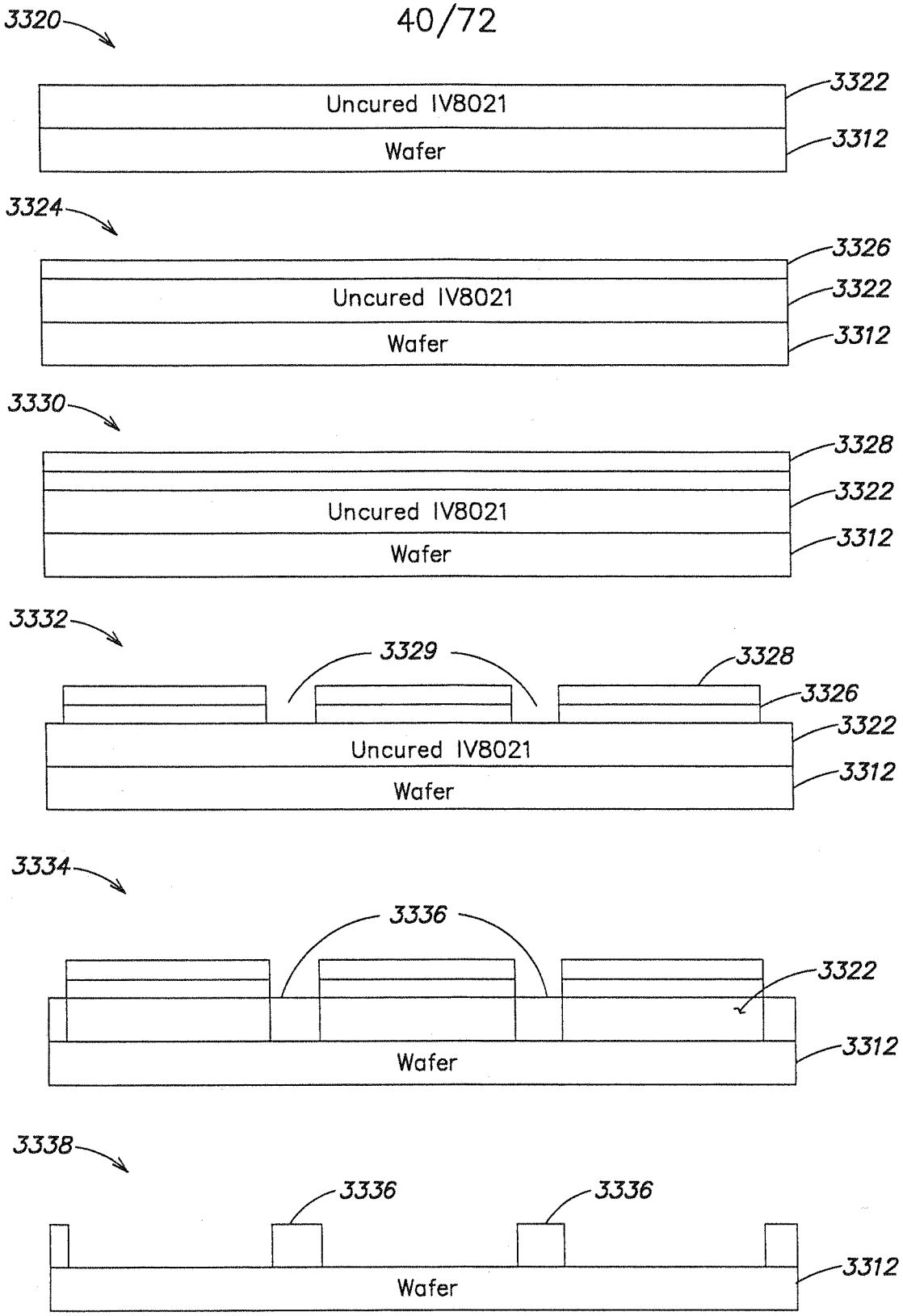

3320
Uncured IV8021
Wafer
3322
3312
3324
Uncured IV8021
Wafer
3326
3322
3312
3330
Uncured IV8021
Wafer
3328
3322
3312
3332
3329
3328
3326
Uncured IV8021
Wafer
3322
3312
3334
3336
3322
Wafer
3312
3338
3336
3336
Wafer
3312

FIG. 33A

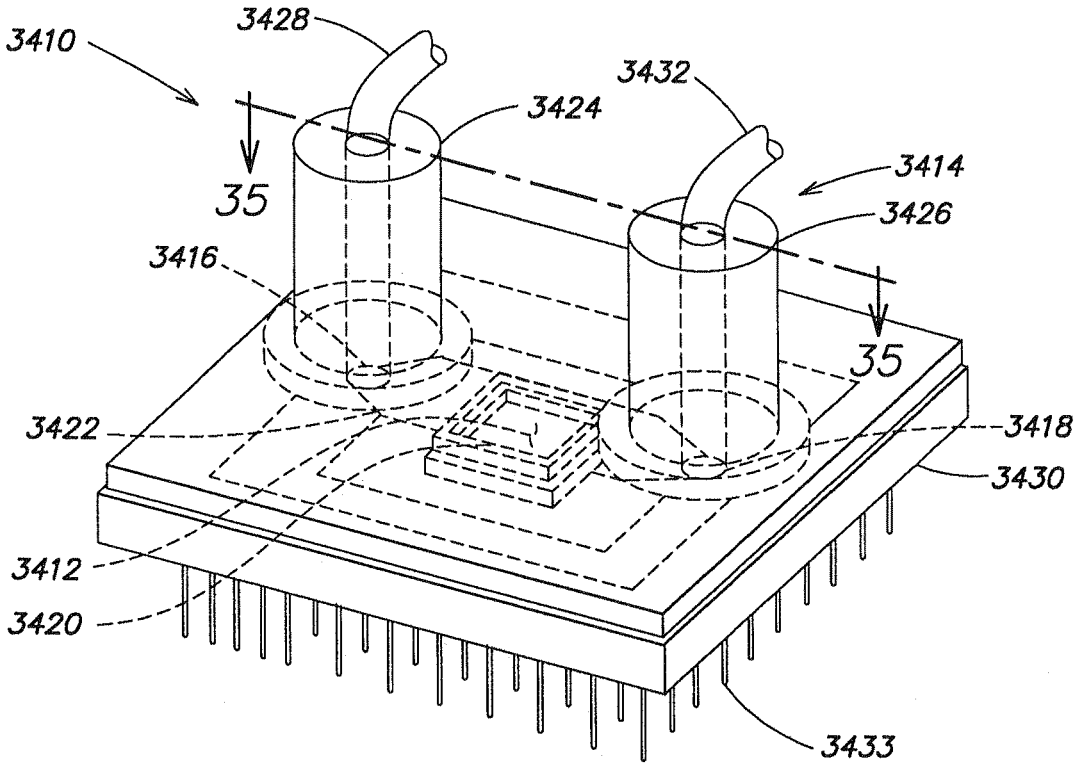

3410
3428
3432
3424
3414
35
3426
3416
35
3422
3418
3430
3412
3420
3433

FIG. 34

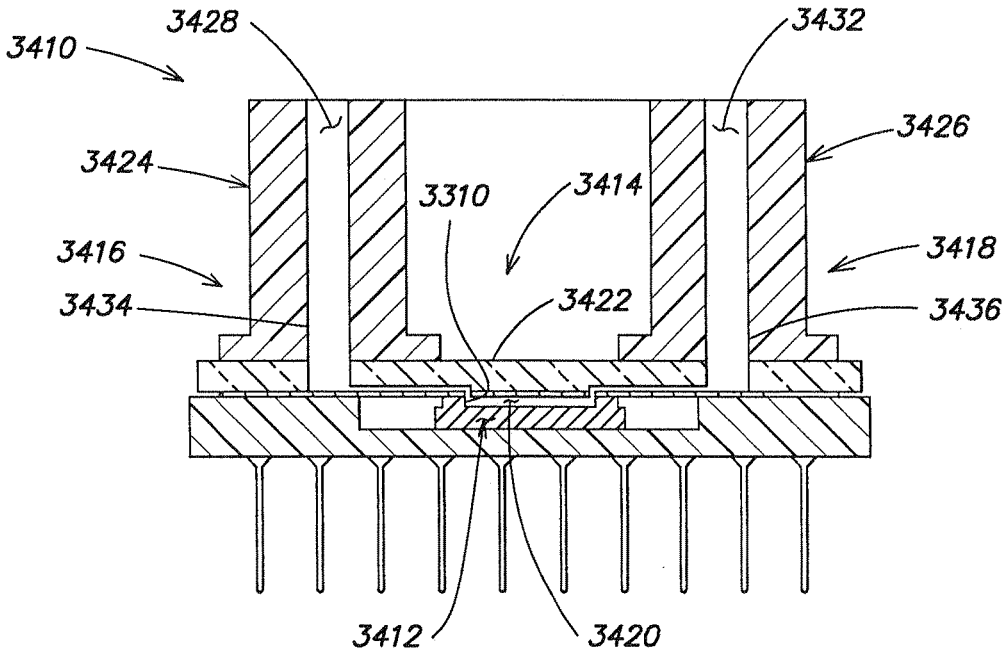

3410
3428
3432
3426
3424
3310
3414
3416
3418
3434
3422
3436
3412
3420

FIG. 35

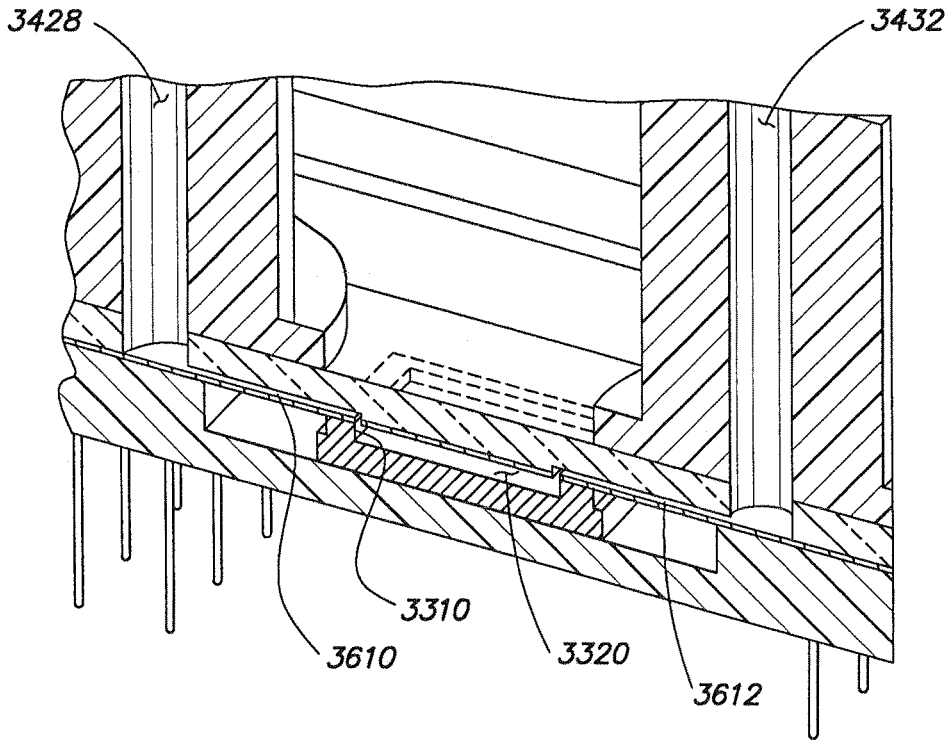

3428
3432
3310
3610
3320
3612

FIG. 36

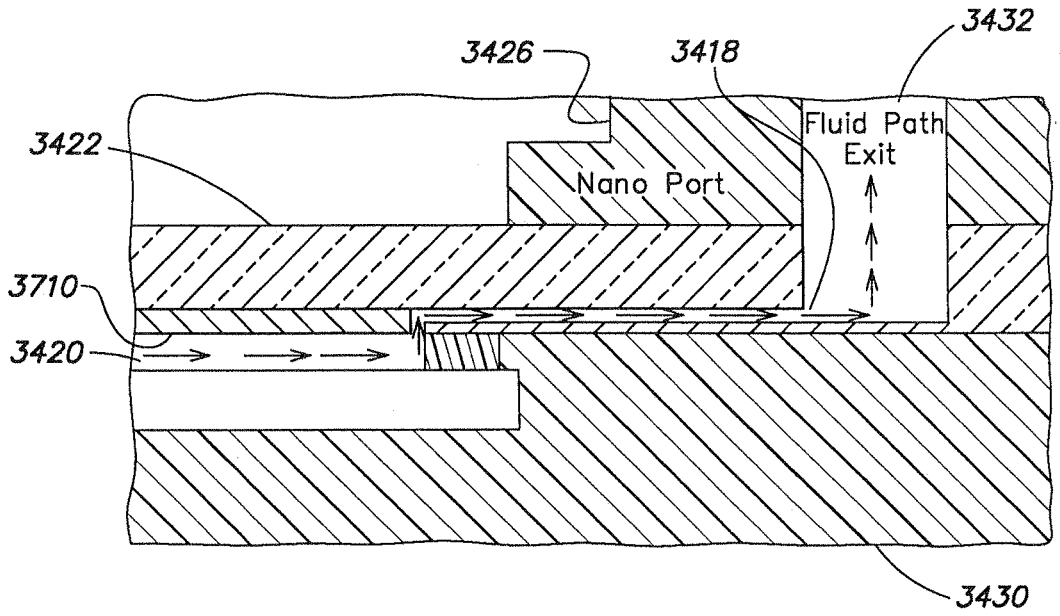


FIG. 37

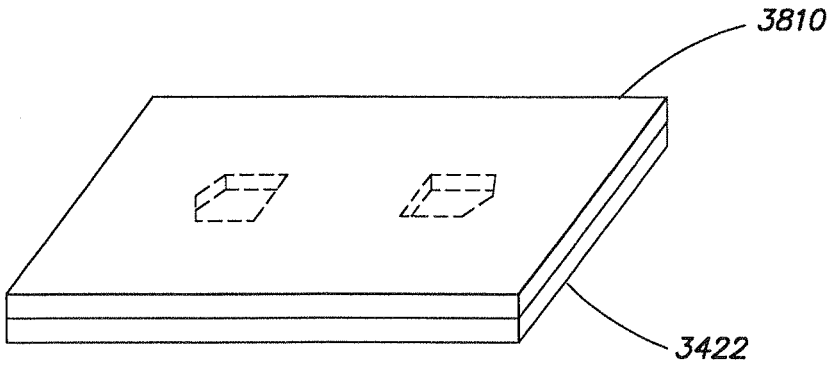


FIG. 38

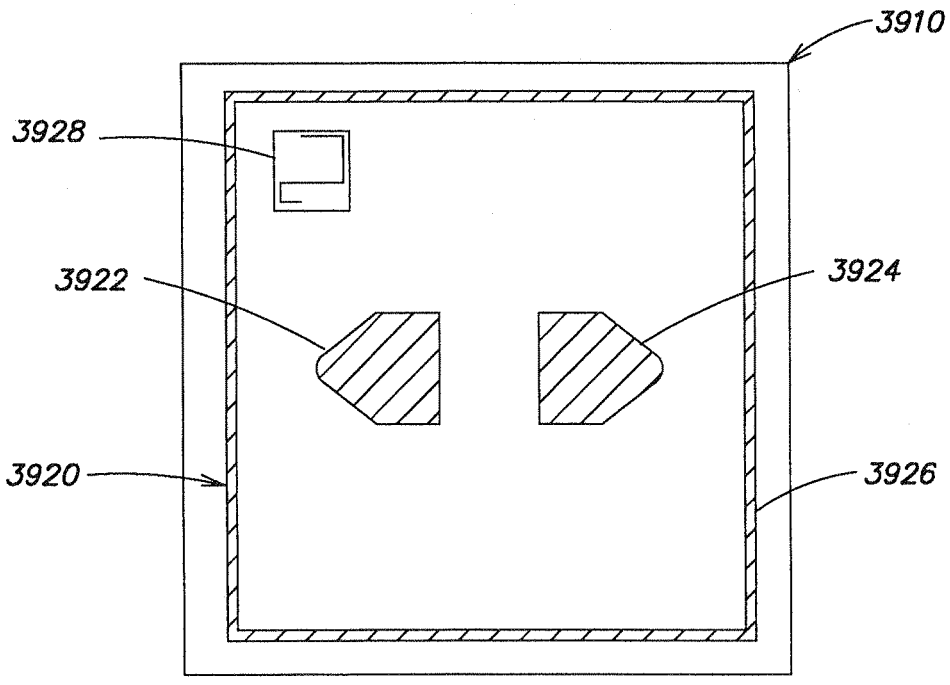


FIG. 39

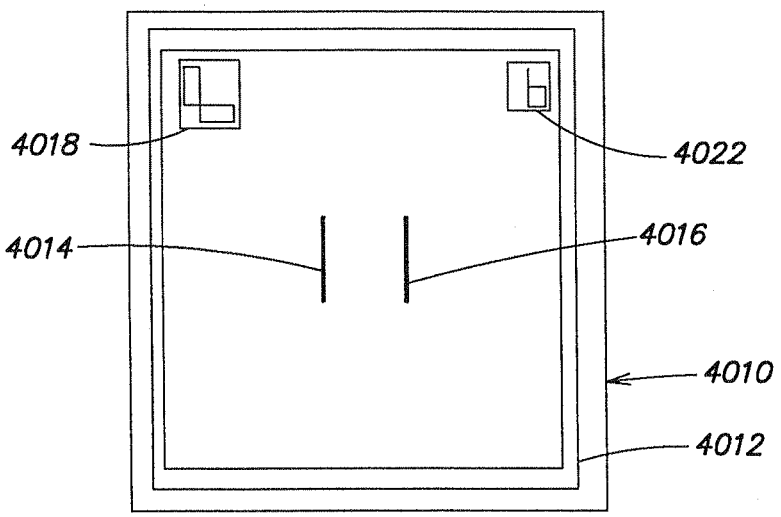


FIG. 40

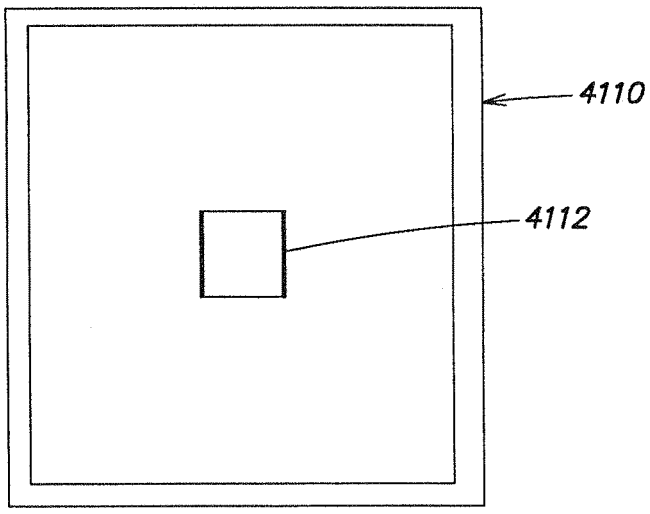


FIG. 41

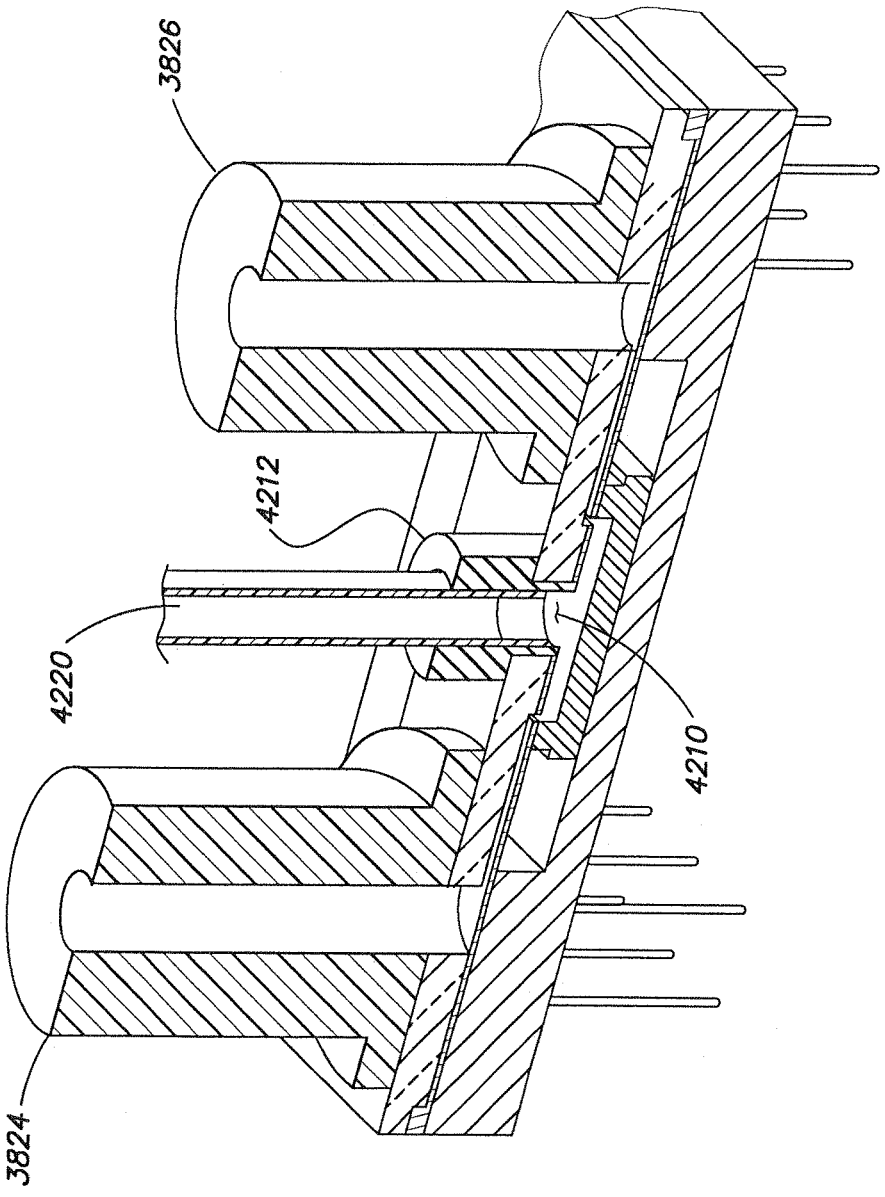


FIG. 42

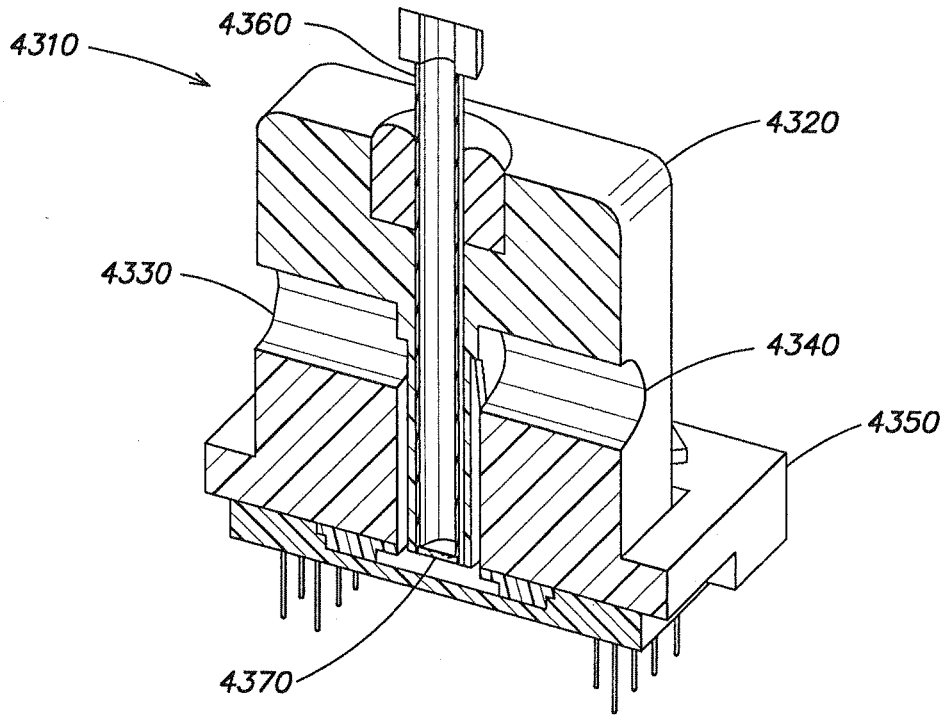


FIG. 43

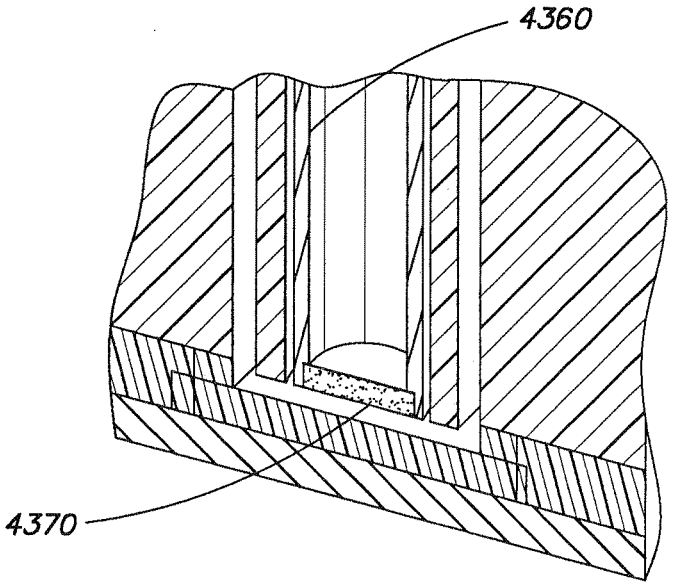


FIG. 44

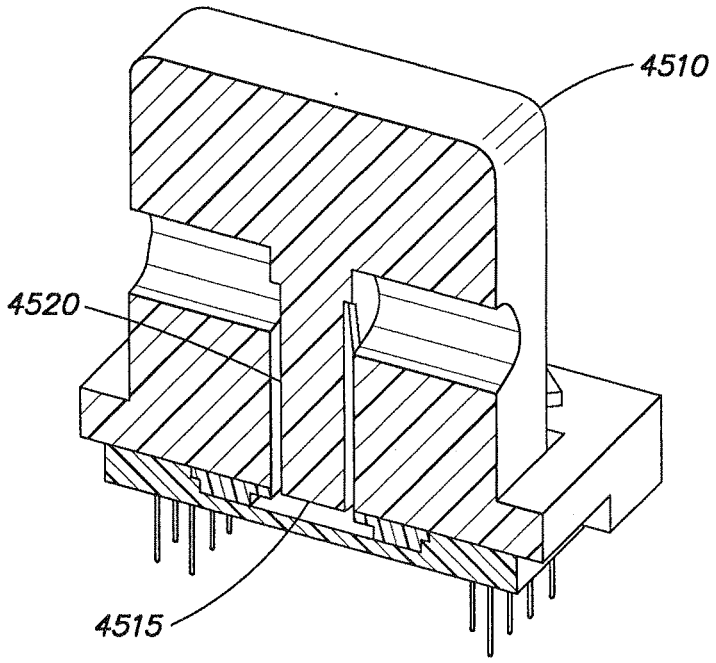


FIG. 45

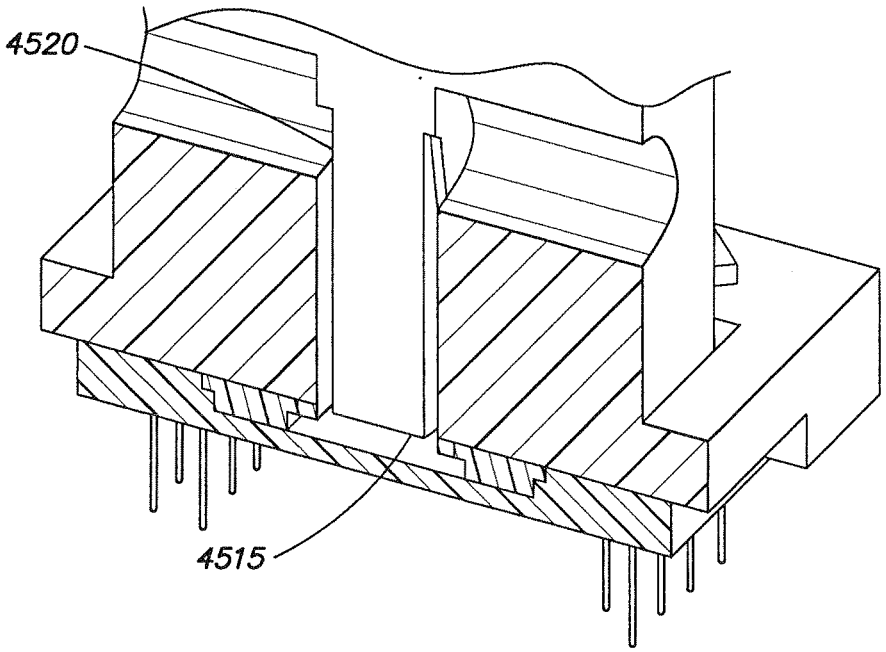


FIG. 46

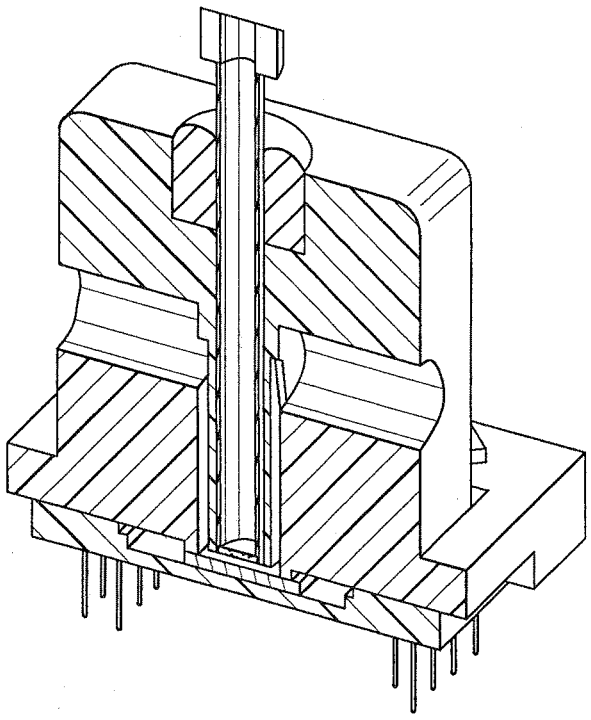


FIG. 47

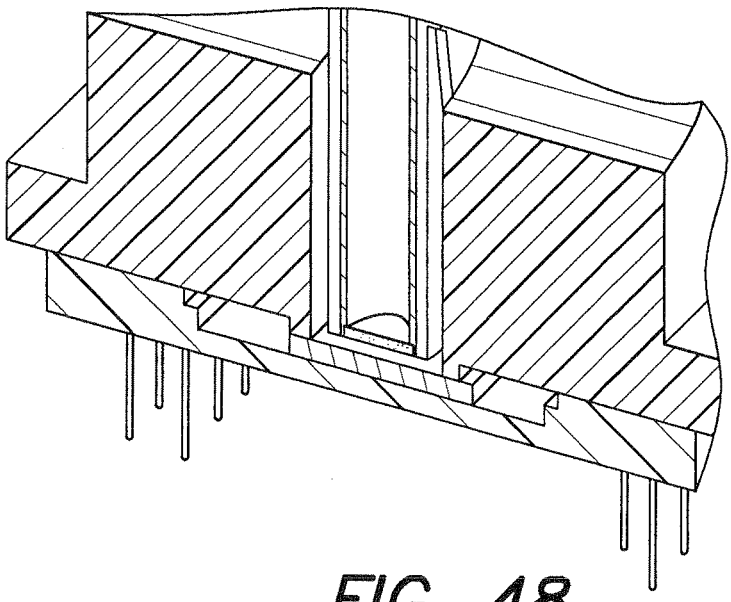


FIG. 48

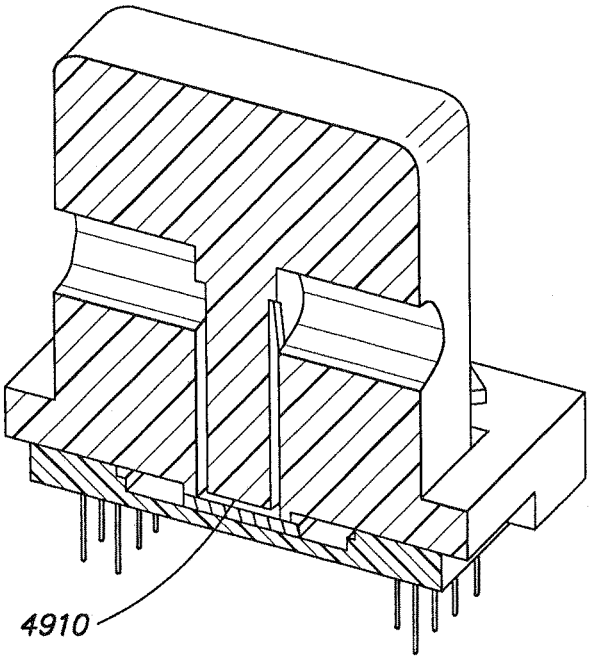


FIG. 49

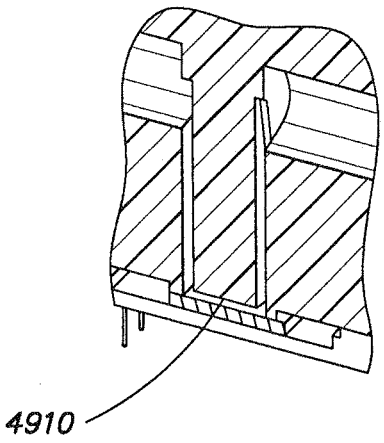


FIG. 50

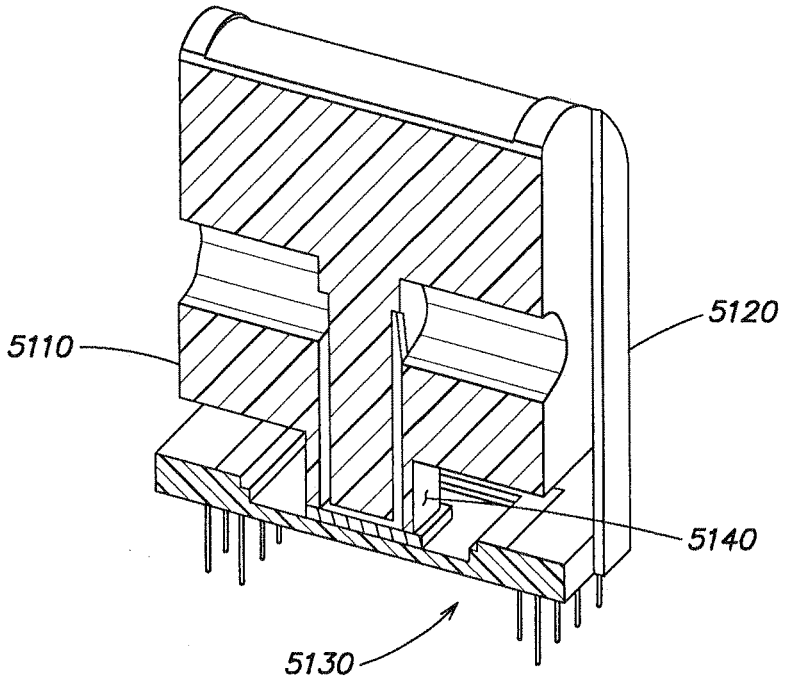


FIG. 51

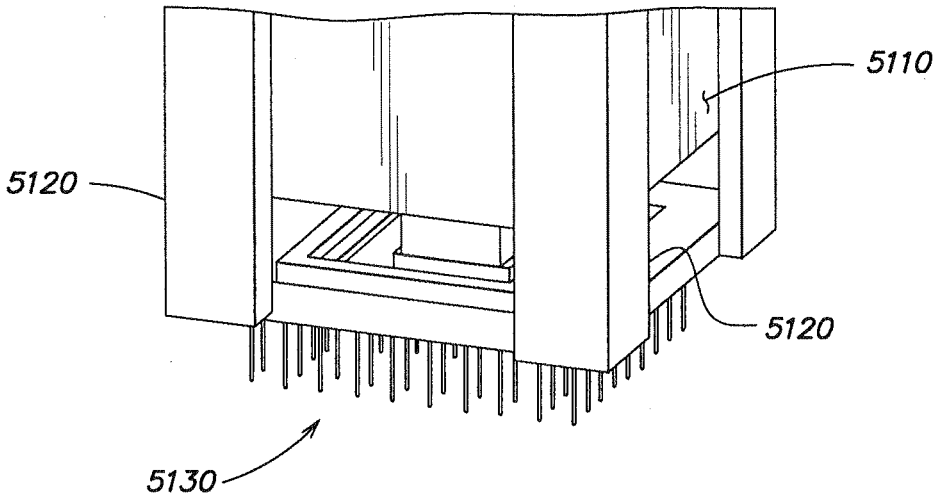


FIG. 52

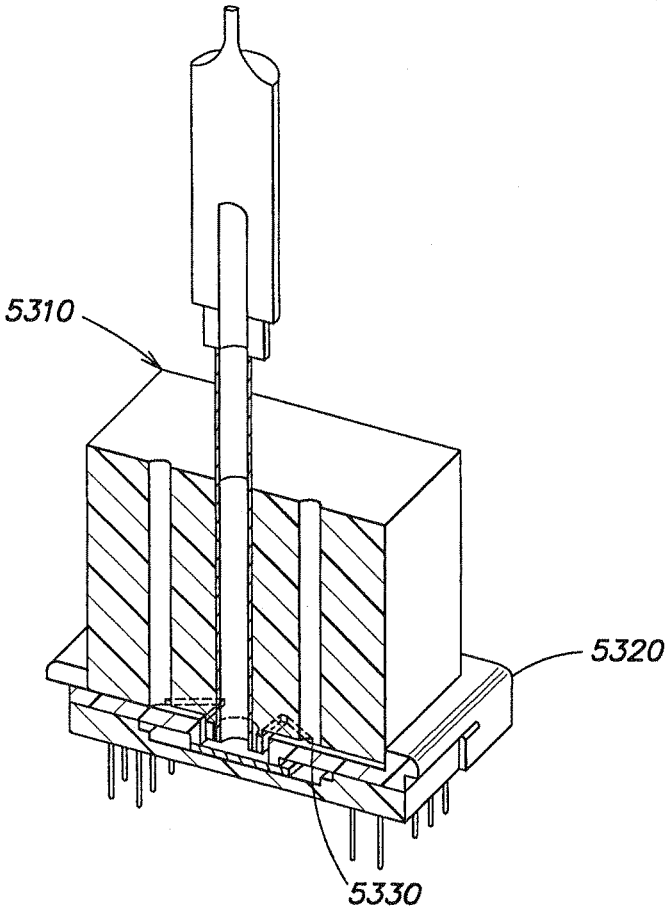


FIG. 53

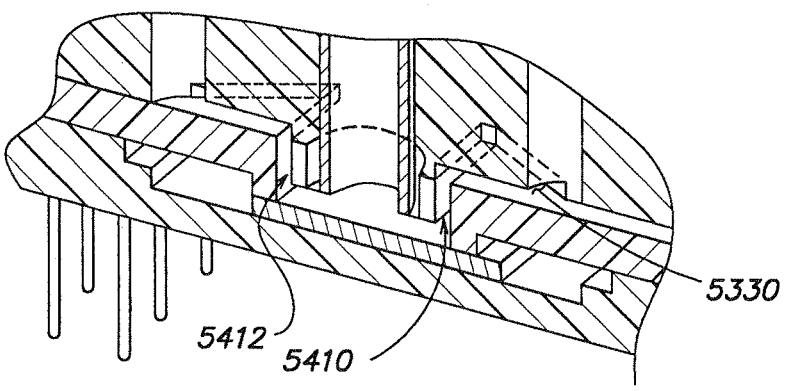


FIG. 54

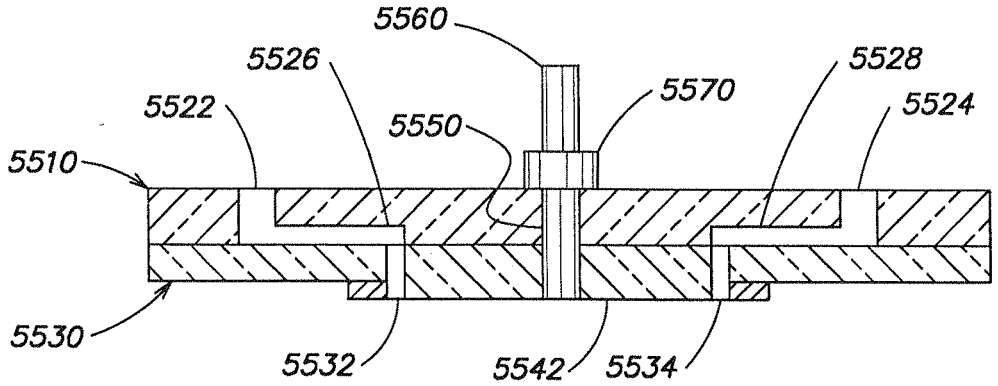

5560
5526
5528
5570
5522
5550
5524
5510
5530
5532
5542
5534

FIG. 55

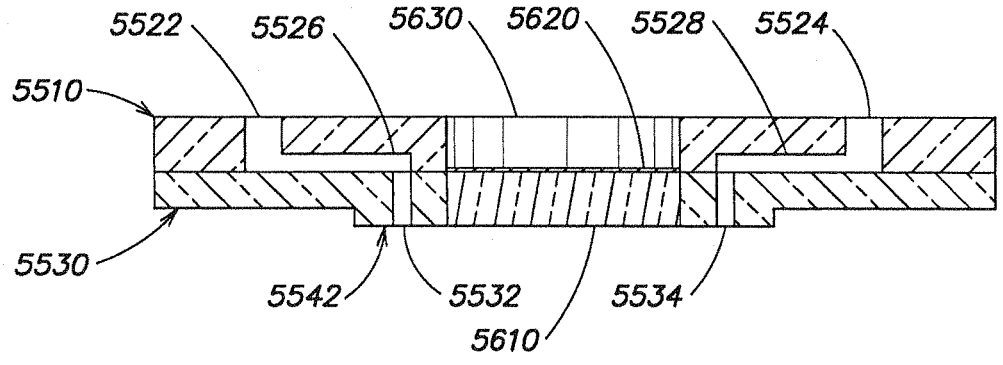

5522
5526
5630
5620
5528
5524
5510
5530
5542
5532
5534
5610

FIG. 56

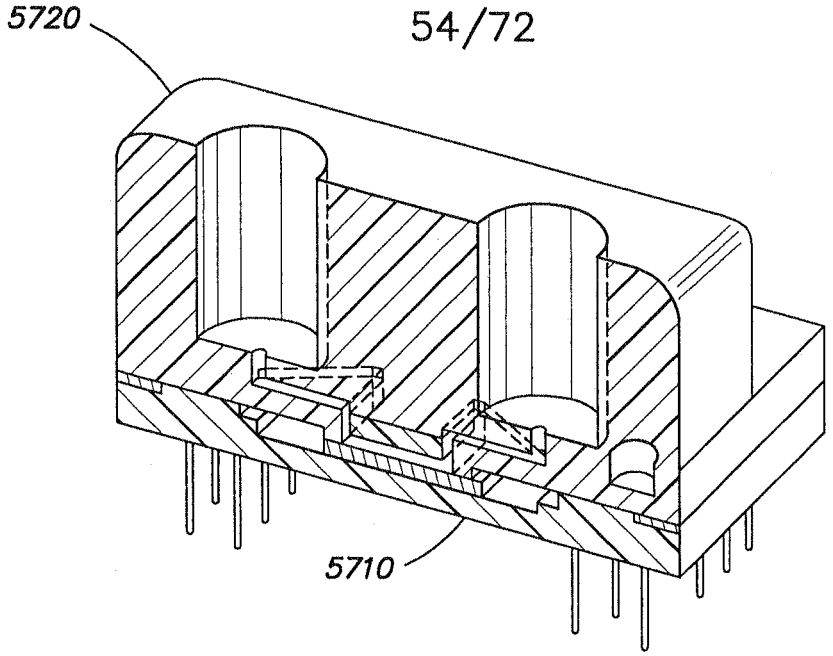


FIG. 57

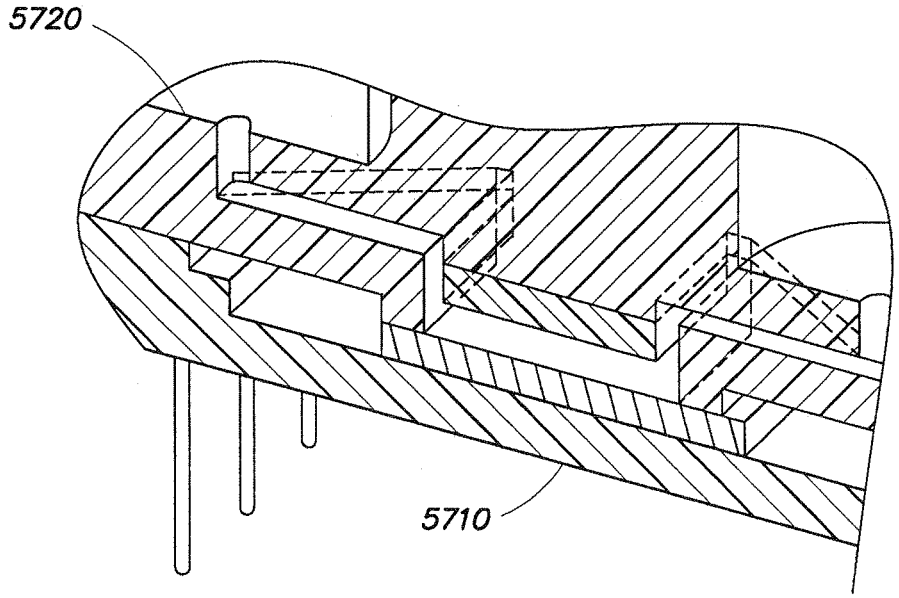


FIG. 58

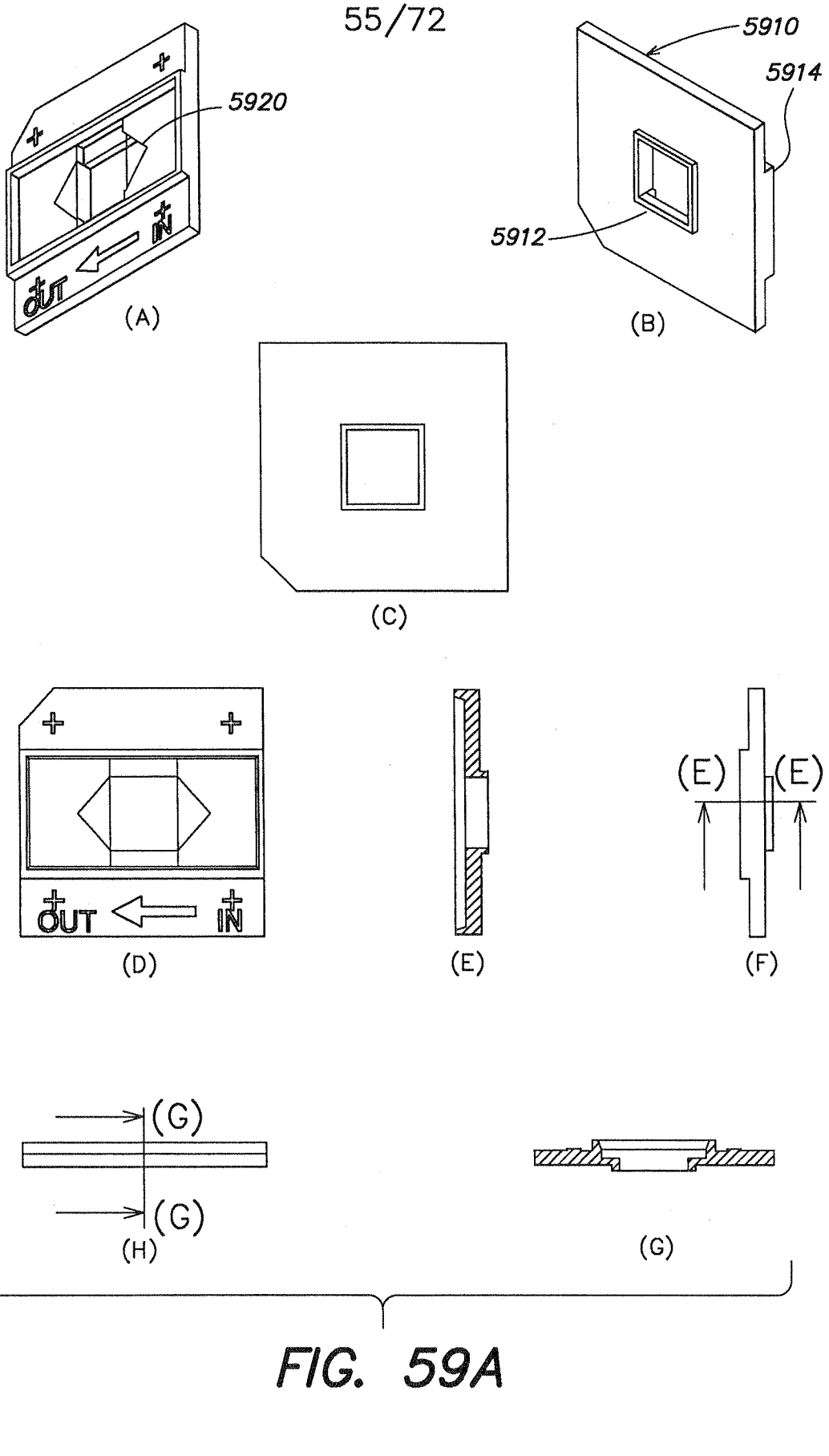


FIG. 59A

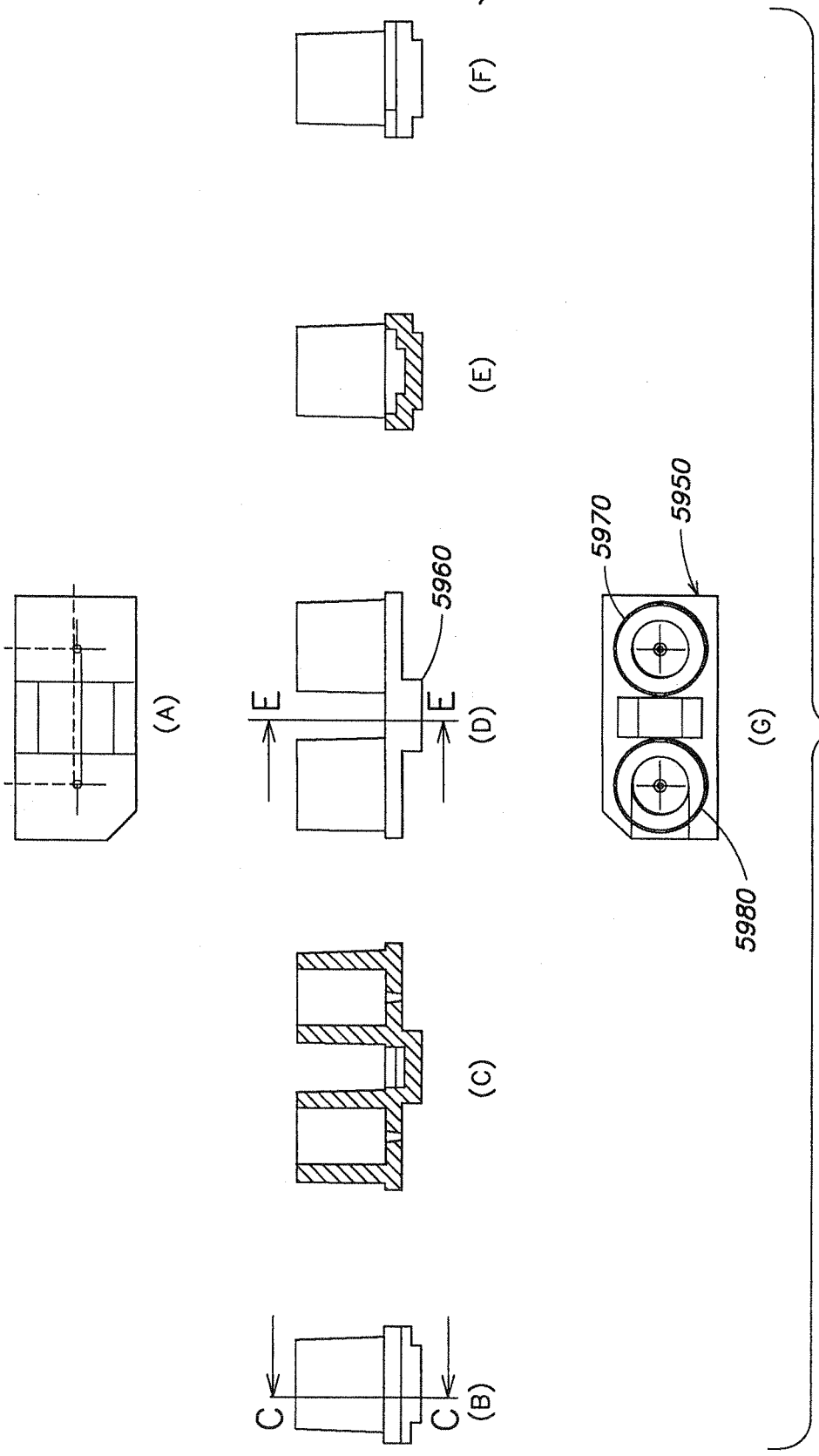
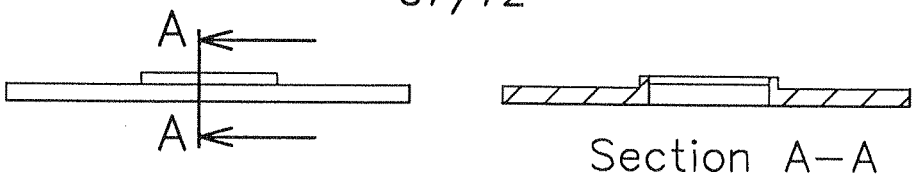
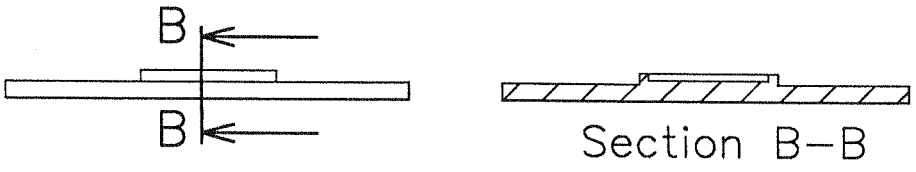


FIG. 59B





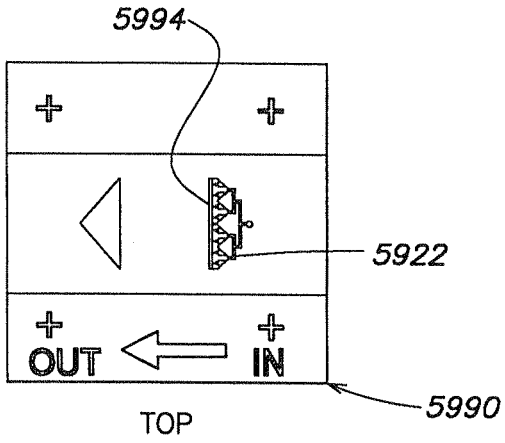


FIG. 59C

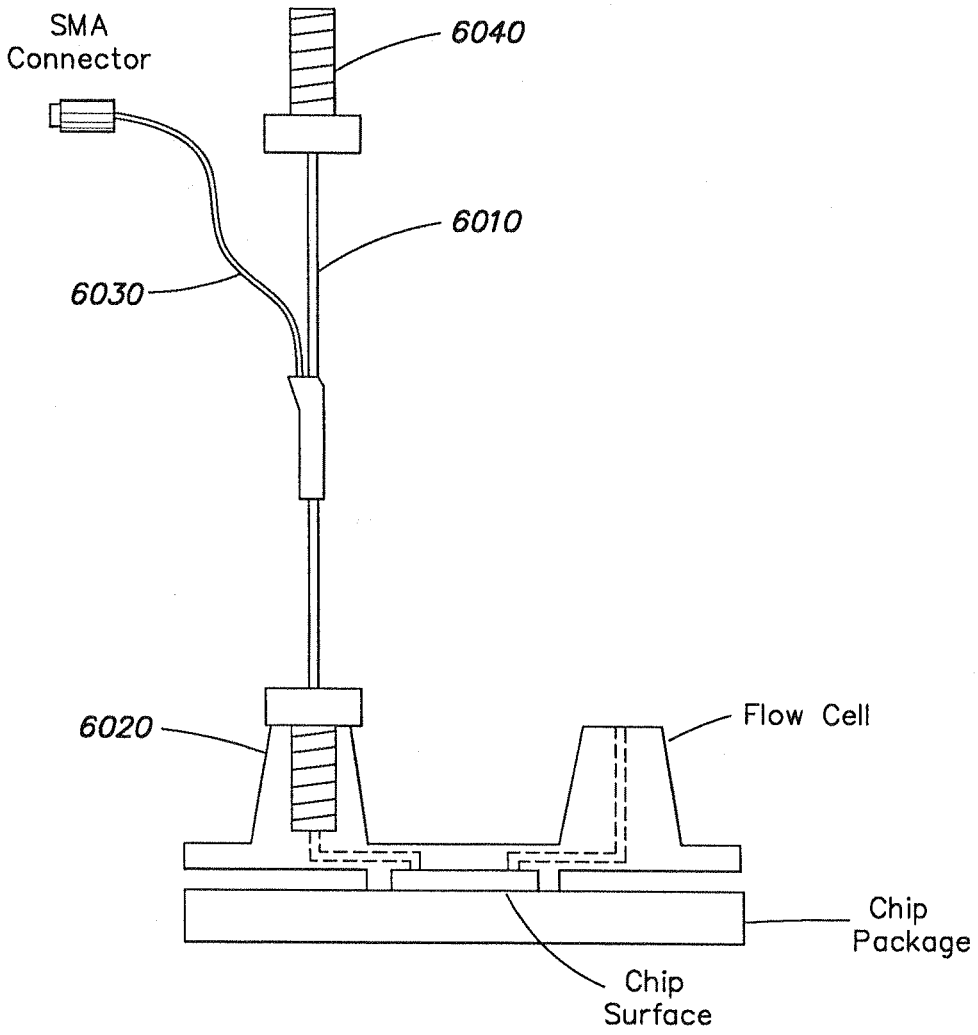

SMA
Connector
6040
6010
6030
6020
Flow Cell
Chip
Package
Chip
Surface

FIG. 60

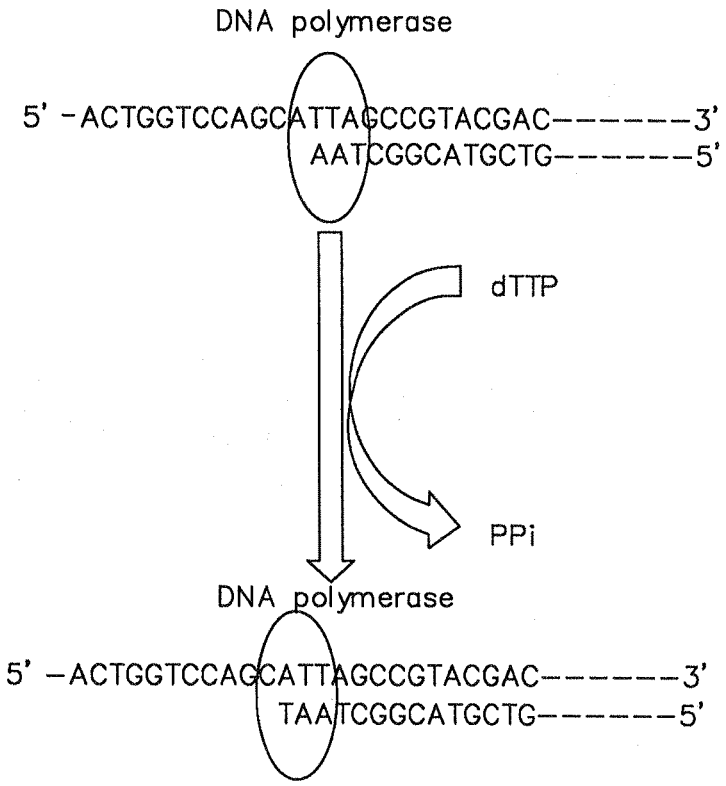

DNA polymerase
5' -ACTGGTCCAGCATTAGCCGTACGAC------3'
AATCGGCATGCTG------5'
dTTP
PPi
DNA polymerase
5' -ACTGGTCCAGCATTAGCCGTACGAC------3'
TAATCGGCATGCTG------5'

FIG. 61

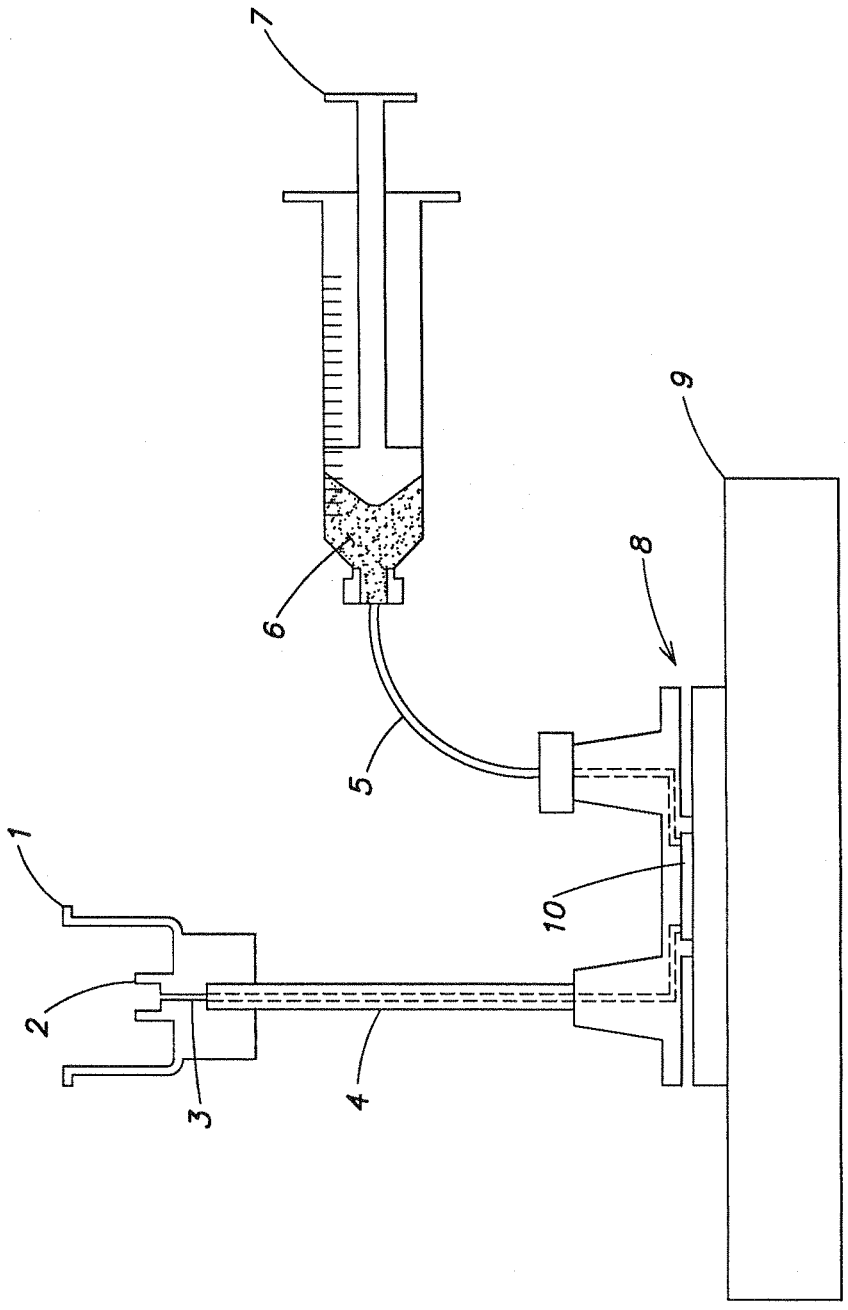


FIG. 62

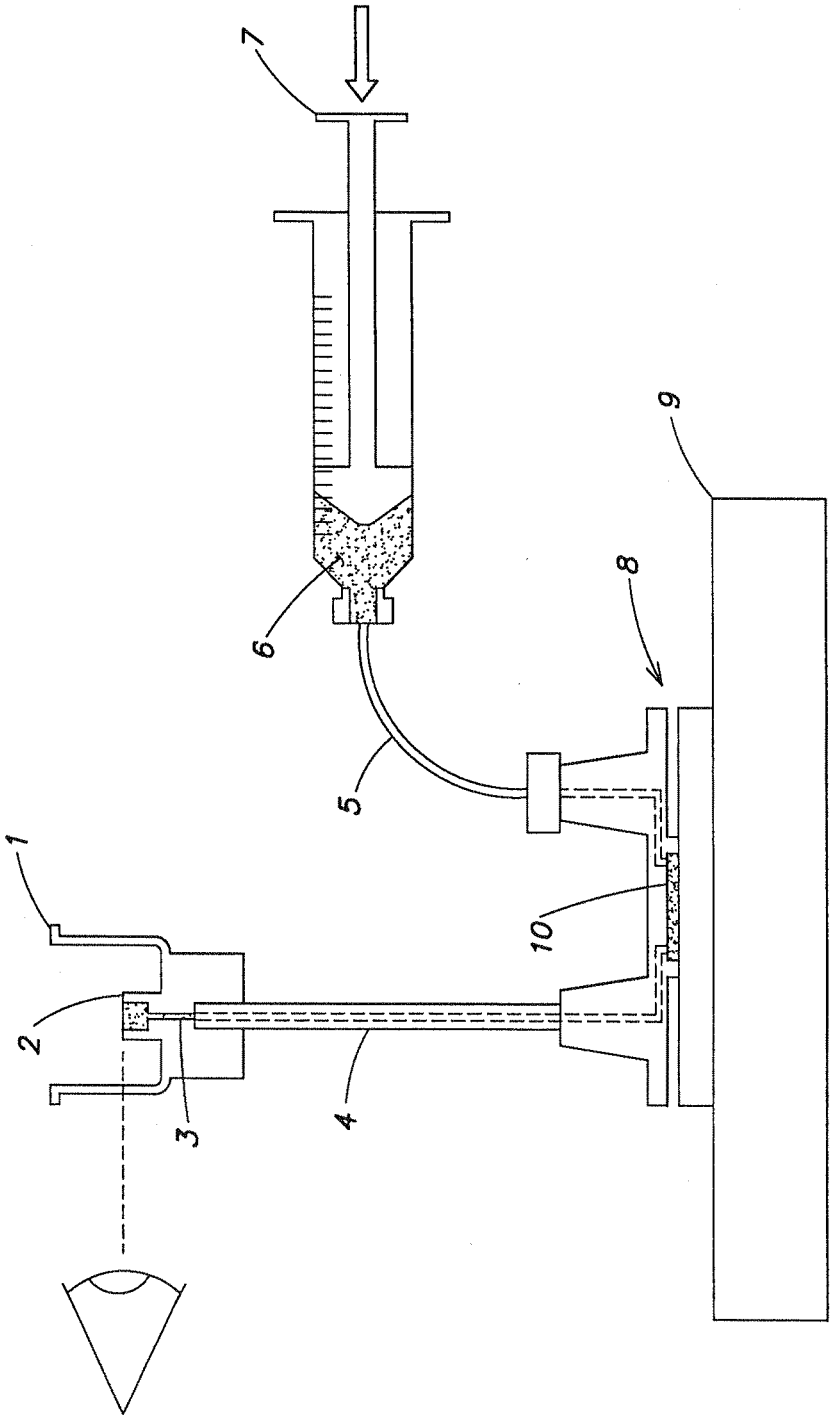


FIG. 63

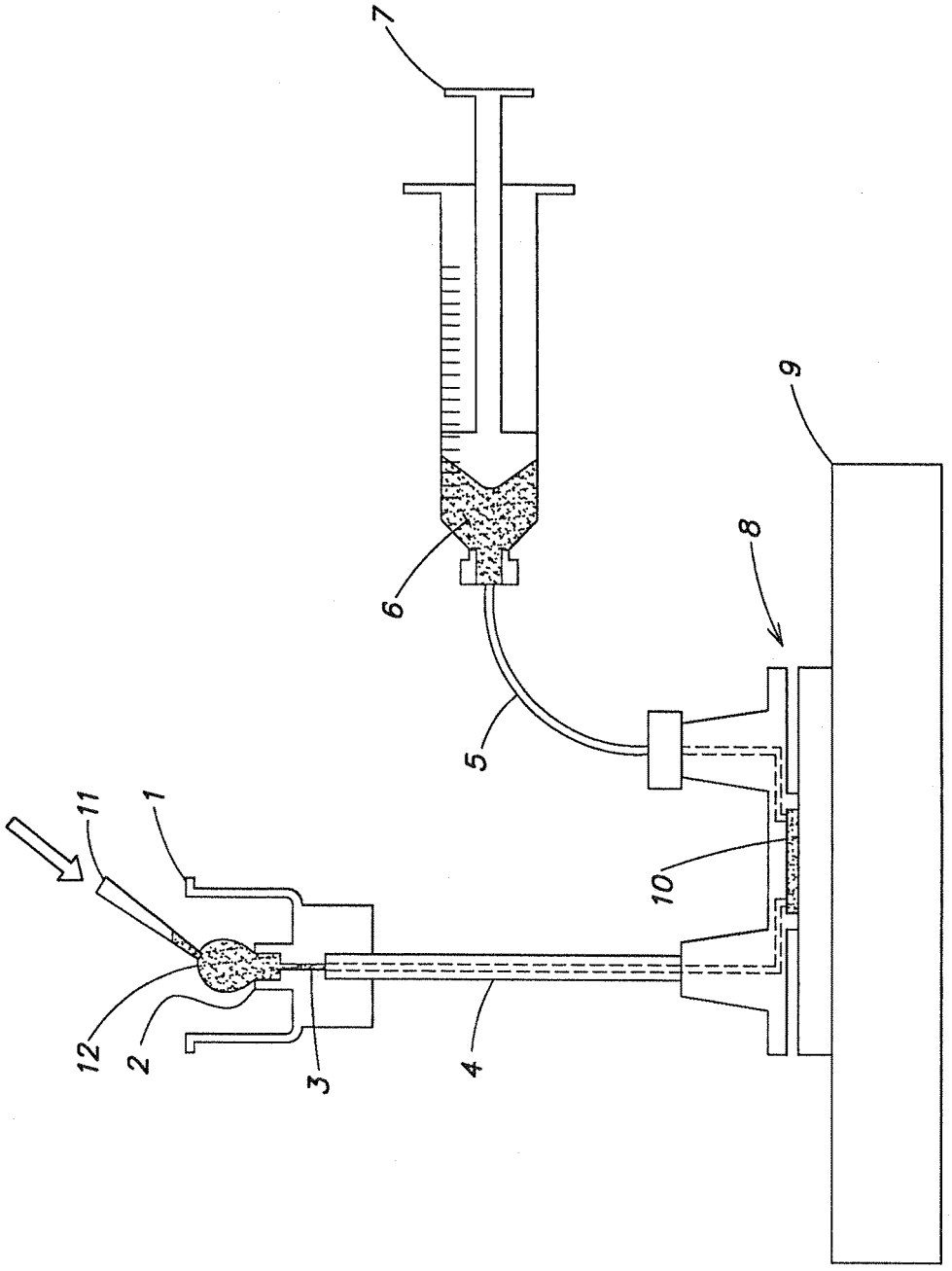


FIG. 64

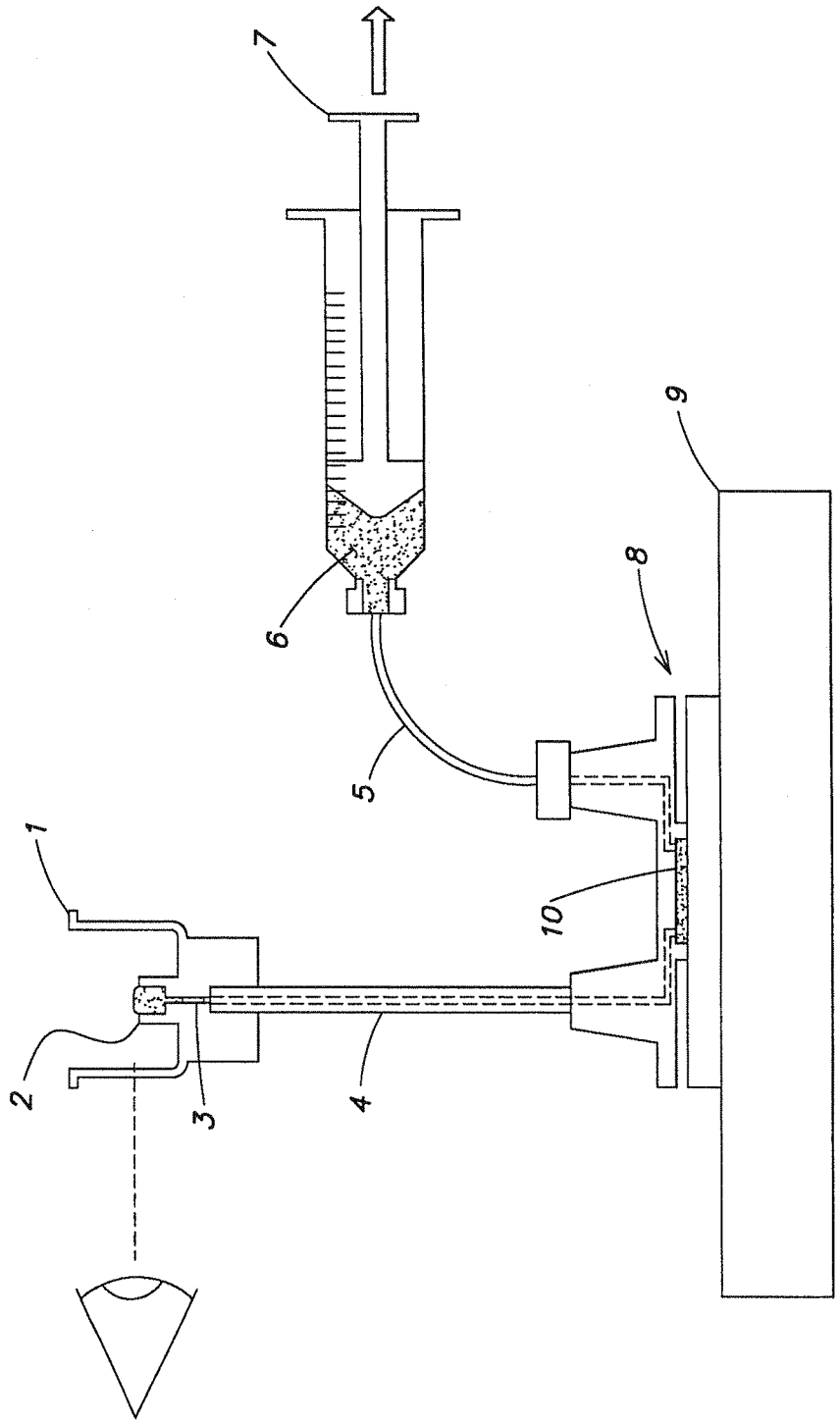


FIG. 65

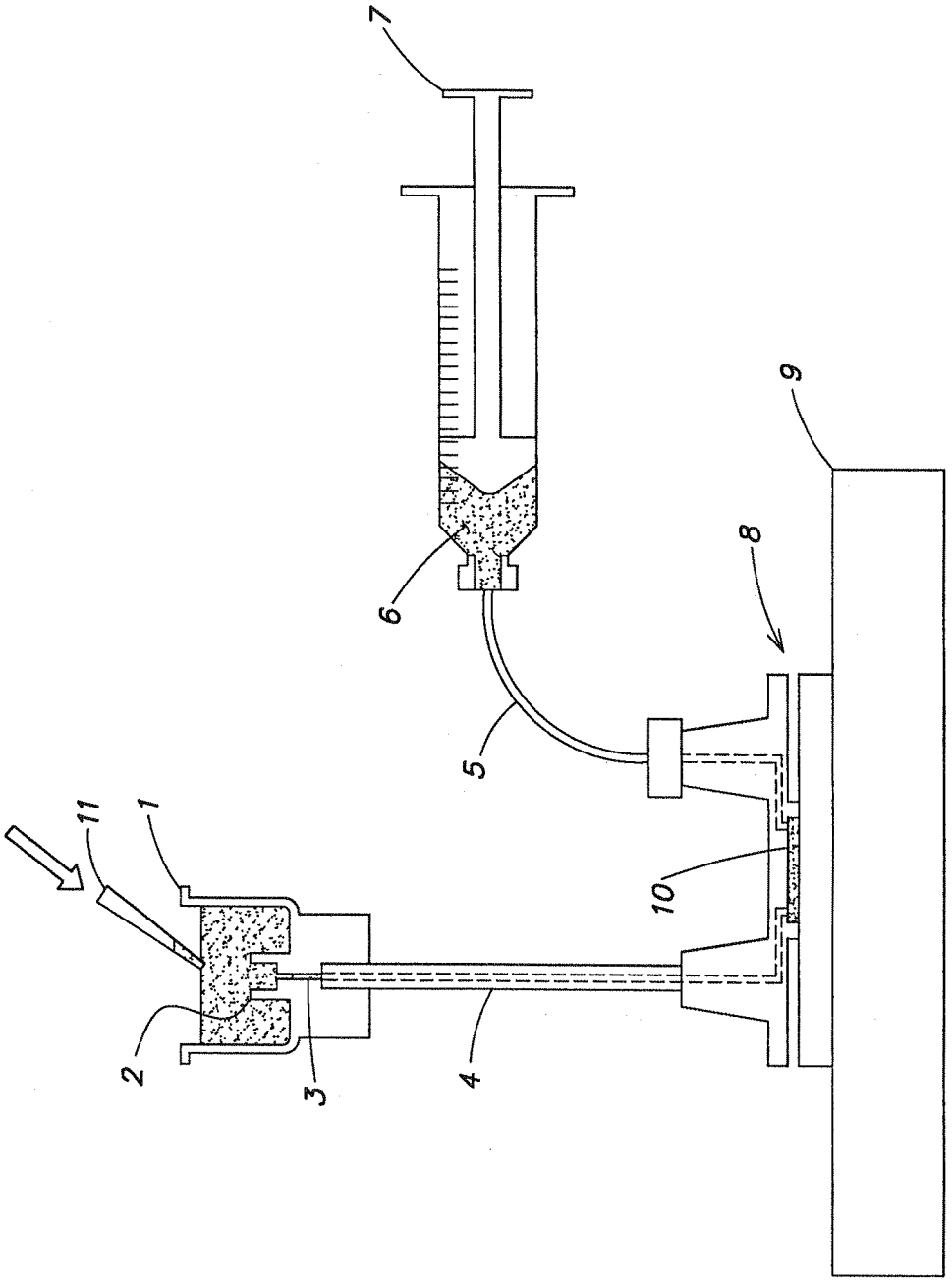


FIG. 66

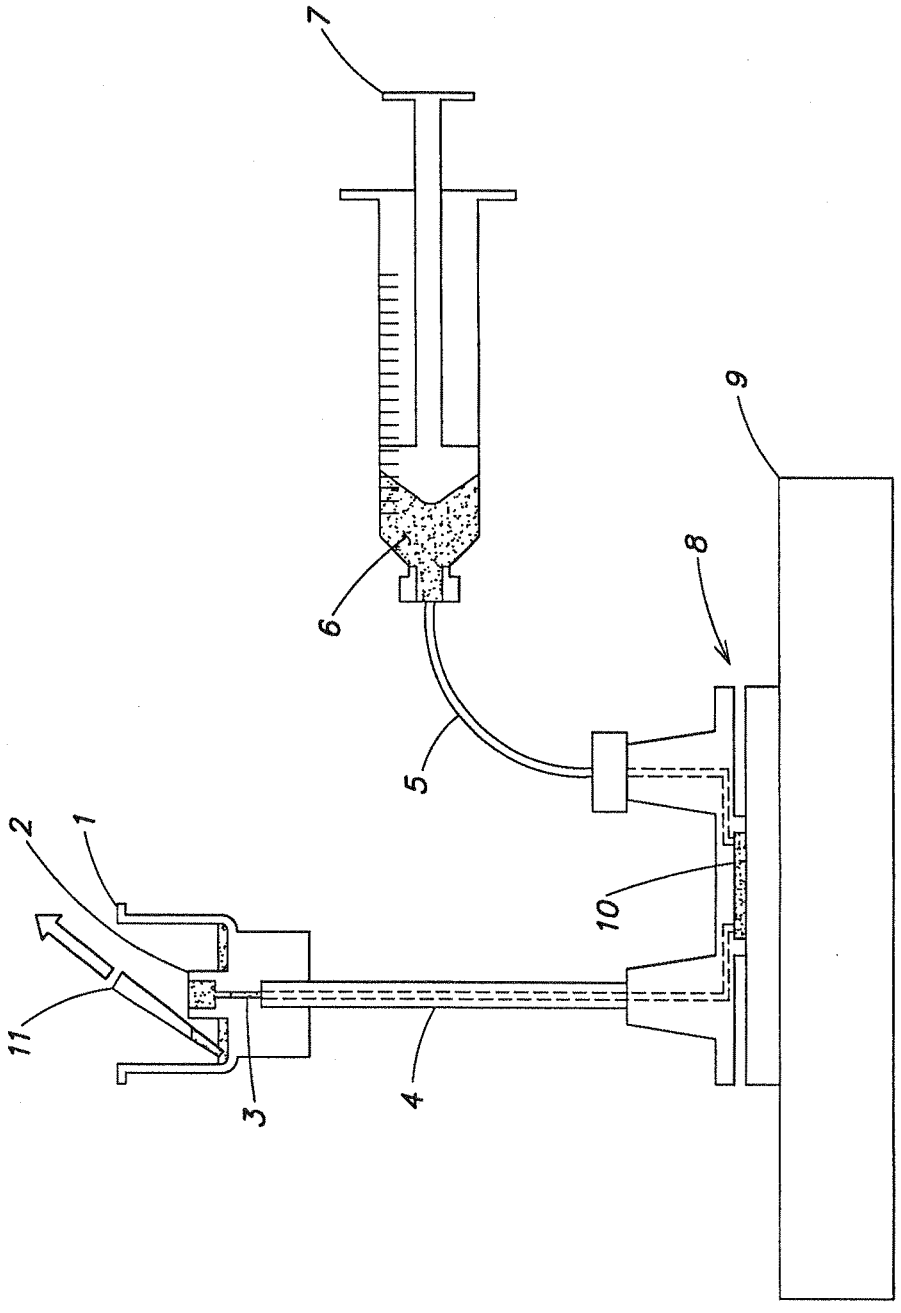


FIG. 67

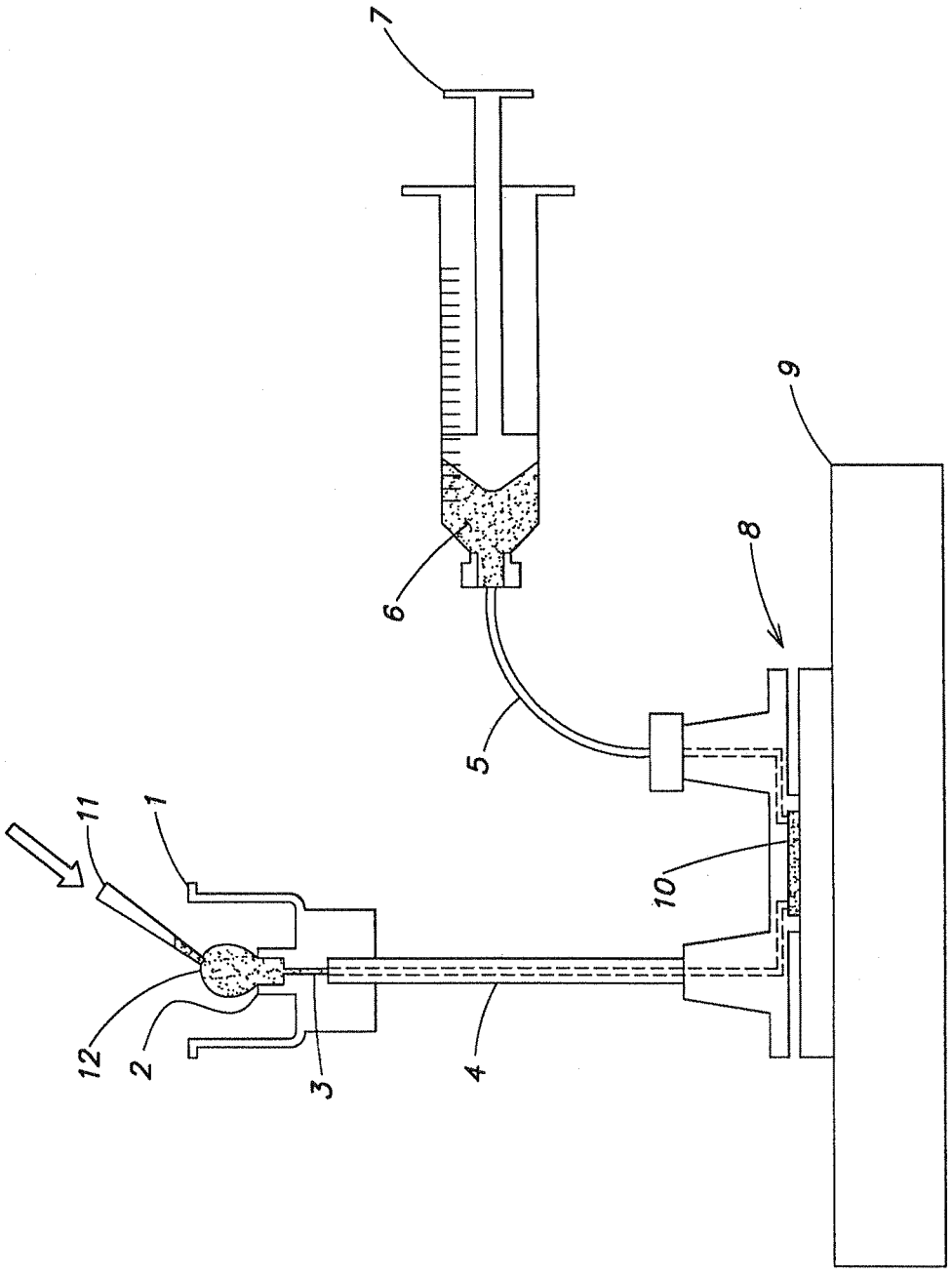


FIG. 68

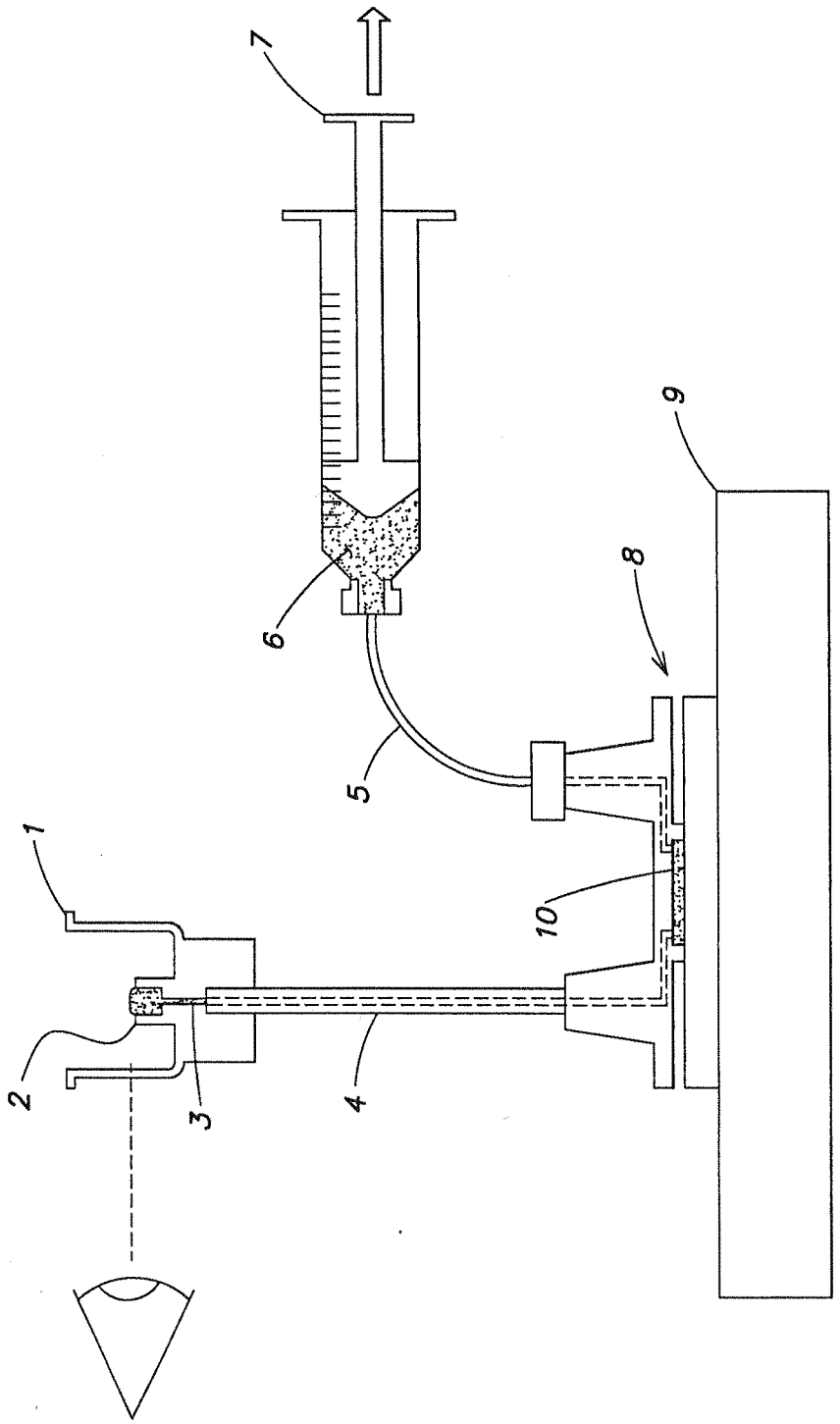


FIG. 69

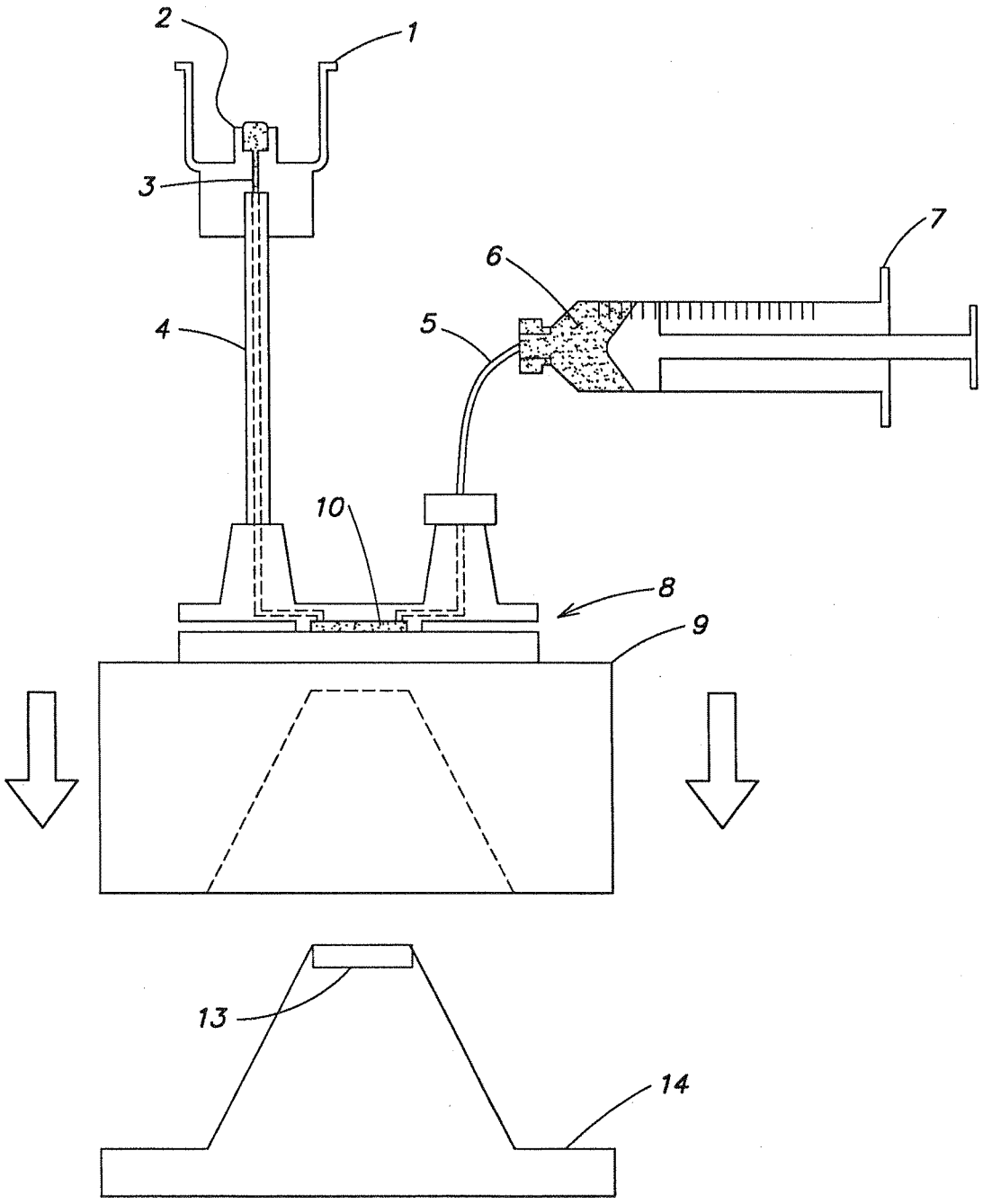


FIG. 70

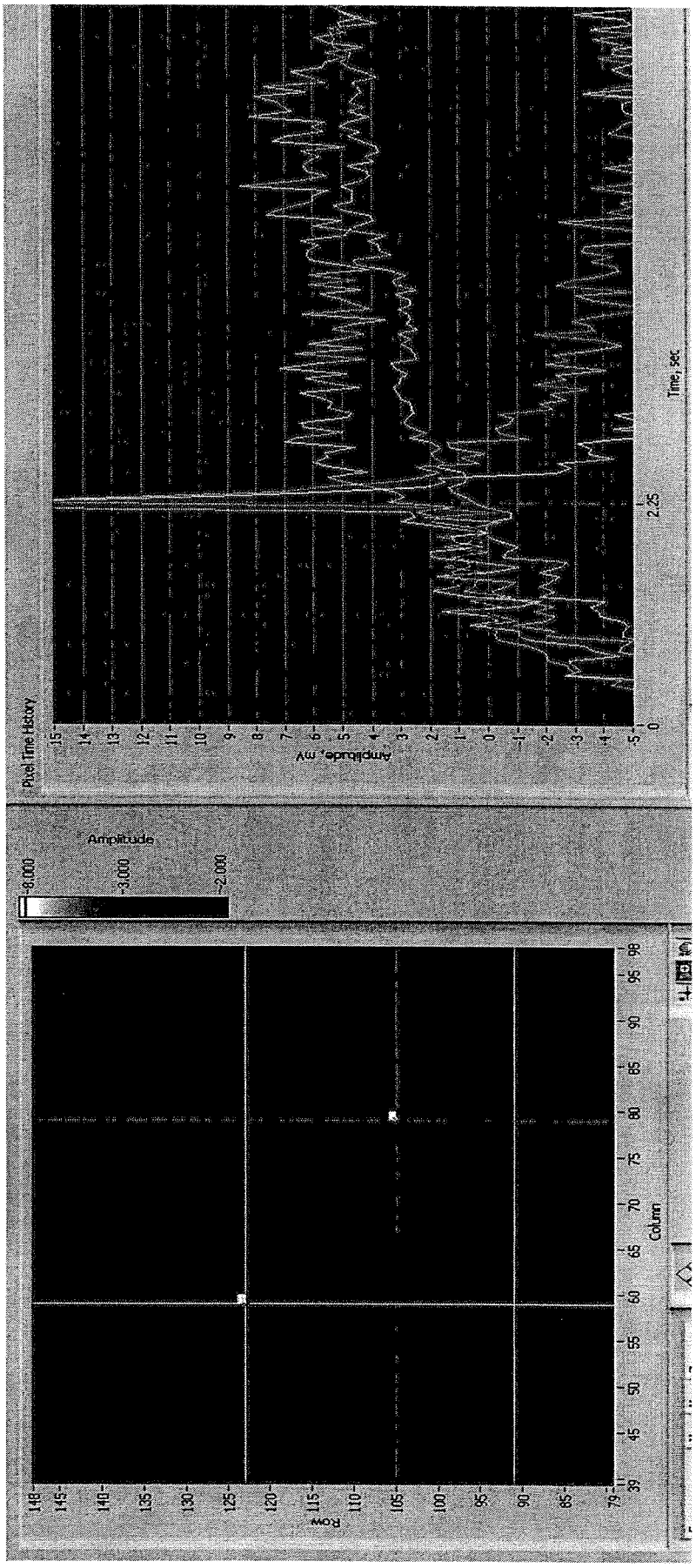

Pixel Time History
Amplitude, mV
Time, sec
Amplitude
-8.000
-3.000
-2.000
Row
Column

FIG. 71A

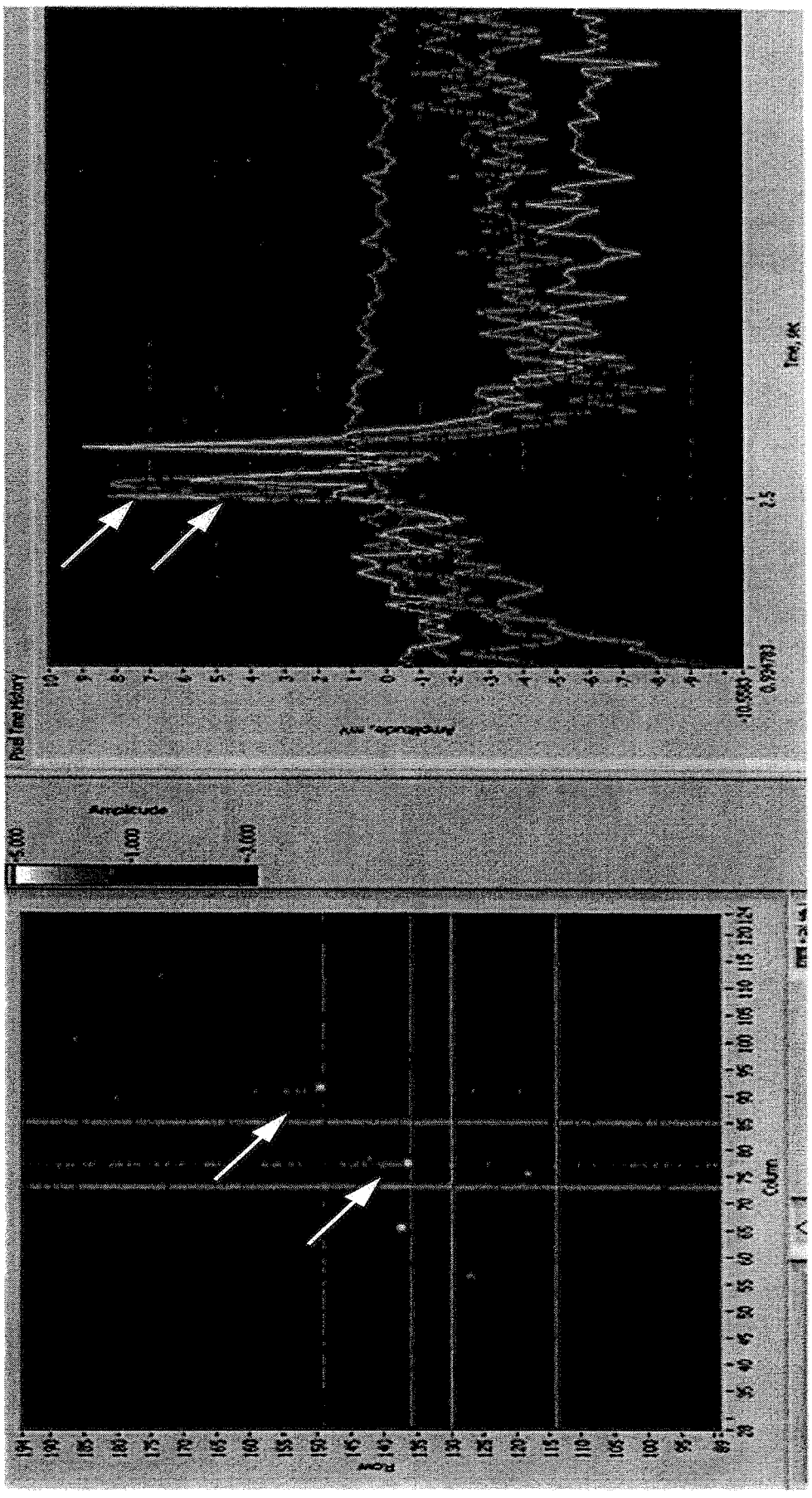


FIG. 71B

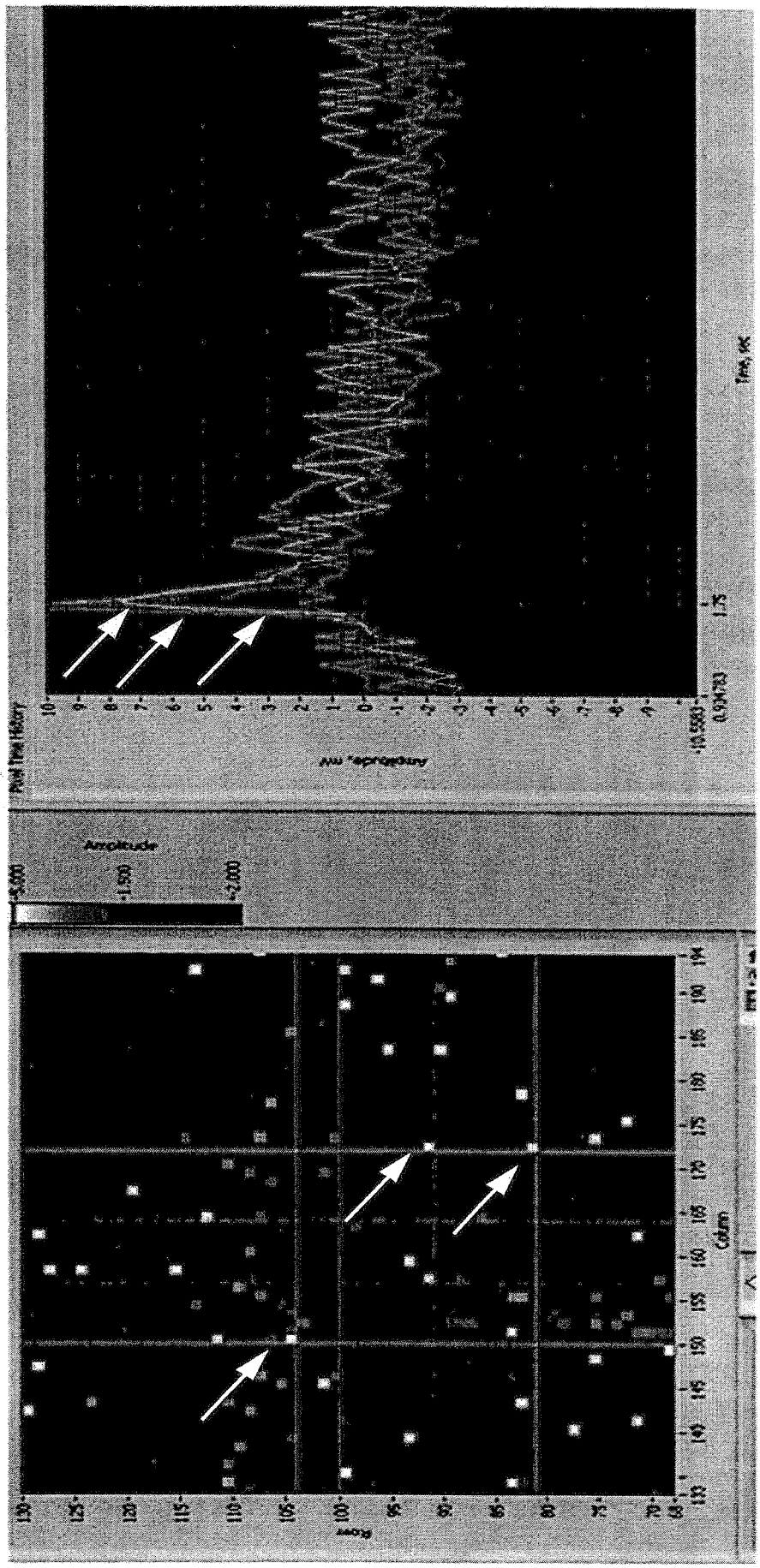

Pixel Time History
Amplitude
Amplitude, mV
Time, sec
Amplitude
+5.000
+1.550
+2.000
Range
Cross

FIG. 71C

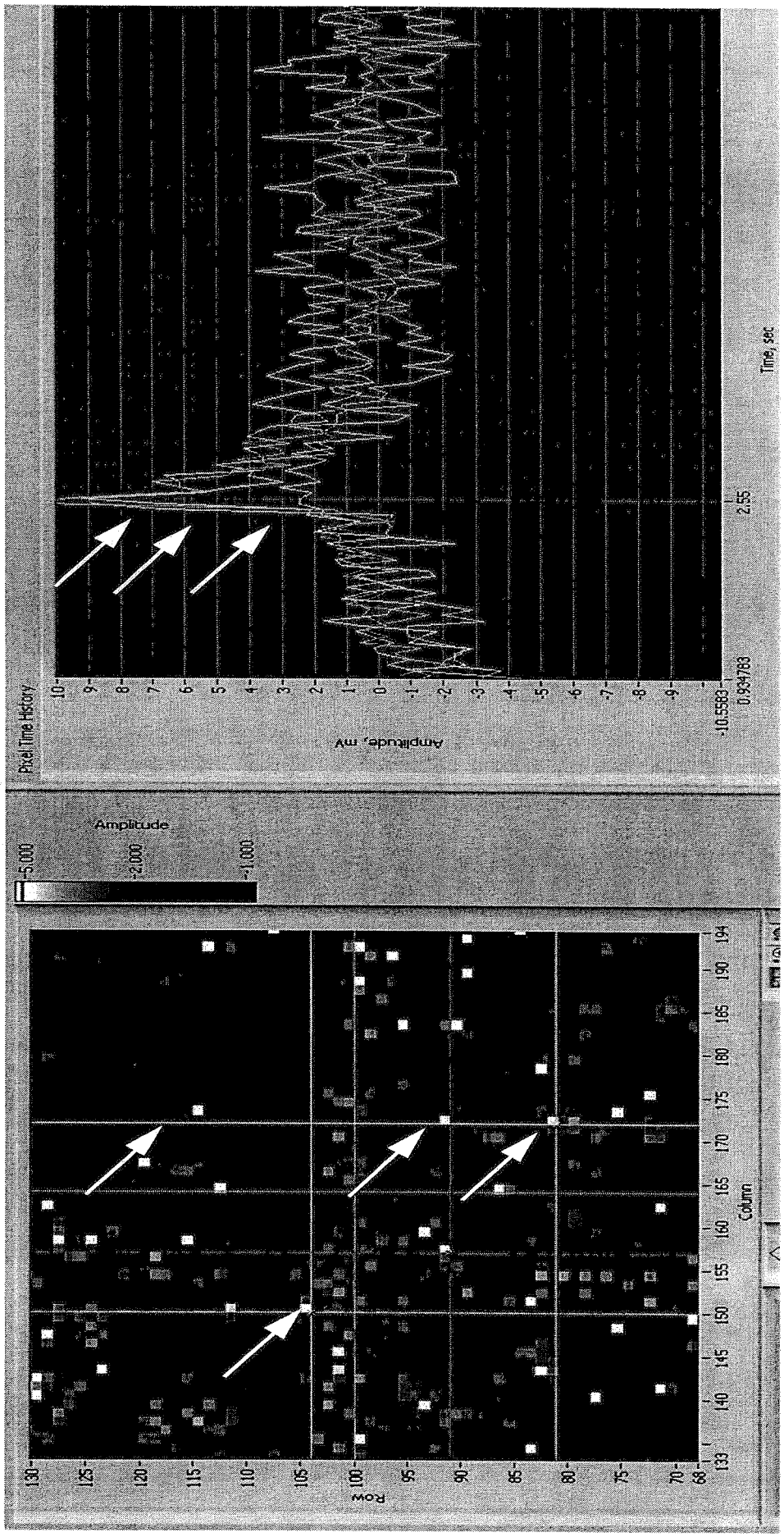

Pixel Time History
Amplitude, mV
Time, sec
Amplitude
Row
Column

FIG. 71D

SEQUENCE LISTING

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Rothberg, Jonathan M
Hinz, Wolfgang
Johnson, Kim L
Bustillo, James

<120> METHODS AND APPARATUS FOR MEASURING ANALYTES USING LARGE SCALE FET ARRAYS

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