ADJUSTING SUBSTRATE TEMPERATURE TO IMPROVE CD UNIFORMITY

Related Application

[0001] This application claims priority under 35 U.S.C. § 119 to U.S. Provisional Application No. 61/286,653 filed December 15, 2009, the content of which is incorporated herein by reference in its entirety.

Background

[0002] With each successive semiconductor technology generation, diameters of substrates, e.g., wafers, tend to increase and transistor sizes decrease, resulting in the need for an ever higher degree of accuracy and repeatability in substrate processing. Semiconductor substrate materials, such as silicon substrates, are processed by techniques which include the use of vacuum chambers. These techniques include non plasma applications such as electron beam deposition, as well as plasma applications, such as sputter deposition, plasma-enhanced chemical vapor deposition (PECVD), resist strip, and plasma etch.

[0003] Plasma etching systems available today are among those semiconductor fabrication tools which are subject to an increasing need for improved accuracy and repeatability. One metric for plasma etching systems is increased uniformity, which includes uniformity of process results on a semiconductor substrate surface as well as uniformity of process results of a succession of substrates processed with nominally the same input parameters. Continuous improvement of within-substrate uniformity is desirable. Among other things, this calls for plasma chambers with improved uniformity, consistency and self diagnostics.

Summary

[0004] Disclosed herein is a method of using a plasma etching system comprising a substrate support assembly for supporting a substrate during plasma etching, the substrate support assembly comprising a plurality of independently controllable heater zones in an arrangement under device die locations on the substrate, and a

controller unit that controls each heater zone. The method comprises (a) measuring pre-etch, or post-etch critical device parameters from previously etched substrate, on the device die locations of the substrate on the substrate; (b) communicating the pre-etch or post-etch critical device parameters to the plasma etching system; (c) subsequently supporting the substrate on the substrate support assembly; (d) communicating process recipe parameters to the plasma etching system and/or loading process recipe parameters from a memory to the plasma etching system; (e) deducing target etching temperatures at pre-determined locations on the substrate from the process recipe parameters, target post-etch critical device parameter data, and the pre-etch critical device parameters from incoming substrates, and/or the post-etch critical device parameters from previously etched substrate; (f) adjusting temperature at each predetermined location based on the target etching temperature at the predetermined location using the controllable heater zones; and (g) plasma etching the substrate.

Detailed Description

[0005] Radial and azimuthal substrate temperature control in a semiconductor processing apparatus to achieve target critical dimension (CD) uniformity on the substrate is becoming more demanding. Even a small variation of temperature may affect CD to an unacceptable degree, especially as CD approaches sub-20nm in semiconductor fabrication processes.

[0006] A substrate support assembly may be configured for a variety of functions during processing, such as supporting the substrate, tuning the substrate temperature, and supplying radio frequency power. The substrate support assembly can comprise an electrostatic chuck (ESC) useful for electrostatically clamping a substrate onto the substrate support assembly during processing. The ESC may be a tunable ESC (T-ESC). A T-ESC is described in commonly assigned U.S. Patent Nos. 6,847,014 and 6,921,724, which are hereby incorporated by reference. The substrate support assembly may comprise a ceramic substrate holder, a fluid-cooled heat sink (hereafter referred to as cooling plate) and a plurality of concentric heater zones to realize step by step and radial temperature control. Typically, the cooling plate is maintained between 0 °C and 30 °C. The heaters are located on the cooling plate

with a layer of thermal insulator in between. The heaters can maintain the support surface of the substrate support assembly at temperatures about 0 °C to 80 °C above the cooling plate temperature. By changing the heater power within the plurality of heater zones, the substrate support temperature profile can be changed between center hot, center cold, and uniform. Further, the mean substrate support temperature can be changed step by step within the operating range of 0 to 80 °C above the cooling plate temperature. A small azimuthal temperature variation poses increasingly greater challenges as CD decreases with the advance of semiconductor technology.

[0007] Controlling temperature is not an easy task for several reasons. First, many factors can affect heat transfer, such as the locations of heat sources and heat sinks, the movement, materials and shapes of the media. Second, heat transfer is a dynamic process. Unless the system in question is in heat equilibrium, heat transfer will occur and the temperature profile and heat transfer will change with time. Third, non-equilibrium phenomena, such as plasma, which of course is always present in plasma processing, make theoretical prediction of the heat transfer behavior of any practical plasma processing apparatus very difficult if not impossible.

[0008] The substrate temperature profile in a plasma processing apparatus is affected by many factors, such as the plasma density profile, the RF power profile and the detailed structure of the various heating the cooling elements in the electrostatic chuck, hence the substrate temperature profile is often not uniform and difficult to control with a small number of heating or cooling elements. This deficiency translates to non-uniformity in the processing rate across the whole substrate and non-uniformity in the critical dimension of the device dies on the substrate.

[0009] Non-uniformity in the critical dimension can be caused by upstream processes, for example, photolithography. Because of the parallel nature of photolithography (i.e. all device dies on a substrate are exposed together) and factors difficult to control such as light source non-uniformity, diffraction on photomasks, non-uniformity in temperature, non-uniformity in photoresist thickness, etc., post-lithography and pre-etch substrates usually have non-uniformity in device features.

If unchecked and allowed to propagate to downstream processes, such non-uniformity can result in reduced device yield.

[0010] It would be advantageous and desirable to incorporate multiple independently controllable heater zones in the substrate support assembly to enable a plasma etching system to actively create and maintain the target spatial and temporal temperature profile, and to compensate for adverse factors that affect CD uniformity.

[0011] A substrate support assembly with independently controlled heater zones is described in U.S. Patent Application No. 12/582,991 filed on October 21, 2009, which is hereby incorporated by reference.

[0012] Described herein is a method of using a plasma etching system having a substrate support assembly with independently controllable heater zones, for compensation for non-uniformity on a substrate to be etched by measuring pre-etch critical device parameters, or post-etch critical device parameters from previously etched substrate, on a plurality of device die locations on the substrate and using the measured information to tune temperatures at predetermined locations on the substrate during etching.

[0013] For example, after a substrate undergoes lithography, a pattern is formed in a resist layer on the substrate. The pattern in the resist layer can have non-uniformity in critical dimensions. Pre-etch critical dimensions in the resist layer on each device die on the substrate can be measured with a suitable tool. The patterned resist layer is used as a mask in later plasma etching of the substrate underneath. Temperature during plasma etching can affect critical dimensions of the etched pattern in the substrate (post-etch critical dimensions). If the pre-etch critical dimensions at a device die location are determined to fall outside of tolerable error from target values, etching temperature of the device die location can be tuned by the heater zones such that the post-etch critical dimensions are within tolerable error from the target values. Thus, the measured pre-etch critical dimensions can be used to adjust etching temperature of each device die location to compensate for the particular amount of error in the pre-etch critical dimensions at the device die location.

[0014] The plasma etching system can have independently controllable heater zones assembled in a heating plate, and a controller unit that controls each heater

zone. By tuning the power of each heater zone under control of the controller unit, the temperature profile during processing can be shaped both radially and azimuthally. The heater zones are preferably arranged in a defined pattern, for example, a rectangular grid, a hexagonal grid, or other pattern. Each heater zone of the heating plate is preferably of similar size (e.g. ±10%) to a single device die on the substrate. In an exemplary arrangement, to minimize the number of electrical connections, power supply and power return lines are arranged such that each power supply line is connected to a different group of heater zones and each power return line is connected to a different group of heater zones with each heater zone being in one of the groups connected to a particular power supply line and one of the groups connected to a particular power return line. No two heater zones are connected to the same pair of power supply and power return lines. Thus, a heater zone can be activated by directing electrical current through a pair of power supply and power return lines to which this particular heater zone is connected. The power of the heater elements is preferably smaller than 20W, more preferably 5 to 10 W. The heater elements can be Peltier devices and/or resistive heaters such as polyimide heaters, silicone rubber heaters, mica heaters, metal heaters (e.g. W, Ni/Cr alloy, Mo or Ta), ceramic heaters (e.g. WC), semiconductor heaters or carbon heaters. The heater elements may be screen printed, wire wound or etched foil heaters. The thickness of the heater elements may range from 2 micrometers to 1 millimeter, preferably 5-80 micrometers. To allow space between heater zones and/or power supply and power return lines, the total area of the heater zones may be up to 90% of the area of the upper surface of the substrate support assembly, e.g. 50-90% of the area. The power supply lines or the power return lines (power lines, collectively) may be arranged in gaps ranging from 1 to 10 mm between the heater zones, or in separate planes separated from the heater zones plane by electrically insulating layers. The power supply lines and the power return lines are preferably made as wide as the space allows, in order to carry large current and reduce Joule heating. The power lines can be in the same plane as the heater zones, or can be on different planes than the heater zones. The materials of the power supply and power return lines may be the same as or different from the materials of the heater elements. Preferably, the materials of the power supply and power return lines are materials

with low resistivity, such as Cu, Al, W, Inconel® or Mo. The substrate support assembly is operable to control the substrate temperature and consequently the plasma etching process at each device die location to maximize the yield of devices from the substrate. The plasma etching system preferably has at least 9 heater zones.

[0015] In one embodiment, the plasma etching system is able to receive measured critical device parameters (e.g. pre-etch critical dimensions) at a plurality of device die locations (preferably at least one location in each device die location) on a substrate to be processed therein (pre-etch critical device parameters), from sources such as a human user, an onboard measurement tool, a host network (a network that shares data between processing tools in a processing line) or the like. Preferably, the plasma etching system receives pre-etch critical device parameters of a batch of substrates to be processed, from an off-board inspection tool via a host communication network. Such off-board inspection tool can be an optical and/or electron beam inspection tool. The plasma etching system can have a hardware and/or software interface for receiving the pre-etch critical device parameters. The plasma etching system can have suitable software for processing the pre-etch critical device parameters.

[0016] The plasma etching system is also able to receive through a hardware and/or software interface and/or load from a memory, process recipe parameters that define dependence of target post-etch critical device parameters on the measured pre-etch critical device parameters and etching temperatures; and to deduce target etching temperature at predetermined locations on the substrate from the process recipe parameters, target post-etch critical device parameters, and measured pre-etch critical device parameters. Preferably, the plasma etching system is able to receive such process recipe parameters for each process recipe step.

[0017] Preferably, the plasma etching system is further able to calculate target control parameters (parameters that can be directly controlled such as power, voltage, current, etc.) for each heater zone based on the target etching temperature of each device die location to achieve the target critical device parameter for each device die.

[0018] The target control parameters can be obtained during manufacture of the substrate support assembly, by measuring response of surface temperatures of the

substrate support assembly to different control parameters applied thereto. Alternatively, the target control parameters can be determined by using a theoretical or empirical model such as heat transfer theories or finite element analyses.

[0019] Preferably, a steady gain matrix can be used to calculate the target control parameters with direct response of each device die location to a control parameter applied to a heater zone underneath, and with indirect response (crosstalk) of said device die to control parameters applied to other heater zones. A steady gain matrix can be calculated using methods described in *Matrix Computation* by G. Golub, et al. (The Johns Hopkins University Press, Boston 1996), which is hereby incorporated by reference in its entirety.

[0020] In one embodiment, assuming the plasma etching system has n independent heater zones. Their respective control parameter is X_i (i=1, 2, ..., n). All the control parameters X_i can be written as a vector:

[0021] $$\mathbf{X} = \begin{pmatrix} X_1 \\ X_2 \\ \vdots \\ X_n \end{pmatrix},$$

[0022] wherein X_i is preferably time-averaged power applied to the i-th heater zone.

[0023] T_i is a target etching temperature at a device die location within the i-th heater zone, which can be written as another vector:

[0024] $$\mathbf{T} = \begin{pmatrix} T_1 \\ T_2 \\ \vdots \\ T_n \end{pmatrix},$$

[0025] The vector **T** is a function of the vector **X**. A relationship between the vector **X** and **T** can described by a n-by-n matrix **K**, wherein $\mathbf{T}=\mathbf{K}\cdot\mathbf{X}$. Diagonal elements K_{ii}, can be measured during manufacture of the substrate support assembly or the plasma etching system. Off-diagonal elements K_{ij} ($i \neq j$) can be measured during manufacture of the substrate support assembly or plasma etching system, or derived from a finite element thermal model, the values of diagonal elements and the physical distance between the i-th and j-th heater zones. The matrix **K** is stored in

the plasma etching system. The plasma etching system also has software or firmware functional to execute an algorithm to deduce **X** based on **T**. The algorithm is a matrix inversion followed by a matrix multiplication, i.e. $\mathbf{X}=\mathbf{K}^{-1}\cdot\mathbf{T}$.

[0026] In another embodiment, assuming the plasma etching system has n independent heater zones. Their respective control parameter is X_i (i=1, 2, ..., n). All the control parameters X_i can be written as a vector:

[0027] $$\mathbf{X}=\begin{pmatrix} X_1 \\ X_2 \\ \vdots \\ X_n \end{pmatrix},$$

[0028] wherein X_i is preferably time-averaged power applied to the i-th heater zone.

[0029] $\boldsymbol{P}=\{P_j\}$ is a set of predicated etching temperatures at predetermined locations on the substrate at which the temperature response to each heater zone is known based on prior modeling or calibration measurements. $\boldsymbol{P}$ can be written as another vector:

[0030] $$P=\begin{pmatrix} P_1 \\ P_2 \\ \vdots \\ Pm \end{pmatrix},$$

[0031] $\boldsymbol{T}=\{T_j\}$ are a set of target etching temperatures at the same predetermined locations on the substrate. T can be written as another vector:

[0032] $$\mathbf{T}=\begin{pmatrix} T_1 \\ T_2 \\ \vdots \\ Tm \end{pmatrix},$$

[0033] In this embodiment, the number m of the locations on the substrate having respective target etching temperatures does not equal the number of heater zones, i.e., $m\neq n$. The locations having temperature response may differ from the locations of the heater zones. The vector **P** is a function of the vector **X**. A relationship between the vector **P** and **T** can be described by an m-by-n matrix **K**, wherein $\mathbf{P}=\mathbf{K}\cdot\mathbf{X}$. Elements K_{ij} can be measured during manufacture of the substrate support

assembly or plasma etching system, or derived from a finite element thermal model. The matrix **K** is stored in the plasma etching system. The plasma etching system also has software or firmware functional to execute an algorithm to deduce X based on T, using the matrix and an optimization algorithm, e.g., a least squares optimization. The optimization algorithm facilitates determination of heater power setpoints by minimizing the differences between predicted temperatures at device die locations and target temperatures at the respective locations on the substrate.

[0034] In the above embodiments, the location at which the substrate characteristics, e.g., CD measurements, are measured may differ from the number of heater zones. In addition, the locations at which the substrate characteristics are measured may not coincide with the locations at which temperature response for each heater zone is known based on modeling or previous measurements, e.g., during manufacturing. That is, the substrate characteristics measurement locations differ from those used to construct the matrix K. Consequently, the substrate characteristics need to be estimated at the same locations as those used to construct matrix K. In a preferred embodiment, a technique, such as linear or nonlinear interpolation, can be used to transform the data for the substrate characteristics, e.g. CD measurements, from the substrate characteristics measurement locations to the locations at which the individual heater responses have been modeled/measured during calibration, i.e., the locations used to construct matrix K.

[0035] In an alternative embodiment, the control parameters can be dynamically determined by a control circuit (e.g. a PID controller) based on output of temperature sensors (e.g. optical sensors, thermal couples, diodes, or the like) in each heater zone.

[0036] While the method of using a plasma etching system has been described in detail with reference to specific embodiments thereof, it will be apparent to those skilled in the art that various changes and modifications can be made, and equivalents employed, without departing from the scope of the appended claims.

We Claim:

1. A method of using a plasma etching system, the plasma etching system comprising a substrate support assembly for supporting a substrate during plasma etching, the substrate support assembly comprising a plurality of independently controllable heater zones in an arrangement under device die locations on the substrate, and a controller unit that controls each heater zone; the method comprising:

measuring pre-etch critical device parameters on a plurality of device die locations on the substrate;

communicating at least one of the pre-etch critical device parameters and post-etch critical device parameters from previously etched substrate to the plasma etching system;

subsequently supporting the substrate on the substrate support assembly;

communicating process recipe parameters to the plasma etching system and/or loading process recipe parameters from a memory to the plasma etching system;

deducing a target etching temperature for predetermined locations on the substrate from at least one of the process recipe parameters, target post-etch critical device parameters, the pre-etch critical device parameters, and the post-etch critical device parameters;

adjusting temperature of each device die location to its target etching temperature, using the controllable heater zones; and

plasma etching the substrate.

2. The method of claim 1, further comprising communicating process recipe parameters to the plasma etching system and/or loading process recipe parameters from a memory to the plasma etching system for each step of an etching process recipe.

3. The method of claim 1, further comprising communicating and/or calculating target control parameters of each heater zone based on the target etching temperatures at the predetermined locations on the substrate.

4. The method of claim 1, wherein when the number of the heater zones and the number of the device die locations are equal, the step of adjusting temperature using the controllable heater zones comprises:

determining heater power setpoints for the heater zones by multiplying an inversed matrix describing a relationship of the target control parameters of the heater zones and the target etching temperatures of the device die locations by a vector whose elements are the target etching temperatures of the device die locations.

5. The method of claim 1, wherein the plasma etching system comprises one or more temperature sensors configured to measure etching temperature of each heater zone location, the method further comprising calculating target control parameters of each heater zone based on outputs from the temperature sensors.

6. A plasma etching system for carrying out the method of claim 1, comprising a substrate support assembly for supporting a substrate during plasma etching, the substrate support assembly comprising a plurality of independently controllable heater zones in an arrangement under the substrate, and a controller unit that controls each heater zone.

7. A plasma etching system for carrying out the method of claim 6, comprising an interface which receives the pre-etch or the post critical device parameters from an off-board inspection tool via a host communication network.

8. The method of claim 1, wherein when the number of the heater zones and the number of the device die locations are not equal, the step of adjusting temperature using the controllable heater zones includes:

determining heater power setpoints for the heater zones based on a matrix describing a relationship of the target control parameters of the heater zones and predicted etching temperatures of the predetermined locations on the substrate,

wherein the difference between the predicted etching temperatures of the device die locations and the target etching temperatures of the device die locations is minimized by an optimization technique.

9. The method of claim 8, wherein the optimization technique is a least squares optimization.

10. A method of using a plasma etching system, the plasma etching system comprising a substrate support assembly for supporting a substrate during plasma etching, the substrate support assembly comprising independently controllable heater zones in an arrangement under device die locations on the substrate, and a controller unit that controls each heater zone; the method comprising:

measuring pre-etch critical device parameters at a first set of predetermined locations on the substrate;

communicating at least one of the pre-etch critical device parameters and post-etch critical device parameters from previously etched substrate to the plasma etching system;

subsequently supporting the substrate on the substrate support assembly;

communicating at least one of process recipe parameters and loading process recipe parameters from a memory to the plasma etching system;

deducing target etching temperatures at a second set of predetermined locations on the substrate based on at least one of the process recipe parameters, target post-etch critical device parameters, the pre-etch critical device parameters, and the post-etch critical device parameters;

determining heater power setpoints for the controllable heater zones based on a relationship between the heater power for each of the heater zones and the predicted etching temperatures at the second set of predetermined locations, wherein the heater power setpoints are determined such that the difference between the

predicted etching temperatures and the target etching temperatures is minimized by an optimization technique;

plasma etching the substrate.

11. The method of claim 10, wherein the optimization technique is a least squares optimization.

12. The method of claim 10, wherein deducing target etching temperatures includes estimating data of pre-etch or post-etch critical device parameters at the second set of predetermined locations based on the data of the pre-etch or post-etch critical device parameters at the first set of predetermined locations.

13. The method of claim 12, wherein the estimating includes interpolating the data of pre-etch or post-etch critical device parameters at the second set of predetermined locations based on the data of the pre-etch or post-etch critical device parameters at the second set of predetermined locations.

14. The method of claim 10, wherein a relationship between the heater power for each of the heater zones and the predicted etching temperatures at the second set of predetermined locations is described by a matrix.

15. The method of claim 13, wherein the interpolating is a linear interpolation.

16. The method of claim 13, wherein the interpolating is a non-linear interpolation.