

WHAT IS CLAIMED IS:

1. A memory device, comprising:
 - a substrate;
 - a bottom select gate (BSG) disposed over the substrate;
 - a plurality of word lines positioned over the BSG with a staircase configuration;
 - a plurality of insulating layers disposed between the substrate, the BSG, and the plurality of word lines;
 - one or more first dielectric trenches formed in the BSG and extending in a length direction of the substrate to separate the BSG into a plurality of sub-BSGs; and
 - one or more common source regions formed over the substrate and extending in the length direction of the substrate, wherein the one or more common source regions extend through the BSG, the plurality of word lines, and the plurality of insulating layers.
2. The memory device of claim 1, further comprising:
 - a top select gate (TSG) positioned over the plurality of word lines, the TSG and the plurality of word lines being spaced apart by the plurality of insulating layers; and
 - one or more second dielectric trenches formed in the TSG and extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs.
3. The memory device of claim 2, wherein the first dielectric trenches and the second dielectric trenches are aligned with each other in a width direction of the substrate.
4. The memory device of claim 2, wherein the one or more common source regions further

pass through the TSG, and the one or more common source regions, the first dielectric trenches, and the second dielectric trenches extend parallel to each other in the length direction of the substrate.

5. The memory device of claim 2, further comprising:

a plurality of channel structures formed over the substrate along a height direction of the substrate that is perpendicular to the substrate, wherein each of the plurality of channel structure passes through the BSG, the plurality of word lines, the TSG, and the plurality of insulating layers.

6. The memory device of claim 1, further comprising:

a plurality of dummy channel structures formed along the a height direction of the substrate that is perpendicular to the substrate, the plurality of dummy channel structures passing through the BSG, the plurality of word lines and the plurality of insulating layers to extend into the substrate.

7. The memory device of claim 5, further comprising a plurality of memory cell sub-blocks, each of the memory cell sub-blocks including a plurality of respective channel structures that are connected to a same sub-BSG and to a same sub-TSG, each of the memory cell sub-blocks being operated individually.

8. The memory device of claim 5, wherein the one or more first dielectric trenches and the one or more common source regions are alternatively disposed in the width direction of the substrate.

9. The memory device of claim 5, wherein the one or more second dielectric trenches

and the one or more common source regions are alternatively disposed in the width direction of the substrate so that a plurality of channel structures are disposed therebetween.

10. The memory device of claim 1, further comprising one or more dummy BSGs that are formed between the plurality of word lines and the BSG, separated by the one or more first dielectric trenches into a plurality of dummy sub-BSGs, and spaced apart from the plurality of word lines and the BSG by the plurality of insulating layer.

11. The memory device of claim 2, further comprising one or more dummy TSGs that are formed between the plurality of word lines and the TSG, separated by the one or more second dielectric trenches into a plurality of dummy sub-TSGs, and spaced apart from the plurality of the word lines and the TSG by the plurality of insulating layers.

12. A method for manufacturing a memory device, comprising:

forming a plurality of first insulating layers, and a bottom select gate (BSG) layer over a substrate, the plurality of first insulating layers being disposed between the substrate, and the BSG layer;

forming one or more first dielectric trenches that pass through the BSG layer, and the plurality of first insulating layers, and extend in a length direction of the substrate, the BSG layer being separated by the one or more first dielectric trenches into a plurality of sub-BSG layers;

forming a plurality of word line layers, and a plurality of second insulating layers over the BSG layer, the plurality of second insulating layers being disposed between the BSG layer and the plurality of word line layers; and

forming one or more common source regions over the substrate and extending in

the length direction of the substrate, each of the one or more common source regions extending through the BSG layer, the plurality of first insulating layers, the plurality of word line layers, and the plurality of second insulating layers.

13. The method of claim 12, further comprising:

forming a top select gate (TSG) layer over the plurality of word line layers, the TSG layer and the plurality of word line layers being spaced apart by the plurality of second insulating layers.

14. The method of claim 13, wherein each of the one or more common source regions further extends through the BSG layer, the plurality of first insulating layers, the plurality of word line layers, the plurality of second insulating layers, and the TSG layer.

15. The method of claim 13, further comprising:

forming one or more second dielectric trenches that extend in the length direction of the substrate, and pass through the TSG layer and a portion of the plurality of second insulating layers that separate an uppermost word line layer and the TSG layer from each other, wherein the first dielectric trenches and the second dielectric trenches are aligned with each other in a width direction of the substrate and are spaced apart by the plurality of word line layers, wherein the TSG layer is separated by the one or more second dielectric trenches into a plurality of sub-TSG layers.

16. The method of claim 13, further comprising;

forming a plurality of channel structures, wherein the plurality of channel structures are formed over the substrate along a height direction that is perpendicular to the substrate, wherein each of the plurality of channel structures passes through the BSG

layer, the plurality of first insulating layers, the plurality of word line layers, the TSG layer, and the plurality of second insulating layers .

17. A method for erasing a 3D-NAND memory device, wherein the 3D-NAND memory device are formed over a substrate and includes a plurality of vertical NAND strings in which a first sub-block of the plurality of vertical NAND strings are connected to a first bottom select gate (BSG), a second sub-block of the plurality of vertical NAND strings are connected to a second BSG, the first BSG and the second BSG are separated by a dielectric trench, and both the first sub-block and the second sub-block of vertical NAND strings are connected to a plurality of shared word lines, the method comprising:

setting the substrate to a first voltage;

setting the first BSG to a second voltage, the second voltage being lower than the first voltage; and

setting the one or more word lines to a third voltage that is equal to zero.

18. The method of claim 17, further comprising:

setting the second BSG to a fourth voltage, the fourth voltage being higher than the second voltage.

19. The method of claim 17, wherein the first sub-block of the plurality of vertical NAND strings are further connected to one or more first dummy BSGs, and the second sub-block of the plurality of vertical NAND strings are further connected to one or more second dummy BSGs, and the first dummy BSGs and the second dummy BSGs are separated by the dielectric trench, the method further comprising:

setting the one or more first dummy BSGs to a fifth voltage, the fifth

voltage being lower than the second voltage; and

setting the one or more second dummy BSGs to a sixth voltage, the sixth voltage being lower than the fourth voltage.

20. The method of claim 18, wherein the second voltage is in a range from zero to 13 volts, and the fourth voltage is in a range from 18 to 25 volts.