

SELF-ALIGNED WIDE BACKSIDE POWER RAIL CONTACTS TO MULTIPLE TRANSISTOR SOURCES

TECHNICAL FIELD

- 5 **[0001]** Embodiments of the disclosure generally relate to semiconductor devices. More particularly, embodiments of the disclosure are directed to power rail architecture, 3D packaging, and methods of manufacturing semiconductor devices.

BACKGROUND

- 10 **[0002]** The semiconductor processing industry continues to strive for larger production yields while increasing the uniformity of layers deposited on substrates having larger surface areas. These same factors in combination with new materials also provide higher integration of circuits per unit area of the substrate. As circuit integration increases, the need for greater uniformity and process control regarding
15 layer thickness rises. As a result, various technologies have been developed to deposit layers on substrates in a cost-effective manner, while maintaining control over the characteristics of the layer.

- [0003]** Semiconductor devices are typically fabricated by sequentially depositing insulating or dielectric layers, conductive layers, and semiconductor layers of material
20 over a semiconductor substrate, and patterning the various material layers using lithography to form circuit components and elements thereon. The conductive layers facilitate electrical wiring to various electrical components including transistors, amplifiers, inverters, control logic, memory, power management circuits, buffers, filters, resonators, capacitors, inductors, resistors, and the like.

- 25 **[0004]** The transistor is a key component of most integrated circuits. Since the drive current, and therefore speed, of a transistor is proportional to the gate width of the transistor, faster transistors generally require larger gate width. Thus, there is a trade-off between transistor size and speed, and "fin" field-effect transistors (finFETs) have been developed to address the conflicting goals of a transistor having maximum
30 drive current and minimum size. FinFETs are characterized by a fin-shaped channel region that greatly increases the size of the transistor without significantly increasing

the footprint of the transistor and are now being applied in many integrated circuits. However, finFETs have their own drawbacks.

[0005] As the feature sizes of transistor devices continue to shrink to achieve greater circuit density and higher performance, there is a need to improve transistor device structure to improve electrostatic coupling and reduce negative effects such as parasitic capacitance and off-state leakage. Examples of transistor device structures include a planar structure, a fin field effect transistor (FinFET) structure, and a horizontal gate all around (hGAA) structure. The hGAA device structure includes several lattice matched channels suspended in a stacked configuration and connected by source/drain regions. The hGAA structure provides good electrostatic control and can find broad adoption in complementary metal oxide semiconductor (CMOS) wafer manufacturing

[0006] Connecting semiconductors to a power rail is typically done on the front of the cell, which requires significant cell area. Accordingly, there is a need for semiconductor devices which are connected to power rails using less cell area.

SUMMARY

[0007] One or more embodiments of the disclosure are directed to methods of forming a semiconductor device. In one or more embodiments, a method of forming a semiconductor device comprises: forming a superlattice structure on a top surface of a substrate, the superlattice structure comprising a plurality of horizontal channel layers and a corresponding plurality of semiconductor material layers alternately arranged in a plurality of stacked pairs; forming a plurality of source trenches and a plurality of drain trenches adjacent to the superlattice structure on the substrate; expanding at least one of the plurality of source trenches and at least one of the plurality of drain trenches to form a source cavity and a drain cavity; depositing a sacrificial material in the source cavity and in the drain cavity; forming a source region and a drain region; forming at CT and CG in electrical contact with the source region and the drain region; forming a damascene trench through the substrate; at least partially removing the sacrificial material to form at least one opening extending to the damascene trench; and depositing a metal in the at least one opening and in the damascene trench.

[0008] Additional embodiments of the disclosure are directed to methods of forming a semiconductor device. In one or more embodiments, a method of forming a semiconductor device comprises: forming a superlattice structure on a top surface of a substrate, the superlattice structure comprising a plurality of horizontal channel layers and a corresponding plurality of semiconductor material layers alternatingly arranged in a plurality of stacked pairs; forming a gate structure on a top surface of the superlattice structure; forming a plurality of source trenches and a plurality of drain trenches adjacent to the superlattice structure on the substrate; expanding at least one of the plurality of source trenches and at least one of the plurality of drain trenches to form a source cavity and a drain cavity; depositing a sacrificial material in the source cavity and in the drain cavity; forming an inner spacer layer on each of the plurality of horizontal channel layers; forming a source region and a drain region; forming an inter-layer dielectric layer on the substrate; forming a replacement metal gate; forming at CT and CG in electrical contact with the source region and the drain region; forming a first metal line; rotating the semiconductor device 180 degrees; planarizing the substrate; planarizing the substrate; depositing an interlayer dielectric material on the substrate; forming a backside power rail via in the substrate; expanding the backside power rail via to form a damascene trench; removing the sacrificial material to form at least one opening; and depositing a metal in the at least one opening and in the damascene trench.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this disclosure and are therefore not to be considered limiting of its scope, for the disclosure may admit to other equally effective embodiments.

[0010] FIG. 1A is a process flow diagram of a method according to one or more embodiments;

- [0011] FIG. 1B is a continuation of the process flow diagram of FIG.1A depicting a method according to one or more embodiments;
- [0012] FIG. 2A illustrates a cross-section view of a device according to one or more embodiments;
- 5 [0013] FIG. 2B illustrates a cross-section view of a device according to one or more embodiments;
- [0014] FIG. 2C illustrates a cross-section view of a device according to one or more embodiments;
- 10 [0015] FIG. 2D illustrates a cross-section view of a device according to one or more embodiments;
- [0016] FIG. 2E illustrates a cross-section view of a device according to one or more embodiments;
- [0017] FIG. 2F illustrates a cross-section view of a device according to one or more embodiments;
- 15 [0018] FIG. 2G illustrates a cross-section view of a device according to one or more embodiments;
- [0019] FIG. 2H illustrates a cross-section view of a device according to one or more embodiments;
- [0020] FIG. 2I illustrates a cross-section view of a device according to one or more
- 20 [0021] FIG. 2J illustrates a cross-section view of a device according to one or more embodiments;
- [0022] FIG. 2K illustrates a cross-section view of a device according to one or more embodiments;
- 25 [0023] FIG. 2L illustrates a cross-section view of a device according to one or more embodiments;
- [0024] FIG. 2M illustrates a cross-section view of a device according to one or more embodiments;
- 30 [0025] FIG. 2N illustrates a cross-section view of a device according to one or more embodiments;

- [0026] FIG. 2O illustrates a cross-section view of a device according to one or more embodiments;
- [0027] FIG. 2P illustrates a cross-section view of a device according to one or more embodiments;
- 5 [0028] FIG. 2Q illustrates a cross-section view of a device according to one or more embodiments;
- [0029] FIG. 2R illustrates a cross-section view of a device according to one or more embodiments;
- [0030] FIG. 2S illustrates a cross-section view of a device according to one or
10 more embodiments;
- [0031] FIG. 2T illustrates a cross-section view of a device according to one or more embodiments;
- [0032] FIG. 2U illustrates a cross-section view of a device according to one or more embodiments;
- 15 [0033] FIG. 3 illustrates a process flow diagram of a method according to one or more embodiments;
- [0034] FIG. 4A illustrates a cross-section view of a device according to one or more embodiments;
- [0035] FIG. 4B illustrates a cross-section view of a device according to one or
20 more embodiments;
- [0036] FIG. 4C illustrates a cross-section view of a device according to one or more embodiments;
- [0037] FIG. 4D illustrates a cross-section view of a device according to one or more embodiments;
- 25 [0038] FIG. 4E illustrates a cross-section view of a device according to one or more embodiments;
- [0039] FIG. 5A illustrates a cross-section view of a device according to one or more embodiments;
- [0040] FIG. 5B illustrates a cross-section view of a device according to one or
30 more embodiments;

- [0041] FIG. 5C illustrates a cross-section view of a device according to one or more embodiments;
- [0042] FIG. 5D illustrates a cross-section view of a device according to one or more embodiments;
- 5 [0043] FIG. 6 illustrates a process flow diagram of a method according to one or more embodiments;
- [0044] FIG. 7A illustrates a cross-section view of a device according to one or more embodiments;
- [0045] FIG. 7B illustrates a cross-section view of a device according to one or
10 more embodiments;
- [0046] FIG. 7C illustrates a cross-section view of a device according to one or more embodiments;
- [0047] FIG. 7D illustrates a cross-section view of a device according to one or more embodiments; and
- 15 [0048] FIG. 8 illustrates a cluster tool according to one or more embodiments.
- [0049] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. The figures are not drawn to scale and may be simplified for clarity. Elements and features of one embodiment may be beneficially incorporated in other embodiments without
20 further recitation.

DETAILED DESCRIPTION

- [0050] Before describing several exemplary embodiments of the disclosure, it is to be understood that the disclosure is not limited to the details of construction or
25 process steps set forth in the following description. The disclosure is capable of other embodiments and of being practiced or being carried out in various ways.
- [0051] As used in this specification and the appended claims, the term “substrate” refers to a surface, or portion of a surface, upon which a process acts. It will also be understood by those skilled in the art that reference to a substrate can also refer to
30 only a portion of the substrate unless the context clearly indicates otherwise.

Additionally, reference to depositing on a substrate can mean both a bare substrate and a substrate with one or more films or features deposited or formed thereon.

[0052] A "substrate" as used herein, refers to any substrate or material surface formed on a substrate upon which film processing is performed during a fabrication process. For example, a substrate surface on which processing can be performed include materials such as silicon, silicon oxide, strained silicon, silicon on insulator (SOI), carbon doped silicon oxides, silicon nitride, doped silicon, germanium, gallium arsenide, glass, sapphire, and any other materials such as metals, metal nitrides, metal alloys, and other conductive materials, depending on the application. Substrates include, without limitation, semiconductor wafers. Substrates may be exposed to a pretreatment process to polish, etch, reduce, oxidize, hydroxylate (or otherwise generate or graft target chemical moieties to impart chemical functionality), anneal and/or bake the substrate surface. In addition to film processing directly on the surface of the substrate itself, in the present disclosure, any of the film processing steps disclosed may also be performed on an underlayer formed on the substrate as disclosed in more detail below, and the term "substrate surface" is intended to include such underlayer as the context indicates. Thus, for example, where a film/layer or partial film/layer has been deposited onto a substrate surface, the exposed surface of the newly deposited film/layer becomes the substrate surface. What a given substrate surface comprises will depend on what films are to be deposited, as well as the particular chemistry used.

[0053] As used in this specification and the appended claims, the terms "precursor", "reactant", "reactive gas" and the like are used interchangeably to refer to any gaseous species that can react with the substrate surface.

[0054] Transistors are circuit components or elements that are often formed on semiconductor devices. Depending upon the circuit design, in addition to capacitors, inductors, resistors, diodes, conductive lines, or other elements, transistors are formed on a semiconductor device. Generally, a transistor includes a gate formed between source and drain regions. In one or more embodiments, the source and drain regions include a doped region of a substrate and exhibit a doping profile suitable for a particular application. The gate is positioned over the channel region and includes a

gate dielectric interposed between a gate electrode and the channel region in the substrate.

[0055] As used herein, the term “field effect transistor” or “FET” refers to a transistor that uses an electric field to control the electrical behavior of the device.

5 Enhancement mode field effect transistors generally display very high input impedance at low temperatures. The conductivity between the drain and source terminals is controlled by an electric field in the device, which is generated by a voltage difference between the body and the gate of the device. The FET's three terminals are source (S), through which the carriers enter the channel; drain (D),
10 through which the carriers leave the channel; and gate (G), the terminal that modulates the channel conductivity. Conventionally, current entering the channel at the source (S) is designated I_S and current entering the channel at the drain (D) is designated I_D . Drain-to-source voltage is designated V_{DS} . By applying voltage to gate (G), the current entering the channel at the drain (i.e., I_D) can be controlled.

15 **[0056]** The metal–oxide–semiconductor field-effect transistor (MOSFET) is a type of field-effect transistor (FET). It has an insulated gate, whose voltage determines the conductivity of the device. This ability to change conductivity with the amount of applied voltage is used for amplifying or switching electronic signals. A MOSFET is based on the modulation of charge concentration by a metal–oxide–semiconductor
20 (MOS) capacitance between a body electrode and a gate electrode located above the body and insulated from all other device regions by a gate dielectric layer. Compared to the MOS capacitor, the MOSFET includes two additional terminals (source and drain), each connected to individual highly doped regions that are separated by the body region. These regions can be either p or n type, but they are both be of the same
25 type, and of opposite type to the body region. The source and drain (unlike the body) are highly doped as signified by a “+” sign after the type of doping.

[0057] If the MOSFET is an n-channel or nMOS FET, then the source and drain are n+ regions and the body is a p region. If the MOSFET is a p-channel or pMOS FET, then the source and drain are p+ regions and the body is an n region. The
30 source is so named because it is the source of the charge carriers (electrons for n-

channel, holes for p-channel) that flow through the channel; similarly, the drain is where the charge carriers leave the channel.

[0058] As used herein, the term "fin field-effect transistor (FinFET)" refers to a MOSFET transistor built on a substrate where the gate is placed on two or three sides of the channel, forming a double- or triple-gate structure. FinFET devices have been given the generic name FinFETs because the channel region forms a "fin" on the substrate. FinFET devices have fast switching times and high current density.

[0059] As used herein, the term "gate all-around (GAA)," is used to refer to an electronic device, e.g., a transistor, in which the gate material surrounds the channel region on all sides. The channel region of a GAA transistor may include nanowires or nano-slabs or nano-sheets, bar-shaped channels, or other suitable channel configurations known to one of skill in the art. In one or more embodiments, the channel region of a GAA device has multiple horizontal nanowires or horizontal bars vertically spaced, making the GAA transistor a stacked horizontal gate-all-around (hGAA) transistor.

[0060] As used herein, the term "nanowire" refers to a nanostructure, with a diameter on the order of a nanometer (10^{-9} meters). Nanowires can also be defined as the ratio of the length to width being greater than 1000. Alternatively, nanowires can be defined as structures having a thickness or diameter constrained to tens of nanometers or less and an unconstrained length. Nanowires are used in transistors and some laser applications, and, in one or more embodiments, are made of semiconducting materials, metallic materials, insulating materials, superconducting materials, or molecular materials. In one or more embodiments, nanowires are used in transistors for logic CPU, GPU, MPU, and volatile (e.g., DRAM) and non-volatile (e.g., NAND) devices. As used herein, the term "nanosheet" refers to a two-dimensional nanostructure with a thickness in a scale ranging from about 0.1 nm to about 1000 nm.

[0061] The embodiments of the disclosure are described by way of the Figures, which illustrate devices (e.g., transistors) and processes for forming transistors in accordance with one or more embodiments of the disclosure. The processes shown are merely illustrative possible uses for the disclosed processes, and the skilled

artisan will recognize that the disclosed processes are not limited to the illustrated applications.

[0062] One or more embodiments of the disclosure are described with reference to the Figures. In the method of one or more embodiments, transistors, e.g., gate all-around transistors, are fabricated using a standard process flow. In some embodiments, a silicon wafer is provided and a buried etch stop layer is formed on the silicon wafer. An epitaxial layer, e.g., epitaxial silicon, is deposited. The wafer is then subjected to device and front-end processing. After front-end processing, the wafer undergoes hybrid bonding, e.g., to copper or to an oxide, and then the wafer is advantageously thinned. Thinning the wafer provides desired flatness and bonding for making a back side power rail possible. To thin the wafer, the silicon substrate layer, which has a starting first thickness, is ground to a second thickness, the second thickness less than the first thickness. After grinding, in some embodiments, the silicon wafer is subjected to chemical mechanical planarization (CMP), followed by etching and CMP buffing, to reduce the thickness of the silicon to a third thickness, the third thickness less than the second thickness. In one or more embodiments, the etching stops at the buried etch stop layer. The contacts are then prefilled with a metal, and metallization is conducted.

[0063] In alternative embodiments, transistors, e.g., gate all-around transistors, are fabricated using a standard process flow. In some embodiments, a silicon wafer is provided and a buried etch stop layer is formed on the silicon wafer. An epitaxial layer, e.g., epitaxial silicon, is deposited. The wafer is then subjected to device and front-end processing. After front-end processing, the wafer undergoes hybrid bonding, e.g., to copper or to an oxide, and then the wafer is advantageously thinned. Thinning the wafer provides desired flatness and bonding for making a back side power rail possible. To thin the wafer, the silicon substrate layer, which has a starting first thickness, is ground to a second thickness, the second thickness less than the first thickness. After grinding, a large mask is deposited and vias are formed in the mask. The wafer is then etched through the vias to the buried etch stop layer, and then the etch stop layer is selectively removed, and liftoff occurs.

[0064] In the method of one or more embodiments, transistors, e.g., gate all-around transistors, are fabricated using a standard process flow. After the source/drain cavity is recessed, the dimension of the source/drain cavity is expanded, and a sacrificial fill material is deposited. Fabrication proceeds with formation of the inner spacer, source/drain epitaxy, formation of an interlayer dielectric, replacement gate formation, CT and CG formation, and frontside metal line formation. The substrate is then flipped and planarized. An interlayer dielectric is deposited on the backside, backside power rail vias are patterned and the interlayer dielectric is etched. A damascene trench is formed, and the sacrificial fill is removed to form an opening. A metal is deposited in the opening, and then backside metal lines are formed. In one or more embodiments, the sacrificial fill material is advantageously selective so that, upon etching, self-aligned trenches and/or vias are formed, thus avoiding misalignment.

[0065] In the method of one or more embodiments, transistors, e.g., gate all-around transistors, are fabricated using a standard process flow. Deep vias are etched with a separate mask, or alternately they are etched with regular contact or via mask. After etching regular vias, mask is placed and then power rail vias are etched to depth below device for ease of backside connection. Both standard and deep vias/contacts are filled simultaneously with titanium nitride/ tungsten (TiN/W) or titanium nitride/ruthenium (TiN/Ru) or molybdenum (Mo) contact fill, followed by planarization. The wafer may be optionally thinned. On the backside, a via is etched to connect to the deep via. Metallization then occurs.

[0066] FIG. 1A illustrates a process flow diagram for a method 6 for forming a semiconductor device in accordance with some embodiments of the present disclosure. FIG. 1B is a continuation of the process flow diagram of FIG. 1A depicting the method 6 according to one or more embodiments. FIGS. 2A-2U depict the stages of fabrication of semiconductor structures in accordance with some embodiments of the present disclosure. The method 6 is described below with respect to FIGS. 2A-2U. FIGS. 2A-2U are cross-sectional views of an electronic device (e.g., a GAA) according to one or more embodiments. The method 6 may be part of a multi-step fabrication process of a semiconductor device. Accordingly, the method 6 may be performed in

any suitable process chamber coupled to a cluster tool. The cluster tool may include process chambers for fabricating a semiconductor device, such as chambers configured for etching, deposition, physical vapor deposition (PVD), chemical vapor deposition (CVD), oxidation, or any other suitable chamber used for the fabrication of a semiconductor device.

5 [0067] FIGS. 2A-2U are the fabrication steps of operations 8 thru 54 in FIGS. 1A-1B. Referring to FIG. 1A, the method 6 of forming the device 100 begins at operation 8, by providing a substrate 102. In some embodiments, the substrate 102 may be a bulk semiconductor substrate. As used herein, the term "bulk semiconductor
10 substrate" refers to a substrate in which the entirety of the substrate is comprised of a semiconductor material. The bulk semiconductor substrate may comprise any suitable semiconducting material and/or combinations of semiconducting materials for forming a semiconductor structure. For example, the semiconducting layer may comprise one or more materials such as crystalline silicon (e.g., Si<100> or Si<111>), silicon oxide, strained silicon, silicon germanium, doped or undoped polysilicon, doped or undoped
15 silicon wafers, patterned or non-patterned wafers, doped silicon, germanium, gallium arsenide, or other suitable semiconducting materials. In some embodiments, the semiconductor material is silicon (Si). In one or more embodiments, the semiconductor substrate 102 comprises a semiconductor material, e.g., silicon (Si), carbon (C), germanium (Ge), silicon germanium (SiGe), germanium tin (GeSn), other semiconductor materials, or any combination thereof. In one or more embodiments, the substrate 102 comprises one or more of silicon (Si), germanium (Ge), gallium (Ga), arsenic (As), or phosphorus (P). Although a few examples of materials from which the substrate may be formed are described herein, any material that may serve
25 as a foundation upon which passive and active electronic devices (e.g., transistors, memories, capacitors, inductors, resistors, switches, integrated circuits, amplifiers, optoelectronic devices, or any other electronic devices) may be built falls within the spirit and scope of the present disclosure.

[0068] In some embodiments, the semiconductor material may be a doped
30 material, such as n-doped silicon (n-Si), or p-doped silicon (p-Si). In some embodiments, the substrate may be doped using any suitable process such as an ion

implantation process. As used herein, the term "n-type" refers to semiconductors that are created by doping an intrinsic semiconductor with an electron donor element during manufacture. The term n-type comes from the negative charge of the electron. In n-type semiconductors, electrons are the majority carriers and holes are the minority carriers. As used herein, the term "p-type" refers to the positive charge of a well (or hole). As opposed to n-type semiconductors, p-type semiconductors have a larger hole concentration than electron concentration. In p-type semiconductors, holes are the majority carriers and electrons are the minority carriers. In one or more embodiments, the dopant is selected from one or more of boron (B), gallium (Ga), phosphorus (P), arsenic (As), other semiconductor dopants, or combinations thereof.

[0069] With reference to FIG. 1A, in some unillustrated embodiments, at operation 10, an etch stop layer may be formed on a top surface of the substrate. The etch stop layer may comprise any suitable material known to the skilled artisan. In one or more embodiments, the etch stop layer comprises silicon germanium (SiGe). In one or more embodiments, the etch stop layer has a high germanium (Ge) content. In one or more embodiments, the amount of germanium is in a range of from 30% to 50%, including a range of from 35% to 45%. Without intending to be bound by theory, it is thought that the germanium content being in a range of from 30% to 50% leads to increased selectivity of the etch stop layer and minimizes stress defects. In one or more embodiments, the etch stop layer has a thickness in a range of from 5 nm to 30 nm. The etch stop layer may serve as an etch stop for planarization (e.g., CMP), dry or wet etch during backside processing.

[0070] In one or more unillustrated embodiments, at operation 12, an epitaxial layer, e.g., epitaxial silicon, may be deposited on the etch stop layer. The epitaxial layer may have a thickness is a range of from 20 nm to 100 nm.

[0071] Referring to FIG. 1A and FIG. 2A, in one or more embodiments, at operation 14, at least one superlattice structure 101 is formed atop the top surface of the substrate 102 or on a top surface of the etch stop layer and epitaxial layer. The superlattice structure 101 comprises a plurality of semiconductor material layers 106 and a corresponding plurality of horizontal channel layers 104 alternatingly arranged in a plurality of stacked pairs. In some embodiments the plurality of stacked groups of

layers comprises a silicon (Si) and silicon germanium (SiGe) group. In some embodiments, the plurality of semiconductor material layers 106 comprise silicon germanium (SiGe), and the plurality of horizontal channel layers 104 comprise silicon (Si). In other embodiments, the plurality of horizontal channel layers 104 comprise silicon germanium (SiGe), and the plurality of semiconductor materials layers 106 comprise silicon (Si).

[0072] In some embodiments, the plurality of semiconductor material layers 106 and corresponding plurality of horizontal channel layers 104 can comprise any number of lattice matched material pairs suitable for forming a superlattice structure 204. In some embodiments, the plurality of semiconductor material layers 106 and corresponding plurality of horizontal channel layers 104 comprise from about 2 to about 50 pairs of lattice matched materials.

[0073] In one or more embodiments, the thickness of the plurality of semiconductor material layers 106 and the plurality of horizontal channel layers 104 are in the range of from about 2 nm to about 50 nm, in the range of from about 3 nm to about 20 nm, or in a range of from about 2nm to about 15 nm.

[0001] With reference to FIG. 1A and FIG. 2B, in one or more embodiments, at operation 16, the superlattice structure 101 is patterned to form an opening 108 between adjacent stacks 105. The patterning may be done by any suitable means known to the skilled artisan. As used in this regard, the term "opening" means any intentional surface irregularity. Suitable examples of openings include, but are not limited to, trenches which have a top, two sidewalls and a bottom. Openings can have any suitable aspect ratio (ratio of the depth of the feature to the width of the feature). In some embodiments, the aspect ratio is greater than or equal to about 5:1, about 10:1, about 15:1, about 20:1, about 25:1, about 30:1, about 35:1 or about 40:1.

[0074] Referring to FIG. 1A and FIG. 2C, at operation 18, a shallow trench isolation (STI) 110 is formed. As used herein, the term "shallow trench isolation (STI)" refers to an integrated circuit feature which prevents current leakage. In one or more embodiments, STI is created by depositing one or more dielectric materials (such as silicon dioxide) to fill the trench or opening 108 and removing the excess dielectric using a technique such as chemical-mechanical planarization.

[0075] With reference to FIG. 1A and FIG. 2D, in some embodiments, a replacement gate structure 113 (e.g., a dummy gate structure) is formed over and adjacent to the superlattice structure 101. The dummy gate structure 113 defines the channel region of the transistor device. The dummy gate structure 113 may be formed
5 using any suitable conventional deposition and patterning process known in the art.

[0076] In one or more embodiments, the dummy gate structure comprises one or more of a gate 114 and a poly-silicon layer 112. In one or more embodiments, the dummy gate structure comprises one or more of tungsten (W), cobalt (Co), molybdenum (Mo), ruthenium (Ru), titanium nitride (TiN), tantalum nitride (TaN),
10 titanium aluminum (TiAl), and N doped polysilicon.

[0077] Referring to FIG. 1A and FIG. 2E, in some embodiments, at operation 22, sidewall spacers 116 are formed along outer sidewalls of the dummy gate structure 113 and on the superlattice 101. The sidewall spacers 116 may comprise any suitable insulating materials known in the art, for example, silicon nitride, silicon oxide, silicon
15 oxynitride, silicon carbide, or the like. In some embodiments, the sidewall spacers are formed using any suitable conventional deposition and patterning process known in the art, such as atomic layer deposition, plasma enhanced atomic layer deposition, plasma enhanced chemical vapor deposition, low-pressure chemical vapor deposition, or isotropic deposition.

[0078] Referring to FIG. 1A and FIG. 2F, at operation 24, in one or more embodiments, source/drain trenches 118 are formed adjacent (i.e., on either side) the superlattice structure 101.

[0079] With reference to FIG. 1A and FIG. 2G, at operation 26, in one or more embodiments, the source/drain trenches 118 are deepened and expanded to form
25 cavities 119 under the superlattice structure 101. The cavities 119 may have any suitable depth and width. In one or more embodiments, the cavity 119 extends through the shallow trench isolation 110 into the substrate 102. In one or more embodiments, the cavity 119 etch and dummy fill extend below the shallow trench isolation 110 and maximally up to the silicon germanium (SiGe) etch stop layer, thus
30 enabling self-aligned contacts without touching the device.

[0080] The cavity 119 may be formed by any suitable means known to the skilled artisan. In one or more embodiments, a hard mask 117 is deposited to block the non V_{ss}/V_{dd} source/drain. In one or more embodiments, the hard mask 117 may comprise and suitable material known to the skill artisan. In some embodiments, the hard mask
5 117 is a resist. Once the hard mask 117 is formed, the cavity 119 is formed by etching.

[0081] The etch process of operation 26 may include any suitable etch process that is selective to the source drain trenches 118. In some embodiments the etch process of operation 26 comprises one or more of a wet etch process or a dry etch
10 process. The etch process may be a directional etch.

[0082] In some embodiments, the dry etch process may include a conventional plasma etch, or a remote plasma-assisted dry etch process, such as a SiCoNi™ etch process, available from Applied Materials, Inc., located in Santa Clara, Calif. In a SiCoNi™ etch process, the device is exposed to H_2 , NF_3 , and/or NH_3 plasma species,
15 e.g., plasma-excited hydrogen and fluorine species. For example, in some embodiments, the device may undergo simultaneous exposure to H_2 , NF_3 , and NH_3 plasma. The SiCoNi™ etch process may be performed in a SiCoNi™ Preclean chamber, which may be integrated into one of a variety of multi-processing platforms, including the Centura®, Dual ACP, Producer® GT, and Endura® platform, available
20 from Applied Materials®. The wet etch process may include a hydrofluoric (HF) acid last process, i.e., the so-called "HF last" process, in which HF etching of surface is performed that leaves surface hydrogen-terminated. Alternatively, any other liquid-based pre-epitaxial pre-clean process may be employed. In some embodiments, the process comprises a sublimation etch for native oxide removal. The etch process can
25 be plasma or thermally based. The plasma processes can be any suitable plasma (e.g., conductively coupled plasma, inductively coupled plasma, microwave plasma).

[0083] Referring to FIG. 1A and FIG. 2H, at operation 28, a sacrificial material 120 is deposited in the cavity 119. The sacrificial material may comprise any suitable material known to the skilled artisan. In some embodiments, the sacrificial material
30 120 comprises silicon germanium (SiGe). In one or more embodiments, the sacrificial material 120 has a high germanium (Ge) content. In one or more embodiments, the

amount of germanium is in a range of from 30% to 50%, including a range of from 35% to 45%. Without intending to be bound by theory, it is thought that the germanium content being in a range of from 30% to 50% leads to increased selectivity of the sacrificial material and minimizes stress defects.

- 5 **[0084]** In one or more embodiments, the sacrificial material 120 is doped with a dopant for lower contact resistance. In some embodiments, the dopant is selected from one or more of boron (B), gallium (Ga), phosphorus (P), arsenic (As), other semiconductor dopants, or combinations thereof. In specific embodiments, the sacrificial material 120 is silicon germanium having a germanium content in a range of
10 from 30% to 50% and doped with a dopant selected from one or more of boron (B), gallium (Ga), phosphorus (P), and arsenic (As).

- [0085]** Referring to FIG. 1A and FIG. 2I, at operation 30, an inner spacer layer 121 is formed on each of the horizontal channel layers 104. The inner spacer layer 121 may comprise any suitable material known to the skilled artisan. In one or more
15 embodiments, the inner spacer layer 121 comprises a nitride material. In specific embodiments, the inner spacer layer 121 comprises silicon nitride.

- [0086]** With reference to FIG. 2J and to FIG. 1A, at operation 32, in some embodiments, the embedded source/drain regions 122 form in a source/drain trench 118. In some embodiments, the source region 122 is formed adjacent a first end of the
20 superlattice structure 101 and the drain region 122 is formed adjacent a second, opposing end of the superlattice structure 101. In some embodiments, the source region and/or drain region 122 are formed from any suitable semiconductor material, such as but not limited to silicon (Si), germanium (Ge), silicon germanium (SiGe), silicon phosphorous (SiP), silicon arsenic (SiAs), or the like. In some embodiments,
25 the source/drain regions 122 may be formed using any suitable deposition process, such as an epitaxial deposition process. In some embodiments, the source/drain regions 122 are independently doped with one or more of phosphorus (P), arsenic (As), boron (B), and gallium (Ga).

- [0087]** In some embodiments, with reference to FIG. 1A and FIG. 2K, at operation
30 34, an inter-layer dielectric (ILD) layer 124 is blanket deposited over the substrate 102, including the source/drain regions 122, the dummy gate structure 113, and the

sidewall spacers 116. The ILD layer 124 may be deposited using a conventional chemical vapor deposition method (e.g., plasma enhance chemical vapor deposition and low-pressure chemical vapor deposition). In one or more embodiments, ILD layer 124 is formed from any suitable dielectric material such as, but not limited to, undoped
5 silicon oxide, doped silicon oxide (e.g., BPSG, PSG), silicon nitride, and silicon oxynitride. In one or more embodiments, ILD layer 124 is then polished back using a conventional chemical mechanical planarization method to expose the top of the dummy gate structure 113. In some embodiments, the ILD layer 124 is polished to expose the top of the dummy gate structure 113 and the top of the sidewall spacers
10 116.

[0088] The dummy gate structure 101 may be removed to expose the channel region 108 of the superlattice structure 101. The ILD layer 124 protects the source/drain regions 122 during the removal of the dummy gate structure 113. The dummy gate structure 113 may be removed using any conventional etching method
15 such as a plasma dry etch or a wet etch. In some embodiments, the dummy gate structure 113 comprises poly-silicon and the dummy gate structure 113 is removed by a selective etch process. In some embodiments, the dummy gate structure 113 comprises poly-silicon and the superlattice structure 101 comprises alternating layers of silicon (Si) and silicon germanium (SiGe).

[0089] Referring to FIG. 1B and FIG. 2L, at operations 38, the formation of the semiconductor device, e.g., GAA, continues according to traditional procedures with nanosheet release and replacement metal gate formation. Specifically, in one or more unillustrated embodiments, the plurality of semiconductor material layers 106 are selectively etched between the plurality of horizontal channel layers 104 in the
25 superlattice structure 101. For example, where the superlattice structure 101 is composed of silicon (Si) layers and silicon germanium (SiGe) layers, the silicon germanium (SiGe) is selectively etched to form channel nanowires. The plurality of semiconductor material layers 106, for example silicon germanium (SiGe), may be removed using any well-known etchant that is selective to the plurality of horizontal
30 channel layers 104 where the etchant etches the plurality of semiconductor material layers 106 at a significantly higher rate than the plurality of horizontal channel layers

104. In some embodiments, a selective dry etch or wet etch process may be used. In some embodiments, where the plurality of horizontal channel layers 104 are silicon (Si) and the plurality of semiconductor material layers 106 are silicon germanium (SiGe), the layers of silicon germanium may be selectively removed using a wet etchant such as, but not limited to aqueous carboxylic acid/nitric acid/HF solution and aqueous citric acid/nitric acid/HF solution. The removal of the plurality of semiconductor material layers 106 leaves voids between the plurality of horizontal channel layers 104. The voids between the plurality of horizontal channel layers 104 have a thickness of about 3 nm to about 20 nm. The remaining horizontal channel layers 104 form a vertical array of channel nanowires that are coupled to the source/drain regions 122. The channel nanowires run parallel to the top surface of the substrate 102 and are aligned with each other to form a single column of channel nanowires.

[0090] In one or more embodiments, a high-k dielectric is formed. The high-k dielectric can be any suitable high-k dielectric material deposited by any suitable deposition technique known to the skilled artisan. The high-k dielectric of some embodiments comprises hafnium oxide. In some embodiments, a conductive material such as titanium nitride (TiN), tungsten (W), cobalt (Co), aluminum (Al), or the like is deposited on the high-k dielectric to form the replacement metal gate 128. The conductive material may be formed using any suitable deposition process such as, but not limited to, atomic layer deposition (ALD) in order to ensure the formation of a layer having a uniform thickness around each of the plurality of channel layers.

[0091] Referring to FIG. 1B and FIG. 2M, at operation 38, the contact to transistor (CT) 132 and contact to gate (CG) 134 are formed.

[0092] With reference to FIG. 1B and FIG. 2N, at operation 40, the metal (M0) line 142 is formed and electrically connected to the via (V1) 144. This is similar to traditional processing, only M0 lines do not have power rails, thus creating ample space for signal lines.

[0093] With reference to FIG. 2O, at operation 42, the device 100 is rotated or flipped 180 degrees, such that the substrate 102 is now at the top of the illustration. Additionally, in one or more embodiments, the substrate 102 is planarized. The

planarization may be any suitable planarization process known to the skill artisan including, but not limited to, chemical mechanical planarization (CMP). In one or more embodiments, before rotating, the front side is bonded to copper (Cu) metallization at last layer, with hybrid bonding (oxide to oxide and Cu to Cu), or electrostatic dummy
5 wafer bonding.

[0094] With reference to FIG. 1B and FIG. 2P, at operation 44, an interlayer dielectric 146/148 is deposited on the backside. The interlayer dielectric materials 146/148 may be deposited by any suitable means known to one of skill in the art. The interlayer dielectric materials 146/148 may comprise any suitable materials known to
10 the skilled artisan. In one or more embodiments, the interlayer dielectric materials 146/148 comprise one or more of silicon nitride (SiN), carbide, or boron carbide, to allow high aspect ratio etch and metallization.

[0095] As illustrated in FIG. 2Q, at operation 46, in one or more embodiments, a backside power rail via 152 is formed. The via 152 may be formed by any suitable
15 means known to the skilled artisan. In one or more embodiments, the via 152 may be formed by patterning and etching the interlayer dielectric materials 146/148.

[0096] Referring to FIG. 1B and FIG. 2R, at operation 48, a damascene trench 154 is formed by expanding the via 152 to the contacts 120, 122. Expansion of the via 152 to form trench 154 increase the size of the open by at least double, permitting self-
20 alignment. In one or more embodiments, the via 152 has a starting size of about 16 nm by about 26 nm and is expanded to form trench 154 having a size of about 90 nm by about 74 nm.

[0097] The damascene trench 154 stops at the contacts 120, 122. The damascene trench 154 may have any suitable aspect ratio known the skilled artisan. In some
25 embodiments, the aspect ratio is greater than or equal to about 5:1, about 10:1, about 15:1, about 20:1, about 25:1, about 30:1, about 35:1 or about 40:1. In one or more embodiments, the critical dimensions of the damascene trench 154 are about 16 nm by about 26 nm, or about 10 nm by about 30 nm, or about 15 nm by about 30 nm. In one or more embodiments, the height of the back side vias depends on the original
30 epitaxial layer thickness deposited over the etch stop layer.

[0098] At operation 50, as illustrated in FIG. 2S, the sacrificial layer 120 is selectively removed to form an opening 156 over the source/drain 122. In one or more embodiments, if the sacrificial layer 120 is doped with one or more of Ga, B, P, it may be removed partially leaving some of the sacrificial layer 120 remained. Partial remove
5 of the sacrificial layer 120 allows the formation of a low resistivity contact to the remaining sacrificial layer 120 (e.g., SiGe).

[0099] At operation 52, as illustrated in FIG. 2T, a metal fill 156 is deposited in the opening 156 formed by removal of the sacrificial layer 120. The metal fill 156 may comprise any suitable material known to the skilled artisan. In one or more
10 embodiments, the metal fill 156 is selected from one or more of titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), tungsten (W), molybdenum (Mo), cobalt (Co), copper (Cu), ruthenium (Ru), and the like.

[00100] With reference to FIG. 1B and FIG. 2U, at operation 54, the backside metal line (M0) 160 is formed. Without intending to be bound by theory, it is thought that
15 locating the power rail on the backside allows for a gain in the area of the cell in a range of from 20% to 30%.

[00101] FIG. 3 illustrates a process flow diagram for a method 60 for thinning a semiconductor wafer in accordance with some embodiments of the present disclosure. FIGS. 4A-4E depict the stages of wafer thinning in accordance with some
20 embodiments of the present disclosure. The method 60 is described below with respect to FIGS. 4A-4E. FIGS. 4A-4E are cross-sectional views of an electronic device (e.g., a GAA) according to one or more embodiments. The method 60 may be part of a multi-step fabrication process of a semiconductor device. Accordingly, the method 60 may be performed in any suitable process chamber coupled to a cluster
25 tool. The cluster tool may include process chambers for fabricating a semiconductor device, such as chambers configured for etching, deposition, physical vapor deposition (PVD), chemical vapor deposition (CVD), oxidation, or any other suitable chamber used for the fabrication of a semiconductor device.

[00102] FIGS. 4A-4E are the fabrication steps of operations 62 thru 76 in FIG. 3.
30 Referring to FIG. 3, the method 60 of thinning the device 400 begins at operation 62. Referring to FIG. 3 and FIGS. 4A-4E, in the method of one or more embodiments,

transistors, e.g., gate all-around transistors, are fabricated using a standard process flow.

[00103] In some embodiments, a silicon wafer 402 is provided and, at operation 62, a buried etch stop layer 404 is formed on the silicon wafer. The buried etch stop layer 404 may comprise any suitable material known to the skilled artisan. In one or more embodiments, the buried etch stop layer 404 comprises silicon germanium (SiGe). In one or more embodiments, the buried etch stop layer 404 has a high germanium (Ge) content. In one or more embodiments, the amount of germanium is in a range of from 30% to 50%, including a range of from 35% to 45%. Without intending to be bound by theory, it is thought that the germanium content being in a range of from 30% to 50% leads to increased selectivity of the buried etch stop layer 404 and minimizes stress defects.

[00104] In one or more unillustrated embodiments, at operation 64, an epitaxial layer, e.g., epitaxial silicon, is deposited. At operation 66, the wafer is then subjected to device and front-end processing. Front-end processing may be the processes described above with respect to the method 6 illustrated in FIGS. 1A-1B and as depicted in cross-sectional views FIGS. 2A-2U.

[00105] Referring to FIG. 3 and FIG. 4B, at operation 68, in one or more embodiments, after front-end processing, the wafer 400 undergoes hybrid bonding, e.g., to copper or to an oxide, and then the wafer is advantageously thinned. Without intending to be bound by theory, it is thought that thinning the wafer advantageously provides the desired flatness and bonding for making a backside power rail possible.

[00106] In one or more embodiments, referring to FIG. 3. and FIG. 4C, to thin the wafer, at operation 70, the silicon substrate layer 402, which has a starting first thickness, t_1 , is ground to a second thickness, the second thickness, t_2 , less than the first thickness. The silicon substrate layer 402 may be ground by any suitable means known to the skilled artisan. In some embodiments, the silicon substrate layer 402 is subjected to chemical mechanical planarization (CMP), followed by etching and CMP buffing, to reduce the thickness of the silicon substrate layer 402 to a third thickness, t_3 , the third thickness less than the second thickness. In one or more embodiments, the first thickness is in a range of from 500 μm to 1000 μm . In one or more

embodiments, the second thickness is in a range of from 20 μm to 100 μm . In one or more embodiments, the third thickness is in a range of from 1 μm to 20 μm .

5 **[00107]** Referring to FIG. 3 and FIG. 4D, at operation 72, the buried etch stop layer 404 is selectively removed to expose the source/drain 408. At operation 74, contacts 410 are then prefilled with a metal, and metallization is conducted, as illustrated in FIG. 4E. In one or more embodiments, the contact 410 is prefilled with a metal is selected from one or more of titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), tungsten (W), molybdenum (Mo), cobalt (Co), copper (Cu), ruthenium (Ru), and the like.

10 **[00108]** FIGS. 5A-5E illustrate the alternative fabrication steps of operations 78-80 in FIG. 3. Referring to FIG. 3, the method 60 of thinning the device 400 begins at operation 62 and proceeds to operation 70, as detailed and illustrated in FIGS. 4A-4C.

15 **[00109]** After the silicon substrate 402 has been thinned by silicon grinding at operation 70, the method may proceed to operation 78 where a large mask 502 is formed on the buried etch stop layer 404. The mask 502 may comprise any suitable material known to the skilled artisan. In one or more embodiments, the mask 502 is selected from one or more of carbide, boron carbide, and silicon nitride.

20 **[00110]** At operation 80, the mask 502 is etched to form a plurality of thru silicon vias (TSV) 508, which extend to the buried etch stop layer 404. The vias 508 may be formed by any suitable means known to the skilled artisan. In one or more embodiments, the vias 508 are formed by etching. The TSVs, which are nano meter size, allow high density packaging of this formed device or other chips which are connected to this device, without need for traditional large TSVs, which add cost and space in regular 3D packaging.

25 **[00111]** At operation 82, referring to FIG. 3 and FIG. 5C, the buried etch stop layer 404 is selectively removed to form an opening 510. The buried etch stop layer 404 may be selectively removed by any suitable means known to the skilled artisan. In one or more embodiments, the buried etch stop layer 404 is selectively removed by etching the side of the device.

30 **[00112]** With reference to FIG. 3 and FIG. 5D, at operation 84, the mask 508 with the vias 508 is lifted off the device. Liftoff may occur by any suitable means known to

the skilled artisan. In one or more embodiments, liftoff allows for thinning of the wafer to a thickness in a range of from 50 nm to 100 nm. In one or more embodiments, the liftoff results in a thinned wafer that is substantially free of defects and scratches in the device 500. In one or more embodiments, liftoff requires lateral (isotropic etch) of the sacrificial layer 120 across the wafer, which is achieved by Selectra® etching.

[00113] FIG. 6 illustrates a process flow diagram for a method 600 of fabricating a semiconductor device in accordance with some embodiments of the present disclosure. FIGS. 7A-7D depict the stages of forming a deep via and backside contact in accordance with some embodiments of the present disclosure. The method 600 is described below with respect to FIGS. 7A-7D. FIGS. 7A-7D are cross-sectional views of an electronic device (e.g., a GAA) 700 according to one or more embodiments. The method 600 may be part of a multi-step fabrication process of a semiconductor device. Accordingly, the method 600 may be performed in any suitable process chamber coupled to a cluster tool. The cluster tool may include process chambers for fabricating a semiconductor device, such as chambers configured for etching, deposition, physical vapor deposition (PVD), chemical vapor deposition (CVD), oxidation, or any other suitable chamber used for the fabrication of a semiconductor device.

[00114] FIGS. 7A-7D are the fabrication steps of operations 602 thru 614 in FIG. 6. Referring to FIG. 6, the method 600 of forming a deep via and backside contact begins at operation 602. Referring to FIG. 6 and FIGS. 7A-7D, in the method 600 of one or more embodiments, transistors, e.g., gate all-around transistors, are fabricated, at operation 602, using a standard process flow. The device 700 may be formed according to the methods described with respect to FIGS. 1A-1B and FIGS. 2A-2Q.

[00115] At operation 604, as illustrated in FIG. 7A, at least one deep via 702 is formed in the frontside. The deep via 702 may have any suitable size or shape. The deep via 702 can have any suitable aspect ratio (ratio of the depth of the feature to the width of the feature). In some embodiments, the aspect ratio is greater than or equal to about 5:1, about 10:1, about 15:1, about 20:1, about 25:1, about 30:1, about 35:1 or about 40:1. In one or more embodiments, the critical dimensions of the deep via 702

are about 16 nm by about 16 nm, or about 10 nm by about 10 nm, or about 15 nm by about 15 nm, or about 20 nm by 20 nm.

[00116] Referring to FIG. 6 and FIG. 7B, at operation 606, the deep via 702 may be filled with a metal 704. The metal 704 may be any suitable metal known to the skilled artisan. In one or more embodiments, the metal 704 is selected from one or more of titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), tungsten (W), molybdenum (Mo), cobalt (Co), copper (Cu), ruthenium (Ru), and the like.

[00117] With reference to FIG. 6 and FIG. 7C, at operation 608, a bonding wafer 706 is bonded to the front side. The substrate 708, at operation 610, may be optionally thinned according to the method(s) described above with respect to FIG. 3. At operation 612, as illustrated in FIG. 7D, a contact 710 is then formed to electrically connect to the metal 704 in the deep via 702. The contact 710 may comprise any suitable material known to the skilled artisan. In one or more embodiments, contact 710 comprises a metal selected from one or more of titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), tungsten (W), molybdenum (Mo), cobalt (Co), copper (Cu), ruthenium (Ru), and the like. At operation 614, as illustrated in FIG. 7D, metallization then occurs.

[00118] In some embodiments, the methods are integrated such that there is no vacuum break. In one or more embodiments, the method 60 is the via etch (operation 80), removal of the buried sacrificial layer (operation 82) and the substrate release liftoff (operation 84), can be integrated such that there is no vacuum break between the operations.

[00119] Additional embodiments of the disclosure are directed to processing tools 300 for the formation of the GAA devices and methods described, as shown in FIG. 8. A variety of multi-processing platforms, including the Reflexion® CMP, Selectra® Etch, Centura®, Dual ACP, Producer® GT, and Endura® platform, available from Applied Materials® as well as other processing systems may be utilized. The cluster tool 300 includes at least one central transfer station 314 with a plurality of sides. A robot 316 is positioned within the central transfer station 314 and is configured to move a robot blade and a wafer to each of the plurality of sides.

[00120] The cluster tool 300 comprises a plurality of processing chambers 308, 310, and 312, also referred to as process stations, connected to the central transfer station. The various processing chambers provide separate processing regions isolated from adjacent process stations. The processing chamber can be any suitable chamber
5 including, but not limited to, a pre-clean chamber, a deposition chamber, an annealing chamber, an etching chamber, and the like. The particular arrangement of process chambers and components can be varied depending on the cluster tool and should not be taken as limiting the scope of the disclosure.

[00121] In the embodiment shown in FIG. 8, a factory interface 318 is connected to
10 a front of the cluster tool 300. The factory interface 318 includes chambers 302 for loading and unloading on a front 319 of the factory interface 318.

[00122] The size and shape of the loading chamber and unloading chamber 302 can vary depending on, for example, the substrates being processed in the cluster tool 300. In the embodiment shown, the loading chamber and unloading chamber 302 are
15 sized to hold a wafer cassette with a plurality of wafers positioned within the cassette.

[00123] Robots 304 are within the factory interface 318 and can move between the loading and unloading chambers 302. The robots 304 are capable of transferring a wafer from a cassette in the loading chamber 302 through the factory interface 318 to load lock chamber 320. The robots 304 are also capable of transferring a wafer from
20 the load lock chamber 320 through the factory interface 318 to a cassette in the unloading chamber 302.

[00124] The robot 316 of some embodiments is a multi-arm robot capable of independently moving more than one wafer at a time. The robot 316 is configured to move wafers between the chambers around the transfer chamber 314. Individual
25 wafers are carried upon a wafer transport blade that is located at a distal end of the first robotic mechanism.

[00125] A system controller 357 is in communication with the robot 316, and a plurality of processing chambers 308, 310 and 312. The system controller 357 can be any suitable component that can control the processing chambers and robots. For
30 example, the system controller 357 can be a computer including a central processing unit (CPU) 392, memory 394, inputs/outputs 396, suitable circuits 398, and storage.

[00126] Processes may generally be stored in the memory of the system controller 357 as a software routine that, when executed by the processor, causes the process chamber to perform processes of the present disclosure. The software routine may also be stored and/or executed by a second processor (not shown) that is remotely
5 located from the hardware being controlled by the processor. Some or all of the method of the present disclosure may also be performed in hardware. As such, the process may be implemented in software and executed using a computer system, in hardware as, e.g., an application specific integrated circuit or other type of hardware implementation, or as a combination of software and hardware. The software routine,
10 when executed by the processor, transforms the general-purpose computer into a specific purpose computer (controller) that controls the chamber operation such that the processes are performed.

[00127] In some embodiments, the system controller 357 has a configuration to control the rapid thermal processing chamber to crystallize the template material.

15 **[00128]** In one or more embodiments, a processing tool comprises: a central transfer station comprising a robot configured to move a wafer; a plurality of process stations, each process station connected to the central transfer station and providing a processing region separated from processing regions of adjacent process stations, the plurality of process stations comprising a template deposition chamber and a template
20 crystallization chamber; and a controller connected to the central transfer station and the plurality of process stations, the controller configured to activate the robot to move the wafer between process stations, and to control a process occurring in each of the process stations.

[00129] The use of the terms "a" and "an" and "the" and similar referents in the
25 context of describing the materials and methods discussed herein (especially in the context of the following claims) are to be construed to cover both the singular and the plural, unless otherwise indicated herein or clearly contradicted by context. Recitation of ranges of values herein are merely intended to serve as a shorthand method of referring individually to each separate value falling within the range, unless otherwise
30 indicated herein, and each separate value is incorporated into the specification as if it were individually recited herein. All methods described herein can be performed in any

suitable order unless otherwise indicated herein or otherwise clearly contradicted by context. The use of any and all examples, or exemplary language (e.g., "such as") provided herein, is intended merely to better illuminate the materials and methods and does not pose a limitation on the scope unless otherwise claimed. No language in the
5 specification should be construed as indicating any non-claimed element as essential to the practice of the disclosed materials and methods.

[00130] Reference throughout this specification to "one embodiment," "certain embodiments," "one or more embodiments" or "an embodiment" means that a particular feature, structure, material, or characteristic described in connection with the
10 embodiment is included in at least one embodiment of the disclosure. Thus, the appearances of the phrases such as "in one or more embodiments," "in certain embodiments," "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily referring to the same embodiment of the disclosure. Furthermore, the particular features, structures, materials, or
15 characteristics may be combined in any suitable manner in one or more embodiments.

[00131] Although the disclosure herein has been described with reference to particular embodiments, those skilled in the art will understand that the embodiments described are merely illustrative of the principles and applications of the present disclosure. It will be apparent to those skilled in the art that various modifications and
20 variations can be made to the method and apparatus of the present disclosure without departing from the spirit and scope of the disclosure. Thus, the present disclosure can include modifications and variations that are within the scope of the appended claims and their equivalents.

What is claimed is:

1. A method of forming a semiconductor device, the method comprising:
 - forming a superlattice structure on a top surface of a substrate, the superlattice structure comprising a plurality of horizontal channel layers and a
 - 5 corresponding plurality of semiconductor material layers alternately arranged in a plurality of stacked pairs;
 - forming a plurality of source trenches and a plurality of drain trenches adjacent to the superlattice structure on the substrate;
 - expanding at least one of the plurality of source trenches and at least
 - 10 one of the plurality of drain trenches to form a source cavity and a drain cavity;
 - depositing a sacrificial material in the source cavity and in the drain cavity;
 - forming a source region and a drain region;
 - forming at CT and CG in electrical contact with the source region and
 - 15 the drain region;
 - forming a damascene trench through the substrate;
 - at least partially removing the sacrificial material to form at least one opening extending to the damascene trench; and
 - depositing a metal in the at least one opening and in the damascene
 - 20 trench.
2. The method of claim 1, wherein expanding at least one of the plurality of source trenches and at least one of the plurality of drain trenches comprises depositing
- 25 a hard mask on at least one of the plurality of source trenches and on at least one of the plurality of drain trenches and not on at least one of the plurality of source trenches and at least one of the plurality of drain trenches, and etching the unmasked source trench and unmasked drain trench to form a source cavity and a drain cavity.
- 30 3. The method of claim 1, wherein the sacrificial material is fully removed.

4. The method of claim 1, wherein the sacrificial material comprises silicon germanium (SiGe).
- 5 5. The method of claim 4, wherein the silicon germanium (SiGe) has a germanium (Ge) content in a range of from 30% to 50%.
6. The method of claim 4, wherein the silicon germanium (SiGe) is doped with a dopant selected from the group consisting of boron (B), gallium (Ga), phosphorus (P), arsenic (As), and combinations thereof.
- 10 7. The method of claim 1, wherein forming the damascene trench comprises etching at least one via into the substrate and expanding the via to form the damascene trench.
- 15 8. The method of claim 1, wherein the plurality of semiconductor material layers and the plurality of horizontal channel layers independently comprise one or more of silicon germanium (SiGe) and silicon (Si).
- 20 9. The method of claim 1, wherein forming the source region and the drain region comprises growing an epitaxial layer thereon.
- 25 10. The method of claim 1, wherein the source region and the drain region are independently doped with one or more of phosphorus (P), arsenic (As), boron (B), and gallium (Ga).
11. The method of claim 1, further comprising forming a gate structure on a top surface of the superlattice structure.
- 30 12. The method of claim 11, further comprising forming a dielectric layer on the gate structure and on the superlattice structure.

13. The method of claim 12, wherein the gate structure comprises one or more of tungsten (W), cobalt (Co), molybdenum (Mo), ruthenium (Ru), titanium nitride (TiN), tantalum nitride (Ta₂N₅), titanium aluminum (TiAl), and N doped polysilicon.
- 5 14. The method of claim 1, wherein the metal comprises one or more of titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (Ta₂N₅), tungsten (W), molybdenum (Mo), cobalt (Co), copper (Cu), and ruthenium (Ru).
- 10 15. A method of forming a semiconductor device, the method comprising:
- forming a superlattice structure on a top surface of a substrate, the superlattice structure comprising a plurality of horizontal channel layers and a corresponding plurality of semiconductor material layers alternately arranged in a plurality of stacked pairs;
 - 15 forming a gate structure on a top surface of the superlattice structure;
 - forming a plurality of source trenches and a plurality of drain trenches adjacent to the superlattice structure on the substrate;
 - expanding at least one of the plurality of source trenches and at least one of the plurality of drain trenches to form a source cavity and a drain cavity;
 - 20 depositing a sacrificial material in the source cavity and in the drain cavity;
 - forming an inner spacer layer on each of the plurality of horizontal channel layers;
 - forming a source region and a drain region;
 - 25 forming an inter-layer dielectric layer on the substrate;
 - forming a replacement metal gate;
 - forming at CT and CG in electrical contact with the source region and the drain region;
 - forming a first metal line;
 - 30 rotating the semiconductor device 180 degrees;
 - planarizing the substrate;

- planarizing the substate;
depositing an interlayer dielectric material on the substrate;
forming a backside power rail via in the substrate;
expanding the backside power rail via to form a damascene trench;
5 removing the sacrificial material to form at least one opening; and
depositing a metal in the at least one opening and in the damascene trench.
- 10 16. The method of claim 15, wherein expanding at least one of the plurality of source trenches and at least one of the plurality of drain trenches comprises depositing a hard mask on at least one of the plurality of source trenches and on at least one of the plurality of drain trenches and not on at least one of the plurality of source trenches and at least one of the plurality of drain trenches, and etching the unmasked source trench and unmasked drain trench to form a
15 source cavity and a drain cavity.
17. The method of claim 15, wherein the sacrificial material comprises silicon germanium (SiGe).
- 20 18. The method of claim 17, wherein the silicon germanium (SiGe) has a germanium (Ge) content in a range of from 30% to 50%.
19. The method of claim 17, wherein the silicon germanium (SiGe) is doped with a dopant selected from the group consisting of boron (B), gallium (Ga),
25 phosphorus (P), arsenic (As), and combinations thereof.
20. The method of claim 15, wherein forming the source region and the drain region comprises growing an epitaxial layer thereon.