

INTERLEAVING BLOCK OPERATIONS IN A COMPUTER SYSTEM**ABSTRACT**

The present invention provides a computer system which includes a processor having an instruction set capable of "delaying" block-store instructions related to any outstanding block-load instruction(s). Accordingly, a method for interleaving block data transfers and processing steps which exploits the characteristics of the instruction set and architecture of the processor in order to increase efficiency and throughput of the computer system is provided. Hence by interleaving the block-store instruction of the previous data block with the block-load instruction of the next data block, the entire block transfer process can be streamlined.

(Fig. 3)