

DRAM CAM Cell With Hidden Refresh

Abstract of the Disclosure

A dynamic content addressable memory (DCAM) cell 200a has a topology that contains fewer than the 16 transistors of a typical SCAM cell. The DCAM 200a can perform a "hidden" refresh of stored data that does not delay nor interrupt the CAM search cycle, thereby providing SCAM-like performance. A non-destructive read operation avoids writing back stored data, because of a refresh-read operation. A reliable CAM search can be performed after a read operation and before or even while the refresh-data is being written back. Soft-error detection processes can be performed on each CAM entry during the pendency of the refresh cycle.

FIG. 2A