CLAIMS

1. An apparatus comprising:

a charge trap structure disposed above a substrate, the charge trap structure including:

a semiconductor pillar operable to conduct a current;

a charge trap region separated from the semiconductor pillar by a tunnel region;

a dielectric blocking region adjacent the charge trap region;

a gate adjacent to the dielectric blocking region operable to control storage of charge in the charge trap region, at least a portion of the gate being separated from at least a portion of an adjacent gate by at least a void; and

a dielectric barrier structured as a nanolaminate of multiple regions of different materials between the dielectric blocking region and the gate, with the dielectric barrier vertically contacting the gate, the adjacent gate, and extending from the gate to the adjacent gate, and with the dielectric barrier constructed to form at least a portion of a boundary of the void.

2. The apparatus of claim 1, wherein the void is contained within at least a portion of the dielectric barrier, at least a portion of the gate, at least a portion of the adjacent gate, and at least a portion of a dielectric region on the gate.

3. The apparatus of claim 1, wherein the dielectric barrier has a thickness in the range from about 15 angstroms to about 50 angstroms between the dielectric blocking region and the gate.

4. The apparatus of claim 1, wherein the tunnel region is an arrangement of one, two, or three dielectric regions.

5. The apparatus of claim 4, wherein the charge trap region is a nitride

region, the blocking dielectric region is an oxide region, the tunnel region includes an oxide and a nitride, the semiconductor pillar includes poly silicon, and the dielectric barrier includes aluminum oxide or a dielectric having a dielectric constant greater than that of aluminum oxide.

6. A memory device comprising:

a string of memory cells including a vertical pillar of semiconductor material; and

multiple charge trap structures arranged in a vertical stack with each charge trap structure vertically adjacent another one of the multiple charge trap structures in the vertical stack, each charge trap structure including:

a tunnel region adjacent and contacting the vertical pillar;

a charge trap region adjacent and contacting the tunnel region;

a dielectric blocking region adjacent and contacting the charge trap region;

a gate, at least a portion of the gate separated from at least a portion of the gate of an adjacent charge trap structure by at least a void; and

a dielectric barrier structured as a nanolaminate of multiple regions of different materials between the dielectric blocking region and the gate, with the dielectric barrier vertically contacting the gate, the gate of the adjacent charge trap structure, and extending from the gate to the gate of the adjacent charge trap structure, and with the dielectric barrier constructed to form at least a portion of a boundary of the void.

7. The memory device of claim 6, wherein the void is contained within at least a portion of the dielectric barrier, at least a portion of a dielectric region on at least a portion of the gate of the charge trap structure, and at least a portion of the dielectric region that is also on at least a portion of the gate of the adjacent charge trap structure.

8. The memory device of claim 6, wherein the tunnel region extends along the vertical pillar of semiconductor material and extends through the other

charge trap structures as the tunnel region of each charge trap structure of the string.

9. The memory device of claim 6, wherein the charge trap region extends along the vertical pillar of semiconductor material and extends through the other charge trap structures as the charge trap region of each charge trap structure of the string.

10. The memory device of claim 6, wherein the dielectric blocking region extends along the vertical pillar of semiconductor material and extends through the other charge trap structures as the dielectric blocking region of each charge trap structure of the string.

11. The memory device of claim 6, wherein the dielectric barrier includes aluminum oxide.

12. The memory device of claim 6, wherein the dielectric barrier includes a dielectric material having a dielectric constant greater than that of aluminum oxide.

13. The memory device of claim 6, wherein the vertical pillar is structured as a doped hollow channel.

14. The memory device of claim 6, wherein the vertical pillar includes poly silicon surrounding a dielectric material.

15. The memory device of claim 6, wherein the gates are incorporated in access lines of a memory array of the memory device.

16. A method comprising:

forming a charge trap structure above a substrate, including:

forming a dielectric barrier structured as a nanolaminate of

multiple regions of different materials on a wall of an opening in a material stack;

forming a dielectric blocking region on and contacting the dielectric barrier;

forming a charge trap region on and contacting the dielectric blocking region;

forming a tunnel region on and contacting the charge trap region;

forming a semiconductor pillar on and contacting the tunnel region, the semiconductor pillar separated from the charge trap region by the tunnel region, the semiconductor pillar operable to conduct a current;

forming a gate on and contacting the dielectric barrier, at least a portion of the gate separated from at least a portion of an adjacent gate by at least a void, the gate separated from the dielectric blocking region by the dielectric barrier, the gate operable to control storage of charge in the charge trap region, with the dielectric barrier vertically contacting the gate, the gate of the adjacent charge trap structure, and extending from the gate to the gate of the adjacent charge trap structure, with the dielectric barrier constructed to form at least a portion of a boundary of the void.

17. The method of claim 16, wherein the method includes:

forming the opening in the material stack with the material stack having alternating sacrificial regions and isolation dielectrics;

removing sacrificial regions adjacent to the dielectric barrier using a chemistry and process to remove the sacrificial region substantially without removing material for the dielectric barrier;

forming the gate in a region in which a sacrificial region has been removed and forming the adjacent gate in a region in which another one of the sacrificial regions has been removed;

removing material from between the gate and the adjacent gate to form an open area by a chemistry and process to remove the isolation dielectrics previously formed between adjacent sacrificial regions without substantially removing the material for the dielectric barriers, without substantially removing

material of the gate, and without substantially removing material of the adjacent gate; and

forming a dielectric in at least a portion of the open area to form the void.

18. The method of claim 16, wherein forming the dielectric barrier includes forming aluminum oxide.

19. The method of claim 16, wherein forming the dielectric barrier includes forming a dielectric material having a dielectric constant greater than that of aluminum oxide.

20. The method of claim 16, wherein forming the charge trap region includes forming a dielectric nitride as the charge trap region.

21. The method of claim 16, wherein forming the gate includes forming tungsten as a portion part of the gate.

22. The method of claim 21, wherein forming the gate includes forming a titanium nitride region on and contacting the dielectric barrier and forming the tungsten on the titanium nitride region.

23. A method comprising:

forming a stack of materials with an opening surrounded by materials to form tunnel regions, charge trap regions, dielectric blocking regions, and dielectric barriers of multiple charge trap structures of a string of memory ~~cells,~~ cells of a memory device, including a first charge trap structure, with each trap structure of the string, except for the first charge trap structure in the string, disposed above another one of the multiple charge trap structures, wherein the materials forming the tunnel regions, the charge trap regions, the dielectric blocking regions, and the dielectric barriers of the multiple charge trap structures vertically run continuously from a topmost charge trap structure of the string to a bottommost charge trap structure of the string at completion of formation of the memory device;

forming multiple gates contacting material for the dielectric barriers after forming the tunnel regions, the charge trap regions, the dielectric blocking regions, and the dielectric barriers for the multiple charge trap structures with each dielectric barrier structured as a nanolaminate of multiple regions of different materials;

removing material from the stack such that at least a portion of each gate of the multiple gates is separated from at least a portion of a vertically adjacent gate of the multiple gates by an open area, exposing portions of the material for the dielectric barriers; and

processing the stack of materials further such that a portion of each open area is left as a void between gates of adjacent charge trap structures, with the material for the dielectric barriers vertically contacting the gates of adjacent charge trap structures such that the material for the dielectric barriers forms at least a portion of a boundary of each void.

24. The method of claim 23, wherein the material for the dielectric barrier includes aluminum oxide.

25. The method of claim 23, wherein the material for the dielectric barrier includes a dielectric material having a dielectric constant greater than that of aluminum oxide.

26. The method of claim 23, wherein forming multiple gates contacting material for the dielectric barriers and removing material such that each gate is separated from a vertically adjacent gate of the multiple gates includes, with the stack of material including alternating sacrificial regions and isolation dielectrics adjacent to the material to form tunnel regions, charge trap regions, dielectric blocking regions, and dielectric barriers:

removing sacrificial regions adjacent to the material for the dielectric barriers using a chemistry and process to remove the sacrificial region substantially without removing material for the dielectric barrier;

forming gate material in each region in which a sacrificial region is removed; and

removing material from between each gate by a chemistry and process to remove the isolation dielectrics previously formed between adjacent sacrificial regions without substantially removing the material for the dielectric barriers and without substantially removing the gate material in each region.

27. The method of claim 26, wherein forming the gate material in each region in which the sacrificial region is removed includes forming the gate material coupled to access lines in a memory array for a memory device.

28. The method of claim 23, wherein the method includes sealing, with a dielectric, the open area between gates of adjacent charge trap structures in forming the void.