Description

This invention relates to integrated semiconductor memory circuits and more particularly to a memory with a very high density of cells, each of which employs means for storing a binary digit of information in a trench or groove formed in a semiconductor substrate.

Integrated semiconductor memory circuits, particularly those employing cells which include essentially a storage capacitor and a switch have achieved high memory cell densities. One of the simplest circuits for providing a small dynamic memory cell is described in commonly assigned US-A-3 387 286, filed July 14, 1967, by R. H. Dennard. Each cell employs a storage capacitor and a field effect transistor acting as a switch to selectively connect the capacitor to a bit/sense line.

In also commonly assigned US-A-3 811 076 by W. M. Smith, and US-A-3 841 926 by R. R. Garnache and W. M. Smith, both filed on January 2, 1973, there is disclosed a one device field effect transistor memory cell of the type described in the hereinabove identified Dennard patent which utilizes a layer of doped polysilicon and an N+ diffusion region in a P type conductivity semiconductor substrate separated by a dielectric medium disposed on the surface of the semiconductor substrate for forming the storage capacitor of the cell. The polysilicon layer extends beyond the storage capacitor to act as a field shield between adjacent cells by applying a negative bias or fixed negative potential to the polysilicon layer. The N+ diffusion region of the storage capacitor is formed by using a doped segment of an insulating layer disposed on the surface of the semiconductor substrate and outdiffusing the dopant into the substrate.

Although the cells described hereinabove do provide memories having a high density of cells in a planar or two dimensional arrangement, yet each cell does require a significant given area of semiconductor substrate surface. To reduce the size of the given surface area for each cell, structures have been made wherein a semiconductor device or a cell is formed in a three dimensional arrangement. In commonly assigned US-A-4 295 924, filed on December 17, 1979 by R. R. Garnache and D. M. Kenney, there is disclosed a semiconductor device located within a groove or trench with a self-aligned conductive layer formed on a wall of the trench either directly or on a supporting insulating layer as an element of the device. A memory cell formed in a groove or trench is described in commonly assigned US-A-4 335 450, filed on January 30, 1980, by D. R. Thomas, wherein there is disclosed a cell having a transistor disposed on a sidewall of a groove or trench with the storage node disposed below the transistor. Also US-A-4 327 476, filed on November 28, 1980, describes a vertical cell having the storage capacitor in a well or trench.

Furthermore, commonly assigned US-A-4 462 040, filed on March 30, 1980, by I. T. Ho and J. Riseman, discloses a one device dynamic random access memory utilizing a trench having vertical sidewalls with the storage capacitor and the transfer device located within the trench, and US-A-4 271 418, filed on October 29, 1979, and US-A-4 225 945, filed on June 6, 1977, and commonly assigned US-A-4 785 337, by D. M. Kennedy, and IBM Technical Disclosure Bulletin, Vol. 27, No. 2, July 1984, pp. 1313 to 1320, by C.G. Jambotkar, teach a one device memory cell formed in a groove or trench with the storage node located at the bottom of the trench, the bit/sense line at the top of this structure and the transfer device on the sidewall of the trench.

Commonly assigned US-A-4 811 067, by B. F. Fitzgerald, K. Y. Nguyen and S. V. Nguyen describes a dynamic memory cell wherein the switching device is located at the bottom of the trench, with the storage capacitor and the bit/sense line being formed along opposite sidewalls of the trench.

US-A-4 673 962, filed March 21, 1985, discloses a memory structure wherein a pair of cells are formed on a semiconductor substrate, each cell having a polysilicon storage node located on a sidewall of a trench opposite that of the other cell.

Commonly assigned US-A-4 769 786, filed on July 15, 1986, by R.R. Garnache and D.M. Kenney, discloses a memory circuit wherein each of the memory cells requires only two lithographic squares of the surface of a semiconductor substrate, wherein one lithographic square is defined by the intersection of two orthogonally arranged lithographic lines, each line being of a given width, e.g., less than a micron, as used in forming elements of devices in integrated semiconductor circuits. In the memory circuit of this patent, two memory cells are formed at the intersection of a trench and a bit/sense line. In the hereinabove cited prior art, none of the references except for the commonly assigned US-A-4 769 786 and the US-A-4 673 962 disclose a very small memory cell which utilizes a semiconductor substrate surface area of less than four lithographic squares.

In the EP-A- 0 180 026 a DRAM cell is disclosed, that needs only a small area. This device consists of a capacitor for storage occupying only a small part of the surface area, because it is located at the mayor sidewalls of a trench. Field effect transistors are also provided at the sidewalls of the trench, for loading and discharging the capacitor.

These memory cells allow already to produce high density memories. However, the space needed per DRAM- cell is not only determined by the resolution of the lithographic process applied for its production, but also by the semiconductor topography to connect that cell with word-lines and bit lines to obtain a DRAM matrix

circuit.

The problem of the invention is to provide a memory with memory cells needing less space, which are adapted in geometry to allow easy connection to bit/sense line and wordline decoders when they are arranged in an array. Additionally, the capacity of bit/sense lines and word lines shall be minimized in order to obtain an improved signal to noise ratio.

The problem is solved by a memory according to claim 1. Further improvements of the invention are characterized in the dependent claims.

The different geometry of the memory according to the invention compared to the memory cells of the EP-A- 0180 026 allows to integrate two independent capacitors and associated field effect transistors on opposite sidewalls of the trench. The bit/sense lines and wordlines required allow to be arranged in a simple matrix structure, with reduced capacitive coupling. Because of the special structure only two lithographic squares of the surfaces of a semiconductor substrate are needed for one cell. In addition the production of a memory array allows to use only simple processing techniques.

Ways of carrying out the invention are described in detail below with reference to drawings which illustrate only specific embodiments in which:

Fig. 1	is a circuit diagram of a dynamic one device memory cell indicating the principle elements thereof,
Fig. 2	is a sectional view taken through line 2-2 of Fig. 3 of two dynamic cells of the structure of the present invention,
Fig. 3	is a plan view of two cells of the present invention disposed on opposite sidewalls of a trench,
Fig. 4	is a plan view of a 2x2 array of cells, each cell being of the type illustrated in Figs. 2 and 3, and
Figs. 5 and 6	are sectional views of the array illustrated in Fig. 4 taken through lines 5-5 and 6-6, respectively.

Referring to the drawings in more detail, there is shown in Fig. 1 a basic circuit diagram of a well known one device dynamic memory cell 10 which includes a field effect transistor 12 having a gate 14, a storage capacitor 16 having a conductive plate 18 and a storage node 20, and a bit/sense line 22. As is known, to store a binary digit in the storage capacitor 16, a high or low voltage is applied to the bit/sense line 22 and the transistor 12 is turned on to charge the storage node 20 if a high voltage is applied to the bit/sense line 22, indicating the presence of, say, a 1 digit, otherwise the storage node 20 remains uncharged, indicating the presence of a stored 0 digit. To read information from the storage capacitor 16, the bit/sense line 22 is charged to a high voltage and the transistor 12 is turned on. If the bit/sense line 22 is discharged, a sense amplifier (not shown) connected to the bit/sense line 22 will indicate the presence of a 0 digit in the storage capacitor 16. If the bit/sense line 22 remains charged, the storage capacitor 16 is storing a 1 digit.

In accordance with the teachings of this invention, a novel vertical structure of the memory circuit of Fig. 1 is illustrated in Figs. 2 and 3, wherein Fig. 3 is a plan view of the structure and Fig. 2 is a sectional view taken through line 2-2 of Fig. 3. As shown in Figs. 2 and 3, two dynamic memory cells 10A and 10B are disposed on opposite sidewalls within a trench 24 formed in a semiconductor substrate 26, preferably made of silicon and having a P- conductivity. Cell 10A includes the field effect transistor 12, the storage capacitor 16 and the bit/sense line 22, formed as an elongated N+ diffusion region within the semiconductor substrate 26 along the upper portion of a first sidewall of the trench 24. A word line 28, preferably made of doped polysilicon, tungsten silicide (WSi_2), or titanium silicide ($TiSi_2$), or a combination of a doped polysilicon layer 28' and a silicide layer 28", as indicated in Fig. 2 of the drawings, or of copper-doped aluminum, is disposed at the upper or major surface of the semiconductor substrate 26 arranged orthogonally within respect to the longitudinal axis of the trench 24 in contact with the gate 14 of the transistor 12.

The transistor 12 and the capacitor 16 are located within the trench 24 on the first sidewall, with the transistor 12 being disposed between the bit/sense line 22 and the storage capacitor 16. The transistor 12 includes the gate 14, which is also preferably made of P-doped polysilicon, tungsten silicide (WSi_2) or titanium silicide ($TiSi_2$), or of copper-doped aluminum, separated from the first sidewall of the trench 24 by a thin insulating layer 30, preferably a triple insulating layer made of silicon dioxide, silicon nitride and silicon dioxide, or a dual layer made of silicon dioxide and silicon nitride. If desired, the gate 14 and the word line 28 may form an integral unit, as indicated in Fig. 2 of the drawings, and made in a single process step. The storage capacitor 16 includes the storage node 20 made in the form of an N+ diffusion region disposed along the first sidewall of the trench 24 and the conductive plate 18, which may be made of P-doped polysilicon including boron, separated from the storage node or N+ diffusion region 20 by a thin insulating layer 32, preferably also a dual or triple insulating layer made of silicon dioxide and silicon nitride. The storage node or N+ diffusion region 20 acts as the source and the bit/sense line or N+ diffusion region 22 acts as the drain of the transistor 12.

A layer of insulation 34 is disposed between the bottom of the trench 24 and the conductive plate 18 to isolate the conductive plate 18 from the semiconductor substrate 26 and a layer of insulation 36 is preferably grown, to a thickness of about 100 nm, as silicon dioxide on the top of the polysilcon plate 18 so as to isolate the transistor gate 14 from the polysilicon plate 18, and an insulating layer 38, preferably made of silicon dioxide, is disposed between the upper or major surface of the semiconductor substrate 26 and the word line 28, with silicon dioxide spacers 40 and 40' insulating the gate 14 from the bit/sense lines 22 and 22', respectively.

The second dynamic memory cell 10B, also located within the trench 24, has a field effect transistor 12' and a storage capacitor 16' disposed on the second or opposite sidewall of the trench 24, with the gate 14, the conductive plate 18 and the word line 28 being common to both cells 10A and 10B. The second transistor 12' includes the gate 14 separated from the second sidewall of the trench 24 by a thin insulating layer 30'. The storage capacitor 16' includes the storage node 20', made in the form of an N+ diffusion region and disposed along the second sidewall of the trench 24 within the semiconductor substrate 26, and the conductive plate 18 separated from the N+ diffusion region 20' by a thin insulating layer 32'. A bit/sense line 22', formed as an elongated N+ diffusion region within the semiconductor substrate 26 along the upper portion of the second sidewall of the trench 24, serves as the drain of the field effect transistor 12', while the storage node 20 serves as the source of the transistor 12'.

As more clearly indicated in Fig. 3 of the drawings, the bit/sense lines 22 and 22' extend in a vertical direction along the longitudinal axis of the trench 24 and orthogonal to the direction of the word line 28.

It can be seen from Figs. 2 and 3 that two very compact one device dynamic memory cells 10A and 10B are provided on opposite sidewalls of the trench 24 isolated from each other, and from any adjacent cells, wherein all elements of the two cells 10A and 10B are located within the trench 24 except for the connecting word line 28. The trench 24 may be made as deep and as wide as necessary to provide a storage capacitor of desired size and a transistor of desired switching characteristics. In one arrangement of the structure of the present invention, the depth of the trench 24 is preferably 7 μm, with a width of 1 μm, and the width of the channel of the transistors 12 and 12' being 1 μm, with the length of the channel also being equal to 1 μm. Each of the thin layers of insulation 30 and 30' forming the gate insulating medium of the transistors 12 and 12', respectively, has a total thickness of about 18 nm, with the thickness of the silicon dioxide layers each being 5 nm and the thickness of the silicon nitride layer being 8 nm when the insulating layer 30 is made in the form of the triple insulating layers. The thickness of each of the insulating or dielectric layers 32 and 32' of the storage capacitors 16 and 16' and of insulation layer 34 at the bottom of the trench 24 is preferably 13 nm, e. g., 4 nm of silicon dioxide, 7 nm of silicon nitride and 2 nm of silicon dioxide. The layers of insulation 30 and 30', 32 and 32' and 34 may also be made of the same materials and have the same thicknesses, if desired. The N+ diffusion regions 20 and 20' each extend into the substrate 26 about 150 nm from their respective sidewalls of the trench 24. With a spacing between adjacent cells of an array of cells along the word line direction equal to one micron or less and along the bit/sense line direction, which is orthogonal to that of the word line direction, equal to 1 μm or less, the size of one cell at the surface of the semiconductor substrate may be made equal to 2 μm^2 microns or less, which is produced when the lithographic line width is equal to 1 μm or less. Furthermore, the capacitance of each of the storage capacitors 16 and 16' versus the capacitance of the bit/sense line 22, assuming 64 cells per bit/sense line, provides a very desirable transfer ratio of about 10 to 20%.

Fig. 4 is a plan view of an array of cells, each cell being of the type illustrated in Figs. 2 and 3 of the drawings, wherein like reference characters refer to similar elements, with two cells 10A and 10B aligned in the horizontal direction along the first word line 28 and two cells 10C and 10D aligned in the horizontal direction along a second word line 28A. The space between the word lines of the array, such as between the word lines 28 and 28A is filled with any suitable insulating material 42, e.g., a polyimide or reflowable borophosphosilicate glass (BPSG). The cells 10A and 10C are also aligned in the vertical direction along bit/sense line 22 and the cells 10B and 10D are aligned in the vertical direction along bit/sense line 22'. As is known, each of the word lines 28 and 28A is connected to word decoder and driver circuits 44 for selective actuation and each of the bit/sense lines 22 and 22' may be connected to known bit line decoder, precharge and sense amplifier circuits 46.

Fig. 5 is a sectional view of Fig. 4 taken through line 5-5 thereof and Fig. 6 is a sectional view of Fig. 4 taken through line 6-6 thereof to more clearly show the details of the elements of the cells 10A, 10B, 10C and 10D of the array.

By referring to Figs. 4 and 5, wherein Fig. 5 is a sectional view taken orthogonally through the trench 24 in an isolation region between storage nodes of the cells, it can be readily seen that the bit/sense lines 22 and 22' pass through the isolation region along the upper portion of the sidewalls of the trench 24 separated by the insulating material 42 and that the N+ storage nodes 20 and 20' do not exist in the isolation region. The conductive plate 18 is disposed in the isolation region at the bottom of the trench 24 insulated from the semiconductor substrate 26 by insulating layers 32, 32' and 34.

By referring to Figs. 4 and 6 of the drawings, wherein Fig 6 is a sectional view taken parallel to a sidewall of the trench 24 through the storage nodes 20' and the bit/sense line 22', it can be seen that the bit/sense line 22' indicated as an elongated N+ diffusion region passes along the upper portion of the semiconductor substrate 26 over the storage node 20' of both transistors 10B and 10D but spaced therefrom, with the word lines 28 and 28A aligned over the storage node 20' of the memory cells 10B and 10D, respectively. The word lines 28 and 28A are separated from the upper or major surface of the semiconductor substrate 26 by the insulating layer 38. The sectional views of the polysilicon layer 28' and of the silicide layer 28" of the word lines 28 and 28A may also be readily seen in Fig. 6 of the drawings. The length of the channel of transistor 12' of each of the memory cells 10B and 10D can be seen as the distance between the N+ diffusion region of the bit/sense line 22' and the N+ diffusion region or storage node 20'.

As is known, to write into or read from a random access memory array as shown in Fig. 4, word line decoder and driver circuits 44 and bit line decoder, precharge and sense amplifier circuits 46 of any known type may be used to select any one or more of the cells 10A, 10B, 10C and 10D. Furthermore, it should be understood that the trench 24 may contain hundreds of memory cells along each of the two sidewalls thereof to which the bit/sense lines 22 and 22' may be connected and that hundreds of similar spaced apart trenches may be arranged parallel to the trench 24 containing similar memory cells to which the word lines 28 and 28A may be connected. The trenches 24 may be spaced apart by one lithographic line, i. e., by as short a distance as 1 μm or less. Furthermore, it should be understood that in order to more effectively utilize the area of the upper or major surface of the semiconductor substrate 26, bit line decoder, precharge and sense amplifier circuits 46 may be located at one end of alternate trenches 24, while the remaining trenches 24 have the bit line decoder, precharge and sense amplifier circuits 44 disposed at the opposite end of the trenches 24. If desired, the word line decoder and driver circuits 44 may also be located at different ends of the word lines 28 and 28A in a similar manner.

Any known process may be used to make the memory cells of the present invention. In one particular process, boron ions with an energy of 10 MeV are implanted through the major surface of the semiconductor substrate 26 to produce a concentration of 10^{17} cm^{-3} to a depth of about 7 μm. Preferably, an epitaxial silicon layer of this thickness and doping is grown using conventional techniques. Then a shallow trench having a depth equal to about the desired width of one of the bit/sense lines 22 and 22' is etched into the semiconductor substrate 26 by known reactive ion etching techniques in a chlorine-based ambient using an oxide masking layer 38 of about 400 nm. By using known chemical vapor deposition techniques, a relatively thick oxide layer, preferably silicon dioxide, doped with about 1% arsenic and about 150 nm thick, is deposited conformally along the sidewalls and bottom of the shallow trench. A known reactive ion etching process is then used to form arsenic-doped oxide sidewall spacers 40 and 40', as indicated in Figs. 2 and 5 of the drawings. Again by using reactive ion etching techniques, the shallow trench is further etched to its full depth as trench 24 illustrated in Figs. 2 and 5 of the drawings. A thin arsenic-doped oxide layer (also about 1% arsenic doped), about 15 nm thick, is deposited conformally in the trench 24, followed by a reactive ion etch to remove the thin arsenic-doped layer from the upper planar surface of the substrate 26 and from the bottom of the trench 24. The trench 24 is filled with any suitable photoresist, and with the use of any known multilayer or multilevel photoresist (MLR) process, including a non-erodable layer, a deep photoresist pattern of lines is cut, by any suitable etching process, orthogonal to the longitudinal axis of the trench 24 to a depth extending to the bottom of the trench 24. This deep photoresist pattern of lines is used to define the storage nodes 20 and 20', and by subsequently etching away the exposed thin arsenic-doped oxide layer, e.g., with the use of dilute buffered hydrogen fluoride, from the sidewalls of the trench 24 within the deeply etched photoresist pattern of lines, discrete segments of arsenic-doped oxide remain on the sidewalls of the trench 24 for use in forming the storage nodes 20 and 20'. The remainder of the photoresist in which the deep photoresist pattern was formed is now removed and the trench 24 is refilled with a new photoresist and reactively ion etched uniformly down into the trench 24 to a depth desired for the upper edge of the storage nodes 20 and 20'. With the upper edge of the storage nodes 20 and 20' defined by the level of this new photoresist, all thin arsenic-doped oxide layer is then removed from the upper portions of the sidewalls of the trench 24 with the use of any appropriate wet etchant. Since the arsenic-doped oxide sidewall spacers 40 and 40' are much thicker than the thin arsenic-doped oxide layer, spacers 40 and 40' will remain substantially undisturbed when etching the thin arsenic-doped oxide layer. The new photoresist is then stripped or removed from the trench 24 and by using any suitable drive-in process the arsenic from the thin arsenic-doped oxide layer and from the thick sidewall spacers 40 and 40' is introduced into the semiconductor substrate 26 to form the storage nodes 20 and 20' and the bit/sense lines 22 and 22', respectively. Thereafter, the thin doped oxide layer is stripped from the sidewalls of the trench 24 and the thin insulating layers 32, 32' and 34 are deposited conformally within the trench 24 by sequentially applying very thin layers of silicon dioxide, silicon nitride and silicon dioxide, with the layers 32 and 32' acting as the dielectric for the storage capacitors 16 and 16'.

The trench 24 is then filled with doped polysilicon and planarized by chemical-mechanical polishing, and the polysilicon is etched to a suitable depth within the trench 24 so as to establish the upper surface of the conductive plate 18 at a level slightly below the upper edge of the storage nodes 20 and 20', as indicated in Fig. 2 of the drawings. In order to provide an electrical contact area to the conductive plate 18, a portion of the trench 24 is masked prior to performing the last etching step. The upper surface of the conductive plate 18 is then covered with the layer of insulation 36 which may be appropriately grown on the polysilicon conductive plate 18 by any known oxidation process, increasing the thickness of the insulating layer 38 on the surface of the substrate 26.

The portions of the thin insulating layers 32 and 32' extending above the layer of insulation 36 are now removed by using any suitable wet etching process and new thin insulating layers 30 and 30' are deposited which will act as the gate dielectric of the transistors 12 and 12'. However, if desired, the extended thin insulating layers 32 and 32' may be used as the gate dielectric of the transistors 12 and 12'. The gate 14 of the transistors 12 and 12' and the word lines 28 and 28' are now made by again depositing doped polysilicon into the trench 24 and onto the upper or major surface of the semiconductor substrate 26, and then printing and etching the polysilicon into parallel strips arranged orthogonal to the longitudinal axis of the trench 24, as indicated more clearly in Fig. 2 of the drawing. If preferred, as stated hereinabove, the word lines 28 and 28A may include dual or multiple layers of conductive material so as to provide more highly conductive word lines 28 and 28A. In this instance, after the polysilicon has been deposited as polysilicon layer 28', about 400 nm thick, for the word lines 28 and 28A and prior to etching, a layer of tungsten silicide or titanium silicide, about 100 nm thick, is deposited over the polysilicon layer 28' to form a more conductive layer 28" in the word lines 28 and 28A, as indicated in Figs. 2 and 6 of the drawings. A polyimide or a reflowable insulating material such as borophosphosilicate glass is then used to fill the voids in the trench 24 between the word lines 28 and 28A and planarized. This latter insulating material may also be used to cover the word lines 28 and 28A with a layer about 500 nm thick. As is necessary, a first level metal layer, a passivating layer and a second level metal layer may be formed on the top of the resulting structure in the usual manner to provide appropriate electrical connections to the various elements of the memory.

It should be noted that an appropriate mask is needed after the arsenic-doped sidewall oxide spacers 40 and 40' have been formed in order to remove the doped sidewall spacers at the ends of the trench 24 to separate the bit/sense lines 22 and 22' from each other. Furthermore, another mask is needed after the arsenic-doped sidewall oxide spacers 40 and 40' have been formed to define an expanded ion implanted region electrically connected to the bit/sense lines 22 and 22' to serve as a contact area for the bit/sense lines 22 and 22' at the ends thereof. It can be readily seen in accordance with the teachings of this invention that an improved memory cell has been provided in a vertical structure within a semiconductor substrate requiring a very small cell substrate surface area, i.e., only two lithography squares by forming within a trench or groove the storage means, the switching means and the bit/sense line of the cell, with the word line disposed on the surface of the semiconductor substrate and arranged orthogonal with respect to the the longitudinal axis of the trench or bit/sense line. With the word line disposed on the surface of the semiconductor substrate, its dimensions are not subjected to the restraints placed on it as it would have were it located within a small trench, such as trench 24, and, therefore, the word line can be more readily made as a thick, highly conductive line. This arrangement is particularly important in memories since the word lines in a memory array are very long and usually significantly longer than the length of the bit/sense lines. Accordingly, it is important for high speed memories to have word lines with a resistance which is as low as possible.

Another advantage of the very dense memory of the present invention is that capacitive coupling is minimized between the bit/sense lines because the doped semiconductor substrate 26 and the word line arrangements maintain a significant shielding effect, not provided by other dense layouts, such as that shown in the hereinabove cited commonly assigned US-A-4 769 786, resulting in an improved signal to noise ratio.

It can be further seen in accordance with the teachings of this invention that a high density, two square memory cell has been provided in a memory array having a highly conductive word line which uses simple, known process steps. For example, the process used does not require forming thick oxide layers deep within the small trenches, since as described hereinabove, only thin insulating layers need be formed in the lower portions of the trenches.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention.

Claims

1. A memory comprising a semiconductor substrate (26) having a major surface and at least one trench (24) with a longitudinal axis, further comprising at least one storage capacitor (16) disposed on a given major sidewall of the trench and a field effect transistor (10) for loading the storage capacitor (16) and disposed on said given mayor sidewall of the trench (24) with a gate electrode (14) and a channel (30) located at the given mayor sidewall of the trench and extending between two electrodes (20, 22) serving as drain and source, wherein the gate electrode (14) material extends into the trench (24),
wherein the storage capacitor (16) comprises a first plate represented by a storage node (20), diffused in the given mayor sidewall of the trench (24) and electrically connected with one (20) of both electrodes which serve as drain and source of the field effect transistor (10), a second plate (18) made of conductive material deposited inside the trench and an insulating layer (52) to separate the first and second plates electrically,
characterised in
that an elongated current carrying element (22) is arranged in parallel to the longitudinal axis of the trench (24) and electrically connected with the other electrode (22) of both electrodes which serve as drain and source of the field effect transistor (10), and in
that an electrically conductive line (28) extends from the gate electrode (14) in a direction orthogonal to the longitudinal axis of the trench (24).

2. A memory according to claim 1, characterized in that the electrically conductive line (28) and the gate electrode (14) are integrally formed and consist of the same material.

3. A memory according to claim 1 or 2, characterized by an insulating layer (36) disposed between the conductive material for the second plate (18) of the storage capacitor (16) and the gate electrodes (14).

4. A memory according to anyone of claims 1 to 4, characterized in that the material for the second plate (18) include doped polysilicon.

5. A memory according to anyone of claims 1 to 4, characterized in that the electrically conductive lines (28) include doped polysilicon.

6. A memory according to claim 5, characterized in that the electrically conductive lines (28) contain silicide.

7. A memory according to anyone of claims 1 to 6,
characterized in
that it contains an array of memory cells, each consisting of the storage capacitors (16) and associated field effect transistors (10), located in a plurality of trenches (26) and connected with associated electrically conductive lines (28) and elongated current carrying elements (22), wherein the electrically conductive lines (28) and the elongated current carrying elements (22) are connected to the outputs of bit line decoders and word line decoders.

8. A memory according to anyone of claims 1 to 7, characterized in that both of the sidewalls of a trench provide storage capacitors (16) with associated field effect transistors (10).

Patentansprüche

1. Speicher mit einem Halbleitersubstrat (26), das eine Hauptoberfläche und wenigstens einen Graben (24) mit einer Längsachse aufweist, und des weiteren mit wenigstens einem auf einer gegebenen Hauptseitenwand des Grabens angeordneten Speicherkondensator (16) sowie einem auf der gegebenen Hauptseitenwand des Grabens (24) angeordneten Feldeffekttransistor (10) zum Laden des Speicherkondensators (16) mit einer Gate-Elektrode (14) und einem Kanal (30), der sich an der gegebenen Hauptseitenwand des Grabens befindet und sich zwischen zwei Elektroden (20, 22) erstreckt, die als Drain und Source dienen, wobei sich das Material der Gate-Elektrode (14) in den Graben (24) hinein erstreckt,
wobei der Speicherkondensator (16) eine erste, durch einen Speicherknoten (20) dargestellte Plattenelektrode, die in die gegebene Hauptseitenwand des Grabens (24) eindiffundiert und mit einer (20) der beiden Elektroden, die als Drain und Source des Feldeffekttransistors (10) dienen, elektrisch verbunden ist, eine zweite, aus leitfähigem Material gefertigte Plattenelektrode (18), die im Inneren des Grabens aufgebracht

ist, sowie eine isolierende Schicht (52) beinhaltet, um die erste und die zweite Plattenelektrode elektrisch zu trennen,
dadurch gekennzeichnet,
daß ein langgestrecktes, stromführendes Element (22) parallel zu der Längsachse des Grabens (24) angeordnet und mit der anderen Elektrode (22) der beiden Elektroden, die als Drain und Source des Feldeffekttransistors (10) dienen, elektrisch verbunden ist, und
daß sich eine elektrische Leiterbahn (28) von der Gate-Elektrode (14) in eine Richtung orthogonal zu der Längsachse des Grabens (24) erstreckt.

2. Speicher nach Anspruch 1, dadurch gekennzeichnet, daß die elektrische Leiterbahn (28) und die Gate-Elektrode (14) integral gebildet sind und aus dem gleichen Material bestehen.

3. Speicher nach Anspruch 1 oder 2, gekennzeichnet durch eine isolierende Schicht (36), die zwischen dem leitfähigen Material für die zweite Plattenelektrode (18) des Speicherkondensators (16) und den Gate-Elektroden (14) angeordnet ist.

4. Speicher nach einem der Ansprüche 1 bis 4, dadurch gekennzeichnet, daß das Material für die zweite Plattenelektrode (18) dotiertes Polysilicium beinhaltet.

5. Speicher nach einem der Ansprüche 1 bis 4, dadurch gekennzeichnet, daß die elektrischen Leiterbahnen (28) dotiertes Polysilicium beinhalten.

6. Speicher nach Anspruch 5, dadurch gekennzeichnet, daß die elektrischen Leiterbahnen (28) Silicid enthalten.

7. Speicher nach einem der Ansprüche 1 bis 6,
dadurch gekennzeichnet,
daß er eine Matrix aus Speicherzellen enthält, die jeweils aus den Speicherkondensatoren (16) und den zugehörigen Feldeffekttransistoren (10) bestehen, die in einer Mehrzahl von Gräben (24) angeordnet und mit zugehörigen elektrischen Leiterbahnen (28) und langgestreckten stromführenden Elementen (22) verbunden sind, wobei die elektrischen Leiterbahnen (28) und die langgestreckten stromführenden Elemente (22) mit den Ausgängen von Bitleitungsdecodern und Wortleitungsdecodern verbunden sind.

8. Speicher nach einem der Ansprüche 1 bis 7, dadurch gekennzeichnet, daß an beiden Seitenwänden eines Grabens Speicherkondensatoren (16) mit zugehörigen Feldeffekttransistoren (10) vorgesehen sind.

Revendications

1. Mémoire comprenant un substrat semiconducteur (26) ayant une surface principale et au moins une tranchée (24) ayant un axe longitudinal et comprenant, de plus, au moins un condensateur de mémorisation (16) disposé sur une paroi principale donnée de ladite tranchée et un transistor à effet de champ (10) pour charger le condensateur de mémorisation (16), disposé sur ladite paroi principale de la tranchée (24) et comprenant une électrode de grille (14) et un canal (30) situés sur ladite paroi principale et s'étendant entre deux électrodes (20, 22) servant de drain et de source, où le corps de l'électrode de porte (14) s'étend dans la tranchée,
dans laquelle le condensateur de mémorisation (16) comprend une première plaque représentée par un point mémoire (20), diffusée dans ladite paroi principale de la tranchée (24) et connectée électriquement à l'une (20) des deux électrodes qui forment le drain et la source du transistor à effet de champ (10), une deuxième plaque (18) à base d'un corps conducteur déposée dans la tranchée, et une couche isolante (52) pour séparer électriquement la première et la deuxième plaque,
caractérisée en ce que :
un élément porteur de courant allongé (22) est disposé parallèlement à l'axe longitudinal de la tranchée (24) et connecté électriquement à l'autre (22) des deux électrodes qui forment le drain et la source du transistor à effet de champ (10), et
une ligne conductrice d'électricité (28) s'étend depuis l'électrode de grille (14) perpendiculairement à l'axe longitudinal de la tranchée (24).

2. Mémoire selon la revendication 1, dans laquelle la ligne conductrice d'électricité (28) et l'électrode de por-

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te (14) sont formées intégralement à base du même matériau.

3. Mémoire selon la revendication 1 ou 2, dans laquelle une couche isolante (36) est disposée entre le corps conducteur de la deuxième plaque (18) du condensateur de mémorisation (16) et les électrodes de grille.

4. Mémoire selon l'une quelconque des revendications 1 à 4, dans laquelle le corps pour former la deuxième plaque (18) contient du polysilicium dopé.

5. Mémoire selon l'une quelconque des revendications 1 à 4, dans laquelle les lignes conductrices d'électricité (28) contiennent du polysilicium dopé.

6. Mémoire selon la revendication 5, dans laquelle les lignes conductrices d'électricité (28) contiennent du siliciure.

7. Mémoire selon l'une quelconque des revendications 1 à 6,
caractérisée en ce que :
elle contient une matrice de cellules de mémoire consistant chacune en des condensateurs de mémorisation (16) et en leurs transistors à effet de champ associés (10), situés dans une pluralité de tranchées (26) et connectés à des lignes conductrices d'électricité (28) et éléments porteurs de courant allongés (22) associés, les dits lignes conductrices d'électricité (28) et éléments porteurs de courant allongés (22) étant reliés aux sorties de décodeurs de lignes de bit et de décodeurs de lignes de mots.

8. Mémoire selon l'une quelconque des revendications 1 à 7, dans laquelle les deux parois d'une tranchée forment des condensateurs de mémorisation (16) et les transistors à effet de champ associés.

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