WHAT IS CLAIMED IS:

1. A non-volatile memory device comprising:

a first semiconductor layer including a peripheral region, the peripheral region including one or more peripheral transistors on a lower substrate; and

a second semiconductor layer on the peripheral region, the second semiconductor layer including an upper substrate, the second semiconductor layer further including a memory cell array on the upper substrate, the upper substrate including

a first upper substrate on the first semiconductor layer,

a first layer on the first upper substrate, and

a second upper substrate on the first layer;

wherein the first layer includes a dielectric layer, and the non-volatile memory device further includes a capacitor, the capacitor including the first upper substrate, the second upper substrate, and the first layer.

2. The non-volatile memory device of claim 1, further comprising:

a contact, the contact electrically connected to the first upper substrate, the contact configured to transfer a voltage to the first upper substrate based on an operation signal being applied to the memory cell array.

3. The non-volatile memory device of claim 2, wherein the contact is electrically connected to a bottom surface of the first upper substrate.

4. The non-volatile memory device of any one of claims 1 to 3, wherein

the first upper substrate includes one or more insulation layers, and

the first upper substrate includes a first section and a second section, the first section and the second section separated by the one or more insulation layers.

5. The non-volatile memory device of claim 4, further comprising:

a first contact, the first contact electrically connected to the first section, the first contact configured to transfer a first voltage to the first section based on a first operation signal associated with a first operation of the memory cell array being applied to the memory cell array; and

a second contact, the second contact electrically connected to the second section, the second contact configured to transfer a second voltage to the second section based on a second operation signal associated with a second operation of the memory cell array being applied to the memory cell array, the second voltage having a different magnitude than a magnitude of the first voltage.

6. The non-volatile memory device of any one of claims 1 to 5, wherein

the first upper substrate and the second upper substrate are doped with an impurity of a first conductivity type, and

the first layer is doped with an impurity of a second conductivity type, and

the second conductivity type is opposite to the first conductivity type.

7. The non-volatile memory device of any one of claims 1 to 6, wherein the non-volatile memory device is configured to apply a ground voltage to the first upper substrate based on an operation signal associated with an operation of the memory cell array being applied to the second upper substrate.

8. The non-volatile memory device of claim 7, wherein the non-volatile memory device is configured to apply a voltage to the first layer based on the operation signal associated with the operation of the memory cell array being applied to the second upper substrate, the voltage having a magnitude greater than or equal to a magnitude of the ground voltage.

9. The non-volatile memory device of any one of claims 1 to 8, wherein

the second upper substrate is doped with an impurity of a first conductivity type, and

the second upper substrate includes a first well region and a second well region, the first well region occupying a portion of the second upper substrate, the first well region doped with an impurity of a second conductivity type, the second conductivity type opposite to the first conductivity type, the second well region occupying a portion of the first well region, the second well region doped with the first conductivity type.

10. The non-volatile memory device of any one of claims 1 to 9, wherein the memory cell array includes

a plurality of gate conductive layers on the second upper substrate, and

a plurality of channel layers penetrating the plurality of gate conductive layers, the plurality of channel layers extending in a direction perpendicular to a top surface of the second upper substrate.

11. A non-volatile memory device comprising:

a lower substrate;

a peripheral region on the lower substrate, the peripheral region including a peripheral circuit on the lower substrate; and

a memory cell region on the peripheral region, the memory cell region including an upper substrate, the memory cell region further including a memory cell array on the upper substrate, the upper substrate including

a first upper substrate,

a second upper substrate above the first upper substrate,

a first layer between the first upper substrate and the second upper substrate ,

a second layer on the second upper substrate, and

a third upper substrate on the second layer;

wherein the first layer includes a dielectric layer, and the non-volatile memory device further includes a capacitor, the capacitor including the first upper substrate, the second upper substrate, and the first layer.

12. The non-volatile memory device of claim 11, further comprising:

a contact, the contact penetrating through the second layer and the third upper substrate and extending in a direction perpendicular to a top surface of the second upper substrate,

wherein the non-volatile memory device is configured to apply a ground voltage to the second upper substrate through the contact based on an operation signal being applied to the memory cell array.

13. The non-volatile memory device of claim 11 or claim 12, wherein

the first upper substrate, the second upper substrate, and the third upper substrate include poly-silicon doped with an impurity of a first conductivity type, and

the second layer includes poly-silicon doped with an impurity of a second conductivity type, the second conductivity type opposite to the first conductivity type.

14. The non-volatile memory device of any one of claims 11 to 13, wherein the non-volatile memory device is configured to apply a power supply voltage associated with the peripheral circuit to the first upper substrate based on an operation signal associated with an operation of the memory cell array being applied to the memory cell region.

15. A method of fabricating a non-volatile memory device, the method comprising:

forming one or more peripheral transistors on a portion of a lower substrate, the one or more peripheral transistors connected to a plurality of peripheral circuit wires, a lower insulation layer covering the one or more peripheral transistors and the peripheral circuit wires;

forming a first upper substrate on the lower insulation layer;

forming a first layer on the first upper substrate;

forming a second upper substrate on the first layer; and

forming a memory cell region on the second upper substrate, the memory cell region including a memory cell array;

wherein the first layer includes a dielectric layer, and the non-volatile memory device further includes a capacitor, the capacitor including the first upper substrate, the second upper substrate, and the first layer.

16. The method of claim 15, wherein

the forming of the first upper substrate includes doping the first upper substrate with an impurity having a first conductivity type, and

the forming of the first layer includes doping the first layer with an impurity having a second conductivity type, the second conductivity type opposite to the first conductivity type.

17. The method of claim 15 or claim 16, wherein the forming of the memory cell region includes forming a plurality of gate conductive layers on the second upper substrate and a plurality of channel layers penetrating the plurality of gate conductive layers, the plurality of channel layers extending in a direction perpendicular to a top surface of the second upper substrate.