ABSTRACT

A semiconductor device includes a lower structure including a peripheral circuit, a lower insulating structure covering the peripheral circuit, and a pattern structure on the lower insulating structure; a stack structure including interlayer insulating layers and horizontal layers alternately stacked on the lower structure, wherein the horizontal layers include gate horizontal layers in a gate region of the stack structure and first insulating horizontal layers in a first insulating region of the stack structure; a memory vertical structure including a portion penetrating the gate horizontal layers; dummy vertical structures including a portion penetrating the gate horizontal layers; a first peripheral contact plug including a portion penetrating the first insulating region; and gate contact plugs on gate pads of the gate horizontal layers, wherein the memory vertical structure and the dummy vertical structure are contacting the pattern structure, and wherein at least one of the dummy vertical structures extend further into the pattern structure than the memory vertical structure in a downward direction.

FIG. 2A