

POLYMORPHIC HETEROGENEOUS MULTI-CORE ARCHITECTURE

Abstract

Methods and architecture for dynamic polymorphic heterogeneous multi-core processor operation are provided. The method for dynamic heterogeneous polymorphic processing includes the steps of receiving a processing task comprising a plurality of serial threads. The method is performed in a processor including a plurality of processing cores, each of the plurality of processing cores being assigned to one of a plurality of core clusters and each of the plurality of core clusters capable of dynamically forming a coalition comprising two or more of its processing cores. The method further includes determining whether each of the plurality of serial threads requires more than one processing core, and sending a go-into-coalition-mode-now instruction to ones of the plurality of core clusters for handling ones of the plurality of serial threads that require more than one processing core.

Fig. No. 3