MULTI-SCREEN GENERATION CIRCUIT

This invention relates to digital video signal processing circuits for use in, for example, color television sets (CTV) and video tape recorders (VTR), and is concerned particularly with multi-screen generation circuits.

New CTV and VTR products, employing new technology for displaying multi-screens on a single monitor, are presently being introduced - especially in Europe, America and Japan. Different multi-screen systems can provide different types of screen - for example, 4-screen, 9-screen, 12-screen, or 16-screen, on one monitor; a multi-screen CTV may have one or more of such types, depending usually upon the manufacturer.

However, in known multi-screen CTV systems, as screen type(s) are fixed to only one or two of such 4-screen, 9-screen, 12-screen or 16-screen modes, the choice of multi-screens has been very limited for a given size of monitor.

Preferred embodiments of the present invention aim to provide a circuit capable of freely displaying on a main screen at a user's choice between 4 and 16 different picture sources in multi-screen mode, and preferably 4 sub-screens, 9-sub-screens, 13 sub-screens and 16 sub-screens, according to the size of the main screen.

Another aim is to provide a circuit capable of giving a free choice in the number of channels in a multi-channel mode, regardless of the number of available

broadcasting channels, which may differ from one region to another.

According to the present invention, there is provided a multi-screen generation circuit for generating one or more sub-screens, in which each sub-screen is a substantially uniformly compressed version of a picture corresponding to one of a plurality of user selectable channels, the circuit comprising input means arranged to receive video signals representing a plurality of video channels, an analog-to-digital converter for digitizing the video signals, processing means arranged to generate from said video signals video data representing a plurality of discrete video pictures, each corresponding to a different video channel, in accordance with n-screen mode selection data (where n is 1 or more) and output means arranged to generate a composite video signal containing said video data, such that the plurality of sub-screens may be displayed simultaneously upon a common screen, each in a respective portion of the screen, the selection data being used to select a desired one of a plurality of selectable n-screen modes, at least one of the screen modes being capable of simultaneously displaying sub-screens in two different sizes upon the common screen.

Preferably, the sampling rate of the analog-to-digital converter is varied in accordance with the screen mode selected.

Preferably, the circuit includes dual port memories, a synchronising signal generator, and a microcomputer and further comprises:

a command decoder that receives a vertical synchronising signal from the synchronising signal

generator and the n-screen mode selection data together with control signals from said microcomputer, and after decoding them, generates screen mode information signals;

an address signal generator that comprises row/column writing and row/column reading address signal generation circuits which generate writing address signals which are applied into said dual-port memories for reading/writing operations, in accordance with the n-screen mode selection data;

a writing reference signal generation circuit (WRS) that generates signals derived from the vertical and horizontal synchronising signals generated by the said synchronising signal generator, and read reference signal corresponding with writing after receiving display mode data from said command decoder;

a writing display controller that receives a vertical sampled signal from said writing reference signal generation circuit and display mode data from said command decoder, then designates row/column writing address signal generators of said address signal generator to be written with display mode data and controls the address generation of data to be written;

an analog-to-digital clock generator that receives horizontal synchronising signals generated from video signals of said synchronising signal generator together with reference frequency signals from a basic clock terminal and display mode data from said command decoder, then demultiplies respectively said reference frequency signal in accordance with the n-screen mode selection data and generates the clock signals for the analog-to-digital converter;

a first multiplexer that multiplexes address signals generated from said address signal generator according to control and then applies said signals as address data to said dual port memories;

a serial-parallel converter that produces a digitized signal of said video signals by control of said dual port memories, and serial luminance data and colour data after converting to parallel luminance data to a first and a second luminance and a colour terminal under the control of said serial-parallel converter;

a write timing generator that receives sampling clock signals for digitizing video signals according to display mode selection from said analog-to-digital clock generator, and dual-port memory write-enable signals and write-begin signals from said writing reference signal generator, and then generates control signals for first and second luminance and colour signal selection for said serial-parallel converter, together with address switching and data transmission signals for the first multiplexer, and also generates a data transmission signal, DT, which runs a transmission control to R/CAS (Row/Column Address Strobe), and WE (Write Enable) terminals of the dual-port memories and the register of serial port;

a read timing generation circuit that receives horizontal synchronising signals from said synchronising signal generator and signals from said reference frequency clock section, generates burst gate pulses and clock signals for a digital-to-analog converter and then generates serial clock signals and control timing signals according to data read;

a latch section that outputs multi-screen data from an address designated by generation of data from said

row/column reading address generation circuits for the address signal generator according to serial clock column signals from the read timing generation circuit, and then latches according to the first and second luminance and colour signals based on clock signals; and

a data multiplexer that mixes data from said latch section according to the control clock of said read timing generation circuit and then outputs to the digital-to-analog converter.

In another aspect, the invention provides video processing and/or display apparatus provided with a multi-screen generation circuit according to the first aspect of the invention.

Such apparatus may comprise a color monitor and/or video recorder. The recorder may be a tape recorder.

For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

Figure 1 is a block diagram of one example of a multi-screen generation system embodying the present invention;

Figure 2 is a block circuit diagram of one example of a multi-screen generation circuit of the system Figure 1;

Figure 3 is a more detailed circuit diagram of an example of an analog-to-digital clock generator 188 of Figure 2;

Figure 4 is a timing diagram illustrating an example of operation of the clock generator of Figure 3;

Figure 5 is a counting state diagram of the clock generator of Figure 3;

Figure 6 is a more detailed circuit diagram of an example of a writing display controller 140 of Figure 2;

Figure 7 is a diagram illustrating examples of waveforms generated in the writing display controller 140 of Figure 6; and

Figure 8 is a diagram illustrating examples of the actual composition of multi-screens in use of the system of Figure 1.

In the system of Figure 1, video signals are divided into R-Y, B-Y and Y signals in a demodulator(DMR), and an fsc signal is trapped in a color difference signal trapper (CDT). A controller receives control signals and clock signals which relate to display mode and are generated from a microcomputer (MICOM), and generates sampling clock signals (ADCLK, DACLK) which are output respectively to an analog-to-digital converter (A/D) and a plurality of digital-to-analog converters (DA1 to DA3). Digitized data from the analog-to-digital converter (A/D) is processed through the controller and stored in a plurality of dual-port memories DM1 through DM4 according to the display mode control signals. Then, video signals for multi-screen display, stored in said dual-port memories DM1 through DM4, are read out, analogized in the digital-to-analog converters DA1 through DA3, synchronized in burst gate pulse by the controller and encoded in a encoder, to provide

synthesized video signals in multi-screen configuration.

Referring now to Figure 2, the controller of Figure 1 comprises a multi-screen generation circuit which comprises, in more detail, a command decoder 10 that receives a vertically synchronous signal from a synchronous signal generator (SYN) 1 and multi-screen mode command data together with control signals through lines 11-14, generated from the MICOM of Figure 1, and after decoding them, generates display mode selection data signals 4p, 9p, 13p, 16p.

An address signal generator 20 comprises row/column writing and row/column reading address signal generation circuits (ASG) 21-24 which divide image data for displaying a number of multi-screen modes into each domain of screen and generates writing address signals which are applied into the dual-port memories (DM1-DM4) of Figure 1 for reading/writing operations. A writing reference signal generation circuit (WRS) 30 generates a vertically/horizontally synchronous signal, which is generated in said synchronous signal generator 1, and reading reference signal corresponding with writing after receiving display mode data from said command decoder 10. A writing display controller 140 receives a vertically sampled signal from the writing reference signal generation circuit 30 and displays mode data from the command decoder 10, then designates row/column writing address signal generators 21, 22 of the address signal generator 20 to be written with display mode data and controls the address generation of data to be written.

An analog-to-digital clock generator(A/D CLK) 188 receives horizontally synchronous signals generated from video signals by said synchronous signal generator 1

together with signals of 4x3.58 MHz from a basic clock terminal (4fsc) and display mode data from said command decoder 10, then demultiplies respectively the 4x3.58 MHz frequency according to the selection of 1, 4, 9, 13 or 16 screens (1p, 4p, 9p, 13p or 16p selection) and generates the clock signal ADCLK for the analog-to-digital convertor A/D of Figure 1.

A first multiplexer 60 multiplexes address signals generated from said address signal generator 20 in accordance with control data decoded by the decoder 10, and then applies the signals as address data to the dual port memories DM1 through DM4 of Figure 1. A serial-parallel converter (SPC) 50 produces a digitized signal of the video signals by control of the dual port memories DM1 through DM4, and converts serial luminance data and color data to parallel data, which is provided to first and a second luminance terminals (YA, YB) and a color terminal (YC) under the control of the serial-parallel converter 50.

A write timing generator 70 receives sampling clock signals for digitizing video signals according to display mode selection from the analog-to-digital clock generator 188, and dual-port memory write-enable signals and write-begin signals from the writing reference signal generator 30, and then generates control signals for first and second luminance and color signal selection for the serial-parallel converter 50, together with address switching and data transmission signals for the first multiplexer 60, and also generates a DT signal which runs a transmission control to RAS (Row Address Strobe), CAS (Column Address Strobe), and WE(Write Enable) terminals of the dual-port memories and the register of the serial port. A read timing generation circuit 80 receives

horizontally synchronous signals from the synchronous signal generator 1 and signals from the reference clock section (4fsc), generates burst gate pulses for the system of Figure 1 together with clock signals for the digital-to-analog converter D/A and then generates serial clock signals and control timing signals according to data read.

A latch section 90 outputs multi-screen data from addresses designated by generation of address data by the row/column reading address generation circuits 23, 24 of the address signal generator 20, according to serial clock column signals (SC) from the read timing generation circuit 80, and then latches the signals on the first and second luminance YA, YB and color YC terminals in accordance with the clock signals. A data multiplexer 100 mixes data from the latch section 90 according to the control clock of the read timing generation circuit 80 and then outputs to the digital-to-analog converter of Figure 1.

As shown in more detail in Figure 3, the digital clock generator 188 of Figure 2 comprises a reset terminal (RESET) 41, a reference clock (4fsc) terminal 42, a horizontally synchronous signal terminal 43, and first through third display mode selection (9p, 4p, 16p) terminals 44, 45, 46, which are connected to the command decoder 10. When a signal received on the reset terminal 41 is passed through invertors (N11, N12) and, together with the output from the horizontally synchronous signal terminal 43 is entered to an AND gate AN11, and the output of the AND gate AN11 is entered into the $\overline{CLR}$ terminals of two D-type flip/flops DF11 and DF12, then the entire system is initialized.

The first display selection terminal 44 is connected to an input port of a NAND gate NA11 and through an invertor N13 to an input port of a NAND gate NA12. Each output port of the NAND gates NA11 and NA12 is connected to an input port of a NAND gate NA13, the output port of which is connected to the data port D of the D-type flip-flop DF11. The output port Q of the flip-flop DF11 is connected to an input port of a NAND gate NA15 and to an input port of an exclusive-OR gate EX011. The output port $\bar{Q}$ of D-flip-flop DF11 is connected to the NAND gates NA11 and NA12. The output port of the exclusive-OR gate EX011 is connected through an invertor N15 to the data port D of the D-type flip-flop DF12, whose output port Q is connected to an input port of the exclusive-OR gate EX011 and to an input port of a NAND gate NA14. The output port $\bar{Q}$ of the flip-flop DA12 is connected to an input port of the NAND gate NA11.

The first and second display mode selection terminals 44, 45 are connected to input ports of an OR gate OR11, whose output port together with the third display mode selection terminal 46 are connected to input ports of a NOR gate NOR12. The output ports of the OR gate OR11 and the NOR gate NOR12 are connected to input ports of NAND gates NA15, NA16 respectively. The outputs of the NAND gates NA14 to NA16 generate, through a NAND gate NA17 to a clock output terminal 47, a signal which controls conversion of analog video signals to digital signals in accordance with a multi-screen mode selection.

In the operation timing diagram example of Figure 4, waveform (4a) is a reference clock signal (4fsc) input on terminal 42; and waveform (4b) is a signal input on reset terminal 41 or horizontally synchronous signal

terminal 43. Waveform (4c) is an output signal of the NAND gate NA17 if 9-screen mode is being written when the logic levels of the first through third display selection terminals 44, 45, 46 are HIGH, LOW, LOW respectively. Wwaveform (4d) is an output signal of the NAND gate NA17 when 4-screen mode or 12th screen of 12-screen display is written when the logic levels of the first through third display selection terminals 44, 45, 46 are LOW, HIGH, LOW respectively. Waveform (4e) is an output signal of the NAND gate NA17 if first and second screens of a 13-screen display are written when the logic levels of the first through third display selection terminals 44, 45, 46 are LOW, LOW, HIGH respectively.

Figure 5 is a diagram illustrating shifts of counting state generated in the output ports Q of the D-flip-flops DF11, DF12 of Figure 3.

In the more detailed circuit diagram of Figure 6, showing the writing display controller 140 of Figure 2, the input ports of AND gates AN1 through AN4 are connected to first through fourth terminals 141 through 144 which receive display mode selection signals (4p, 9p, 13p, 16p) from the command decoder 10 of Figure 2. The output ports of the AND gates AN1 through AN4 are connected through a NOR gate NOR1 to a data port of a D-type flip-flop DF1 and an enable port EN of a counter CNT1. An output port Q of the D-type flip-flop DF1 and an output of an invertor N140 are connected to an OR gate OR1, the output of which is connected to an input port of an AND gate AN5, which is connected on its other input ports to a reset terminal 145 and a multi-screen conversion signal terminal 146. The output port of the AND gate AN5 is connected to a reset port R of the counter CNT1.

A reset port 147 and a vertically synchronous signal terminal 148 are connected rrespectively to reset ports R and clock ports CK of a two-stage counter CNT 2, CNT3. Output ports QC, QD or QA through QC of the counter CNT2, CNT3 are connected to the input port of a multiplexer MUX1. An output Q of the multiplexer MUX1 is connected to the clock port CK of the counter CNT1 and through an invertor N140 to the clock port CK of the D-type flip-flop DF1 and input port of the OR gate OR1. Outputs QA through QD of the counter CNT1 generate writing control signals through writing control ports WC0 - WC3; and outputs of the writing control ports WC0 through WC3 are configured to be entered into the AND gates AN1 through AN4.

In the timing diagram of Figure 7, illustrating an example of operation of the writing display controller of Figure 6, (7a) is an output signal of the output port Q of the multiplexer MUX1, and (7b) is a "HIGH" waveform of the third display mode selection (13p) terminal 143, whilst the first and second display mode selection (4p, 9p) terminals 141, 142 and the fourth display mode selection (16p) terminal 144 are "LOW". (7c) is an input signal of the reset terminal 145 and the multi-screen conversion signal terminal 146; (7d) is an output of the output ports QA through QD of the counter CNT1 and also a control data waveform of the writing control ports WC0 through WC3; (7e) is an enable signal of the output counter CNT1 from the NOR gate NOR 1; and (7f) is an output signal of the output port Q of the D-type flip-flop PF1.

In the illustrative diagram of Figure 8, showing an actual multi-screen configuration, (8A) is an example of a 4-screen display, (8B) is an example of a 9-screen

display, (8C) is an example of a 13-screen display, and (8D) is an example of a 16-screen display.

Now, an example of the operation of the system described above with reference to Figures 1 through 8 will be given.

When a 1-screen mode is set with a vertical reference of 240 lines and a horizontal rerference of 372 dots to write a field display to the dual port memory (DM1-MD4) of Figure 1, three out of the four dual-port memories DM1 through DM4 are used as Y (YA, YB) and two of the dual port memories DM1 through DM4 are assigned to C, (B-Y), (R-Y) as the band width ratio of the luminance signal Y and color signal C is about 4:1.

The dual port memories DM1 through DM4 can be configured into areas as in Table 1 below.

SCREENS	VER SYNC(line)	HOR SYNC(number)
4	120	186
9	80	124
13	60 for 1-12th screen	93
	120 for 13th screen	186
16	60	93

Table 1

A vertical and horizontal synchronising signal generated by the synchronous signal generator 1 from a video input signal and the 4x3.58 MHz reference frequency signal from the reference clock terminal (4fsc) are entered into the analog-to-digital clock generator 188 and writing reference signal generator 30, and data to select the same displays as (8A) through (8D) of Figure 8 is entered through the MICOM into the command decoder 10.

In this case, display mode selection data 4p, 9p, 13p, 16p from the command decoder 10, generated by display mode selection command, is entered into the analog-to-digital clock generator 188 and the writing reference signal generation circuit 30. At the same time, a clock signal is generated as a result of conversion of a video signal into a digital signal in the analog-to-digital clock generator 40.

Now, referring particularly to Figure 2, a signal (4a), which is the same as that at the 4fsc port of Figure 2, is applied as a clock signal to the D-type flip-flops DF11-DF12 through the reference clock port 42 of Figure 3 and the D-type flip-flops DF11-DF12 are reset according to the input signal (4b) of the reset terminal 41 and horizontally synchronous signal terminals 41, 43 and therefore initialized. At this time an analog-to-digital (hereinafter referred to as "A/D") clock signal is generated, based on a selected mode of multi-screen according to input signals of the first, second, third screen selection (9p, 4p, 16p) terminals 44, 45, 46.

For example, if a reference clock for a single screen is taken as the signal 4fsc, in the 4-screen mode 8A of Figure 8 the clock is divided by half when a horizontally synchronous signal is taken as a reference signal, so that when the clock is divided a signal such

as 4d of Figure 4 is generated.

In the case of the 9-screen mode 8B of Figure 8, a horizontally synchronous signal is scaled down to 1/3, so that a signal such as 4C of Figure 4 is generated - thus, the 4fsc signal is divided by 3.

In the case of the 16-screen mode of Figure 8, a horizontally synchronous signal is divided into 4, so that a signal such as 4e of Figure 4 is generated - thus, the 4fsc signal is divided by 4.

In the case of the 13-screen mode 8D of Figure 8, divisions can be made differently on the corresponding horizontal lines in such a way that 16-screen and 4-screen can be generated preferentially.

Clocks to generate 4p, 9p-13p, 16p are converted according to the input logic of the first through third display mode selection terminals 44, 45, 46.

That is, when writing 9p, the output of the NAND gate NA17 is a third division of 4fsc, so that the output is generated in the same way as when the first display mode selection terminal 44 is "HIGH" and second, third display mode selection terminals 45, 46 are "LOW". When writing 4p or the 13th screen of 13p, a signal such as 4d is generated if the second display mode selection terminal 45 is "HIGH" and the first and third display selection terminals 44, 46 are "LOW". When writing 16p or the first through 12th screen of 13p, a signal such as 4e is generated if the third display mode selection terminal 46 is "HIGH" and the first and second display mode selection terminals 44, 45 are "LOW".

Accordingly, based on an input of the horizontally synchronous signal terminal 43 connected to the AND gate AN11 in Figure 3, the 4fsc signal at the reference clock terminal 42 is divided as specified by the signal at the first through third display mode selection signal terminals 44-46.

At this time, if it is assumed that the output port Q of the D-type flip-flop DF1 is Q1 and the output port Q of the D-type flip-flop DF2 is Q2, Q1 is divided by 2 and Q2 is divided by 4 so that, when terminal 45 is "HIGH", a clock is generated for 4-screen mode and when the terminal 46 is "HIGH", a corresponding clock for 16-screen mode is output through the NAND gates NA14 through NA1. That is, when the outputs of Q1 and Q2 are shifted 00 -> 11 -> 10 -> 01 as in Figure 5, three divisions occur because the output 10 returns to 00 if the first display mode selection signal terminal 44 is "HIGH", but the output progresses to 01 if the first display mode selection signal terminal is "LOW", corresponding to a mode other than the 9-screen mode.

Accordingly, the output of the counter of Figure 3 changes transiently according to the state of the first display mode selection signal terminal 44 and if this is "HIGH", the reference frequency signal 4fsc is divided by three, so that an A/D clock corresponding to 9-screen mode is supplied.

As mentioned above, also in the case of 13- and 16-screen modes, the 4fsc signal is divided and supplied as the A/D clock (ADCLK) signal of the analog-to-digital converter of Figure 1, and is also applied to the write timing generator 70. In addition, by means of the writing reference signal generation circuit 30 a writing-

begin control signal and a memory writing-enable signal are applied to the write timing generator 70 according to the display mode selection data and vertically/horizontally synchronous signal from the synchronous signal generator 1, and at the same time, fed into the writing display controller 140 as a vertically sampled signal. At this time, the R-Y, B-Y, Y signals, which are output from the demodulator of Figure 1, are sequentially selected in said write timing generator 70 after sampling in the analog-to-digital converter according to the A/D clock, converted into a digital signal, and then entered into the serial-parallel converter 50.

The signal which is entered into the serial-parallel converter 50 is divided according to first and second luminance YA, YB and color YC signals based on a control clock of the write timing generator 70, and then is sent to the dual-port memories DM1, DM2. Meanwhile, the writing display controller 140 generates the window control signals WC0 through WC3 of Figure 6 in order to specify row-column addresses to write together with display mode selection data.

Now, considering the writing display controller 140 of Figure 6 in more detail, signals are entered into the first through fourth display mode selection signal (4p, 9p, 13p, 16p) terminals 141 through 144 and outputs of the output ports QA through QD and ripple carry port of the counter CNT1, are logicized, and corresponding data is generated through the NOR gate NOR1. If the output of the NOR gate NOR1 is generated as the waveform (7e) of Figure 7, an output of the output port Q of the D-type flip-flop DF1 is generated as the waveform (7f) of Figure 7. This output is, of course, all reset in an

initial stage by the reset terminals 145, 147. However, once the reset is completed and a conversion signal C is entered into the multi-screen conversion pulse terminal 146, the counter CNT 1 is shifted into a reset state in order to reset to jump to other display mode.

Meanwhile, a synchronous signal from the vertically synchronous signal terminal 148 is received as a clock signal and counted in the two-stage counter CNT2, CNT3 and entered into the multiplexer MUX1. Then the multiplexer MUX1 selects the corresponding output value of the counter CNT1, CNT2 under the control of the strobe selector terminal 150 by the command decoding signal which is received from the MICOM, and the output of output port Q of the multiplexer MUX1 is counted in the counter CNT1. Then, window control signals WC3 through WC0 are generated and sent to output ports QA through QB as (7d), and entered into the row-column writing address generation circuits 21, 22, so that a display mode selection can be specified.

Once a corresponding value has been counted from the said first through fourth display mode selection signal terminals, then the above operation is reset by the AND gates AN1 through AN4, NOR gate NOR1 and D-type flip-flop DF1.

Terminal 150 is put under the control of the MICOM for the purpose of strobe time variation at CNT2, CNT3 and MUX1, and then port 4 of MUX1 selects input a value of between 1 through 6 according to up or down of output time variation an initial stage.

Figure 7 illustrates the case in which 143 = "HIGH", that is, 12p (i.e. 13th screen of 13p); here, it

is obvious that CNT1 is disabled when WC0 through WC3 are 1.

The output Q of D-type flip-flop DF 1 resets CNT1 with one delayed clock of the output of the NOR gate NOR1, thereby generating a writing display control signal continuously, so that 13 screens can appear all at once in one main screen. The method described above works in the same manner for 4p, 9p and 16p.

In order to cause a state where writing is performed only once and just the last screen is changed (continuously stopped at 12 after writing 0 through 12), a setting operation can be performed by using the set port of DF1 so that a 0 output of NOR 1 is not applied to an input of AN5.

Digital video signals of the serial-parallel converter 50 are generated in the row/column writing address generation circuits 21, 22 of address signal generator 20 in accordance with timing signals $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{DT}$ of the write timing generator 70, and thereby corresponding multi-screen video data is written in appropriate addresses of the dual-port memories DM1 through DM4 selected by the first multiplexer 60 in accordance with the display mode selection window as desired by a user.

When reading, by a read control signal generated in the command decoder 10, by a horizontally/vertically synchronous signal, there is generated in the row/column reading address generation circuits 23, 24 an address of the main dual-port memories DM1 through DM4 and a selection is made in the first multiplexer 60, then a multi-screen data of corresponding address is read and

sent out according to a serial clock of the read timing generation circuit 80. The data output is latched in the latch section 90 and is multiplexed in the data multiplexed in the multiplexer 100 by a control clock generated in the read timing generation circuit 80. The multiplexed data is converted to an analog signal in the digital-to-analog converter D/A according to the clock DA CLK of the read timing generation circuit (80). The converted analog signal is encoded in the encoder according to a burstgate pulse and output as multisynthetic video signal.

The foregoing description of the operation of the illustrated embodiment which is given as only one example of the present invention is centred only around 1, 4, 9, 13, 16 multi-screens. It is apparent to those who are skilled in the art that, without departing from the scope of the present invention, that the number of multi-screens be varied.

As described above, embodiments of the present invention may have such advantages that display mode selection data is received and an A/D clock converts the data accordingly and also controls a window control signal and address values, which are divided across memory areas, are loaded according to a window control signal, so that any display mode among a plurality of display modes (e.g. 1-screen, 4-screen, 9-screen, 13-screen, 16-screen) can be selected and displayed.

* C L M S *

CLAIMS

1. A multi-screen generation circuit for generating one or more sub-screens, in which each sub-screen is a substantially uniformly compressed version of a picture corresponding to one of a plurality of user selectable channels, the circuit comprising input means arranged to receive video signals representing a plurality of video channels, an analog-to-digital converter for digitizing the video signals, processing means arranged to generate from said video signals video data representing a plurality of discrete video pictures, each corresponding to a different video channel, in accordance with n-screen mode selection data (where n is 1 or more) and output means arranged to generate a composite video signal containing said video data, such that the plurality of sub-screens may be displayed simultaneously upon a common screen, each in a respective portion of the screen, the selection data being used to select a desired one of a plurality of selectable n-screen modes, at least one of the screen modes being capable of simultaneously displaying sub-screens in two different sizes upon the common screen.

2. A multi-screen generation circuit according to claim 1, wherein the sampling rate of the analog-to-digital converter is varied in accordance with the screen mode selected.

3. A multi-screen generation circuit according to claim 1 or 2, including dual port memories, a synchronising signal generator, and a microcomputer said circuit comprising:

a command decoder that receives a vertical synchronising signal from the synchronising signal generator and the n-screen mode selection data together with control signals from said microcomputer, and after decoding them, generates screen mode information signals;

an address signal generator that comprises row/column writing and row/column reading address signal generation circuits which generate writing address signals which are applied into said dual-port memories for reading/writing operations, in accordance with the n-screen mode selection data;

a writing reference signal generation circuit (WRS) that generates signals derived from the vertical and horizontal synchronising signals generated by the said synchronising signal generator, and read reference signal corresponding with writing after receiving display mode data from said command decoder;

a writing display controller that receives a vertical sampled signal from said writing reference signal generation circuit and display mode data from said command decoder, then designates row/column writing address signal generators of said address signal generator to be written with display mode data and controls the address generation of data to be written;

an analog-to-digital clock generator that receives horizontal synchronising signals generated from video signals of said synchronising signal generator together with reference frequency signals from a basic clock terminal and display mode data from said command decoder, then demultiplies respectively said reference frequency signal in accordance with the n-screen mode selection data

and generates the clock signals for the analog-to-digital converter;

a first multiplexer that multiplexes address signals generated from said address signal generator according to control and then applies said signals as address data to said dual port memories;

a serial-parallel converter that produces a digitized signal of said video signals by control of said dual port memories, and serial luminance data and colour data after converting to parallel luminance data to a first and a second luminance and a colour terminal under the control of said serial-parallel converter;

a write timing generator that receives sampling clock signals for digitizing video signals according to display mode selection from said analog-to-digital clock generator, and dual-port memory write-enable signals and write-begin signals from said writing reference signal generator, and then generates control signals for first and second luminance and colour signal selection for said serial-parallel converter, together with address switching and data transmission signals for the first multiplexer, and also generates a data transmission signal, DT, which runs a transmission control to R/CAS (Row/Column Address Strobe), and WE (Write Enable) terminals of the dual-port memories and the register of serial port;

a read timing generation circuit that receives horizontal synchronising signals from said synchronising signal generator and signals from said reference frequency clock section, generates burst gate pulses and clock signals for a digital-to-analog converter and then

generates serial clock signals and control timing signals according to data read;

a latch section that outputs multi-screen data from an address designated by generation of data from said row/column reading address generation circuits for the address signal generator according to serial clock column signals from the read timing generation circuit, and then latches according to the first and second luminance and colour signals based on clock signals; and

a data multiplexer that mixes data from said latch section according to the control clock of said read timing generation circuit and then outputs to the digital-to-analog converter.

4. A multi-screen generation circuit, substantially as hereinbefore described with reference to the accompanying drawings.

5. Video processing and/or processing apparatus provided with a multi-screen generation circuit according to any of the preceding claims.

6. Apparatus according to claim 5, comprising a colour monitor.

7. Apparatus according to claim 5 or 6, comprising a video recorder.

8. Apparatus according to claim 7, wherein the recorder is a tape recorder.