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TV LINE AND FIELD DETECTION APPARATUS WITH GOOD NOISE IMMUNITY

The present invention relates to detection of information that may be present in a video signal during vertical blanking intervals. A video signal typically includes vertical display intervals, or fields, having a plurality of horizontal line intervals, e.g. 262.5 lines per field in NTSC video systems. The beginning of each vertical and horizontal interval is identified by respective vertical and horizontal sync pulses that are included in a composite video signal. During a portion of each vertical interval, information in the video signal may not be intended for display. For example, a vertical blanking interval spans approximately the first 20 horizontal line intervals in each field. In addition, several line intervals adjacent to the vertical blanking period, e.g. line 21, may be within an overscan region of a video display and will not be visible.

The lack of displayed image information during blanking and overscan intervals makes it possible to insert an auxiliary information component, e.g. teletext or closed caption data, into these intervals. Standards such as Federal Communications Commissions (FCC) Regulations define the format for each type of auxiliary information including the positioning of the information within a vertical interval. For example, the present closed captioning standard (see e.g. 47 CFR §§ 15.119 and 73.682) specifies that digital data corresponding to ASCII characters for closed captioning must be in line 21 of field 1. Future modifications to the standard may permit auxiliary information such as closed caption data to be located in other lines, e.g. line 21 of every field.

Auxiliary video information is extracted from the video signal using a decoder. Acceptable performance of the decoder requires reliable identification of the particular lines and fields of the video signal that include auxiliary video data. If video signal strength decreases (e.g. caused by poor reception), the probability of errors in the decoder output increases. For example, detection

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of synchronizing events in a video signal, such as vertical sync pulses, may provide a timing reference point for identifying video lines (e.g. line 21) that may contain auxiliary video information. However, a decrease in video signal strength causes a corresponding decrease in sync signal amplitude. Attempting to decode auxiliary video information from a weak video signal increases the likelihood either that the desired synchronizing pulses may not be detected or that noise pulses may be erroneously interpreted as the desired synchronizing pulses. As a result, a decoder may operate incorrectly in response to a weak video signal.

The error rate of the decoder should remain at an acceptable level as long as the strength of the video signal is sufficient to produce a "viewable" picture. The point at which the error rate becomes unacceptable depends on the content of the auxiliary information. For example, an error rate causing loss of several characters of closed caption text during an interval spanning several minutes may not be objectionable. It is desirable, however, to minimize the error rate over a broad range of video signal strength.

The present invention resides, in part, in recognition of the described problem and, in part, in providing apparatus for solving the problem. In accordance with aspects of the present invention, an auxiliary video information decoder includes means for identifying a desired horizontal line of video in a video signal. The decoder includes means for detecting a reference pulse in a synchronizing signal. First and second window pulse signals are generated at predetermined delay intervals after detection of the reference pulse. Detection of a pulse in the synchronizing signal during at least one of the window pulses indicates occurrence of the desired horizontal line interval.

The invention may be better understood by referring to the drawing in which:

Figure 1 shows a circuit diagram of a portion of a video signal processing system that includes video line detection apparatus according to the present invention; and

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Figures 2 and 3 show signal waveforms useful for understanding the operation of the circuit shown in Figure 1.

In regard to the following detailed description of an embodiment of the invention that is shown in the drawing, it should be remembered that a television system may include features for generating various synchronizing signals. For example, a sync separator may produce sync signals derived from the sync components of the video signal. Deflection circuitry produces repetitive sync signals at regular intervals to define uniform electron beam deflection intervals. The input signals for the circuit in Figure 1 include a separated sync signal CSYNC derived from the video signal, and a flyback pulse VPLS from the vertical deflection circuitry.

Other input signals in Figure 1 include signals 128FH and 2FH which serve as clock signals at frequencies of 128 times the horizontal rate and 2 times the horizontal rate, respectively. For NTSC systems, signals 128FH and 2FH have periods of approximately .5 μs and 32 μs, respectively. Signals 128FH and 2FH may be generated at the outputs of appropriate stages of a counter (not shown in Figure 1). This counter may be part of, for example, a high frequency phase lock loop (PLL) associated with an on-screen display (OSD) feature that may be included in the video system. The PLL is locked to the horizontal deflection pulses and, therefore, indirectly to the horizontal sync component of the video signal. As a result, normal horizontal sync pulses in signal CSYNC line up with every other falling edge of signal 2 FH as shown in Figure 2.

Input signal WR1 in Figure 1 may be generated, for example, by a microcomputer (μC) (not shown in Figure 1) that controls the system. Signal WR1 serves to reset some circuits and load a number (also supplied by the μC) into 5-bit latch 100 at the start of operation. The number stored in latch 100 is related to the TV line to be identified. Changing the number in latch 100 permits changing the line number that will be identified in accordance with the specification for the type of auxiliary information that is being decoded.

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For the exemplary embodiment shown in Figure 1, the relationship between the number loaded in latch 100 and the particular line identified by the system is: L = N - 5, where N is the line to be identified, and L is the number loaded in latch 100. As is discussed further below, the value 5 that is subtracted from N is related to the line number at which the first wide vertical pulse occurs as defined by the particular video signal specification (e.g. line 4 in field 1 for NTSC standard signals as shown in Figure 2). The following description of the operation of the embodiment in Figure 1, and the waveforms in Figures 2 and 3, assumes that the values of N and L are 12 and 7, respectively. Thus, line 12 is being identified and the number 7 is loaded in 5-bit latch 100. As will be apparent from the following description, different values may be used for N and L to permit identifying other line numbers, e.g. line 21 for closed caption data.

The circuit shown in Figure 1 looks for a pulse in signal CSYNC which is wider than 12 μs, i.e. it looks for the first wide vertical sync pulse which is normally 30 μs long (the approximate width of horizontal sync and equalizing pulses is 4 μs and 2 μs respectively). This function is implemented with 4-stage counter 136. Counter 136 is reset every 32 μs by signal RESPWC, a narrow pulse generated at the falling edge of signal 2FH by D-type flip flop (DFF) 128, inverter 130, and NOR gate 132. Counter 136 is clocked by signal CLKPWC at 1 μs intervals whenever signal CSYNC is at logic 1. Signal CLKPWC is generated by toggle flip flop (TFF) 134 having a clock input coupled to signal 128FH and a toggle input (T) coupled to signal CSYNC.

A count of 12 in counter 136 is detected by NAND gate 138 when signal CLKPWC is high. The output of NAND gate 138 is coupled to the clock input of DFF 140. The output of DFF 140 goes to logic 1 in response to counter 136 reaching a count of 12. Signal CLRLC, an inverted version of the output of DFF 140 via inverter 142, is coupled to the reset input of a 6-bit counter comprised of counters 104 and 106. The clock input of counters 104 is coupled to signal 2FH. The most significant output of counter 104 clocks counter 106. The effect of counter 136

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reaching a count of 12 is that the reset signal to counters 104 and 106 is removed enabling counters 104 and 106 to count negative transitions of signal 2 FH after counter 136 reaches a count of 12.

When the count produced by counters 104 and 106 reaches the value stored in latch 100, as determined by comparator 108, 32 μs wide window pulse signal WND1 is generated by DFF 110 in synchronism with positive transitions of signal 2 FH. Another 32 μs wide window pulse on signal WND2 is generated by DFF 112 when the window pulse on signal WND1 terminates.

As shown in Figure 1, the least significant bit of the "A" input to comparator 108 (input from latch 100) is hard-wired to logic 1 (VCC) while the number stored in latch 100 is coupled to the remaining "A" inputs of comparator 108. The effect is that the value at the "A" input of comparator 108 is equal to (2 x L) + 1. This approach is used so that changing the value of L by an integer amount causes the line number being detected to change by the same integer amount. For example, storing 16 rather than 7 in latch 100 will cause line 21 rather than line 12 to be detected.

The value of L is multiplied by 2 in the relationship (2 x L) + 1 because counters 104 and 106 are being clocked at twice the horizontal line rate by signal 2FH. The number 1 is added to (2 x L) because it is desirable to shift the window pulses on signals WND1 and WND2 by one-half of a horizontal line interval (1 cycle of signal 2FH) so that the horizontal sync pulse occurring at the beginning of the desired line will be centered in the window pulse. Thus, for the described exemplary embodiment, comparator 108 will indicate that the output of counters 104 and 106 equals the latch value L, and enable the generation of the window pulses, when the count value at the output of counters 104 and 106 is 15 (i.e. (2 x 7) +1). The value in counters 104 and 106 is indicated on the waveform for signal B0 (the least significant counter output bit) in Figures 2 and 3. The signal timing depicted in Figures 2 and 3 illustrates that the difference between the line number being identified (N) and the value stored in latch 100 (L) is the above-mentioned value 5 for the exemplary

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embodiment shown in Figure 1 operating with NTSC standard signals.

A sync pulse in the signal CSYNC waveform which occurs during one of the two window pulses is the sync pulse that corresponds to the start of the desired TV line (line 12 in the described embodiment) as shown in Figure 2. A sync pulse on signal CSYNC during one of the window pulses is detected via OR gate 114 and NAND gate 118. The output of NAND gate 118 provides a "set" signal at the set input of set-reset latch 120. Signal LINE at the output of latch 120 becomes active (goes to logic 1 in Figures 1 to 3) in response to the set signal to indicate detection of the desired line.

The active state of signal LINE is terminated 64 μs later by signal ENDLINE coupled to the reset input of latch 120 via NOR gate 116. The 64 μs interval is defined by a counter (not shown in Figure 1) that is enabled for counting when the desired horizontal sync pulse occurs as indicated by signal LINE. The counter is clocked by signal 128FH having a period of .5 μs until a count of 128 is produced indicating that a 64 μs period has elapsed. Signal ENDLINE is then generated to terminate signal LINE.

A field identification signal FIELD1 is generated at the output of TFF 152. The rising edge of the vertical deflection pulse on signal VPLS clocks TFF 152 to produce signal FIELD1.

The preceding comments describe the operation of the embodiment shown in Figure 1 under normal conditions, i.e. a strong signal and no noise. In accordance with aspects of the invention, features of the exemplary embodiment shown in Figure 1 operate to ensure reliable operation during weak or noisy signal conditions.

Two lines (equivalent to four half-lines as counted with the 2 FH clock) after the 6-bit counter comprised of counters 104 and 106 is activated by signal CLRLC, the status of the vertical pulse on signal VPLS at the output of inverter 124 is sampled by DFF 126. The two line sampling delay is established by set-reset latch 122. Signal CLRLC at the set input of latch 122 "sets" signal

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SMPLV at the inverted output of latch 122 to logic 0 when signal CLRLC is at logic 1 inactivating counters 104 and 106. Signal B2 from the third least significant output of the 6-bit counter (22 output) is coupled to the reset input of latch 122. Signal B2 goes to logic 1 after four pulses (a two video line interval) occur on signal 2FH. Thus, when signal CLRLC activates counters 104 and 106 by going to logic 0, the set signal to latch 122 is removed enabling a high level on signal B2 (after a two video line interval) to reset latch 122 causing signal SMPLV to go to logic 1. The transition of signal SMPLV from logic 0 to logic 1 after two line intervals clocks DFF 126 sampling signal VPLS.

If the vertical pulse is absent, signal NOVP at the output of DFF 126 becomes a logic 1. Absence of the vertical pulse on signal VPLS when the sampling operation occurs indicates that the wide pulse detected by counter 136 and NAND gate 138 is a noise pulse. A logic 1 on signal NOVP resets DFF 140 via NOR gate 144 causing signal CLRLC go to logic 1. As a result, counters 104 and 106 are cleared preventing the generation of window pulses on signals WND1 and WND2.

The described feature prevents a wide noise pulse in signal CSYNC that is not in the immediate vicinity of the the normal vertical sync pulses from erroneously generating the LINE signal. As an example, Figure 3 illustrates the operation when an 18 μs wide noise pulse occurs between the first two pre-equalizing pulses in signal CSYNC. The operation of the noise detection feature is relatively independent of the phase and width of the vertical pulse on signal VPLS. The desired noise pulse detection operation occurs as long as the vertical pulse on signal VPLS does not start more than two lines after the first vertical sync pulse on signal CSYNC, and is at least two lines wide.

Values other than the above-described two line (four half line) period may be used for the delay between detection of a wide pulse (wider than 12 μs) on signal CSYNC and testing for the presence of the vertical pulse on signal VPLS. Different video systems may exhibit timing relationships between signals CSYNC and VPLS that differ from the relationship shown in Figures 2 and

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3. For example, in certain video systems the vertical pulse on signal VPLS from deflection circuitry may begin during line 5 rather than line 4 as indicated in Figure 2. Testing for the presence of a vertical sync pulse on signal VPLS during line 4 (a 2 line delay) when a vertical sync pulse does not begin until line 5 will cause detection of the first wide vertical pulse on signal CSYNC to be erroneously interpreted as detection of a noise pulse. Changing the delay to a 3-line delay would eliminate this problem. Thus, the operation of the described embodiment may be adapted to the requirements of various video systems.

In a noise-free environment, the desired horizontal sync pulse in signal CSYNC will always occur in the middle of the window pulse on signal WND1 in field 1, and in the middle of the window pulse on signal WND2 in field 2 as shown in Figures 2 and 3, respectively. This characteristic could be used for field identification, but the result may not be correct under weak signal conditions if one or more pulses occur in both adjacent windows. The circuit in Figure 1 solves this problem by using the very reliable and noise-free vertical deflection pulse on signal VPLS to toggle TFF 152 to produce signal FIELD1.

To ensure that signal FIELD1 has the correct phase, signal FIELD1 is forced into the correct state by resetting the toggle flip-flop whenever the correct sequence of events for field 2 has been detected. This corresponds to a pulse in signal CSYNC not occurring in the window pulse on signal WND1, but being present in the immediately following window pulse on signal WND2. Detection of the sequence of events indicating field 2 is provided by NAND gates 146 and 150, and DFF 148. Operation of the described feature is illustrated in Figure 3 where the wrong polarity of signal FIELD1 has been assumed at the start.

As described above, the active state of signal LINE is terminated by signal ENDLINE. Signal LINE could be terminated by the pulse in signal CSYNC which immediately follows the pulse on signal CSYNC that occurs during the window pulse on signal WND1 or WND2. However, noise on signal CSYNC might cause premature termination of signal LINE. Thus, signal ENDLINE is

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reliably generated regardless of the presence of noise as previously described.

Another feature that improves noise immunity involves using signal 2 FH rather than signal CSYNC as the clock for the line counter. Signal 2FH is the output of a counter stage in a PLL and is, therefore, relatively stable. Signal CSYNC is derived from the video signal and may exhibit noise pulses corresponding to noise in the video signal.

It should be noted that any given number loaded into the 5-bit latch will result in signal LINE becoming active for the corresponding line during field 1 as well as during field 2. It may be necessary, therefore, to interrogate the status of signal FIELD1 to determine whether the signal LINE is in the desired field. For example, present closed caption standards limit closed caption information to line 21 of field 1. This may be accomplished by having a μC that is controlling the system test the state of signal FIELD1 when signal LINE is active. Alternatively, hardwired logic could be used to condition signal LINE with signal FIELD1.

Another feature of the disclosed arrangement is that the 32 μs width of the window pulses on signals WND1 and WND2 permits a phase error approaching +/-16 μs between the horizontal sync pulses on signal CSYNC and every other falling edge of 2 FH. This is an important feature because relatively large phase errors may occur. For example, in the case of a video cassette recorder (VCR) having mechanical misadjustments in the tape reading mechanism, the video line just before the start of the vertical blanking period where the read heads are switched is stretched (or less commonly compressed) and has a period substantially different from 64 μs. The speed of the horizontal PLL may be too slow to correct this error by the time the first wide vertical sync pulse occurs on signal CSYNC. The resulting phase error may have a magnitude approaching 16 μs. The phase error tolerance of the disclosed arrangement permits accurate decoding of auxiliary information to occur despite the existence of phase error.

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CLAIMS

1. Apparatus for detecting the beginning of a particular horizontal line interval within a particular vertical field interval in a video signal, said video signal having an image synchronizing component comprising a plurality of vertical pulses indicating occurrence of said vertical field intervals and a plurality of horizontal pulses indicating occurrence of respective ones of a plurality of horizontal line intervals included in each of said vertical field intervals, said apparatus comprising:

means responsive to said image synchronizing component for detecting occurrence of said vertical pulses;

means responsive to an input reference signal at a predetermined frequency for establishing a first delay with respect to occurrence of said vertical pulses, said first delay being related to a number of said horizontal intervals expected to occur between said vertical pulse in said particular vertical field interval and said particular one of said horizontal intervals;

means coupled to said detecting means and to said delay means for generating a first timing pulse said first delay after occurrence of said vertical pulse, and for generating a second timing pulse delayed a second delay with respect to said first timing pulse, said second delay being related to the duration of said horizontal line interval; and

means responsive to said first and second timing pulses and to said video signal for detecting occurrence of one of said horizontal pulses during said first or said second timing pulses.

2. The apparatus of claim 1 wherein said detecting means detecting a horizontal pulse during a predetermined one of said first and second timing pulses but not during the other one of said first and second timing pulses indicates occurrence of said particular vertical field interval.

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3. The apparatus of claim 1 wherein said first and second timing pulses exhibit a duration related to the duration of said horizontal line interval such that said predetermined relationship substantially decreases a sensitivity of said detecting means to timing variations in the occurrence of said vertical pulses.

4. The apparatus of claim 3 wherein said duration of each of said first and second timing pulses is substantially one-half of one of said horizontal line intervals.

5. The apparatus of claim 1 wherein said means for detecting said vertical pulses includes a counter for counting cycles of an input clock signal at a frequency substantially greater than the frequency of occurrence of said horizontal line intervals;

said counter being enabled to count in response to a pulse in said video signal occurring during an interval when said reference pulse is expected to occur; and

said counter producing a count representative of the duration of said counter enabling pulse.

6. The apparatus of claim 1 wherein said means for detecting said vertical pulses comprises:

first means for detecting a wide pulse in said image synchronizing component, said wide pulse having a duration substantially longer than one of said horizontal pulses; and

second means for detecting a pulse occurring in a deflection synchronizing signal a predetermined delay after detection of said wide pulse, said predetermined delay being related to the duration of said horizontal line intervals.

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7. The apparatus of claim 5 wherein

said predetermined frequency of said input reference signal is two times the frequency of occurrence of said horizontal line intervals;

said frequency of said input clock signal is 128 times the frequency of occurrence of said horizontal line intervals; and

said input reference signal and said input clock signal exhibit substantially stable frequency characteristics.

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