

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
11 May 2006 (11.05.2006)

(10) International Publication Number
WO 2006/049834 A1

(51) International Patent Classification:

H01L 21/8238 (2006.01) *H01L 21/265* (2006.01)
H01L 21/336 (2006.01)

[DE/DE]; Berggartenstrasse 38, 01277 Dresden (DE).
BUCHHOLTZ, Wolfgang [DE/DE]; Am Bomberge 8,
 01445 Radebeul (DE).

(21) International Application Number:

PCT/US2005/036779

(74) **Agent: DRAKE, Paul, S.;** Advanced Micro Devices, Inc., 5204 East Ben White Boulevard, Mait Stop 562, Austin, TX 78741 (US).

(22) International Filing Date: 12 October 2005 (12.10.2005)

(25) **Filing Language:** English

(26) **Publication Language:** English

(30) Priority Data:

10 2004 052 617.6	29 October 2004 (29.10.2004)	DE
11/145,697	6 June 2005 (06.06.2005)	US

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

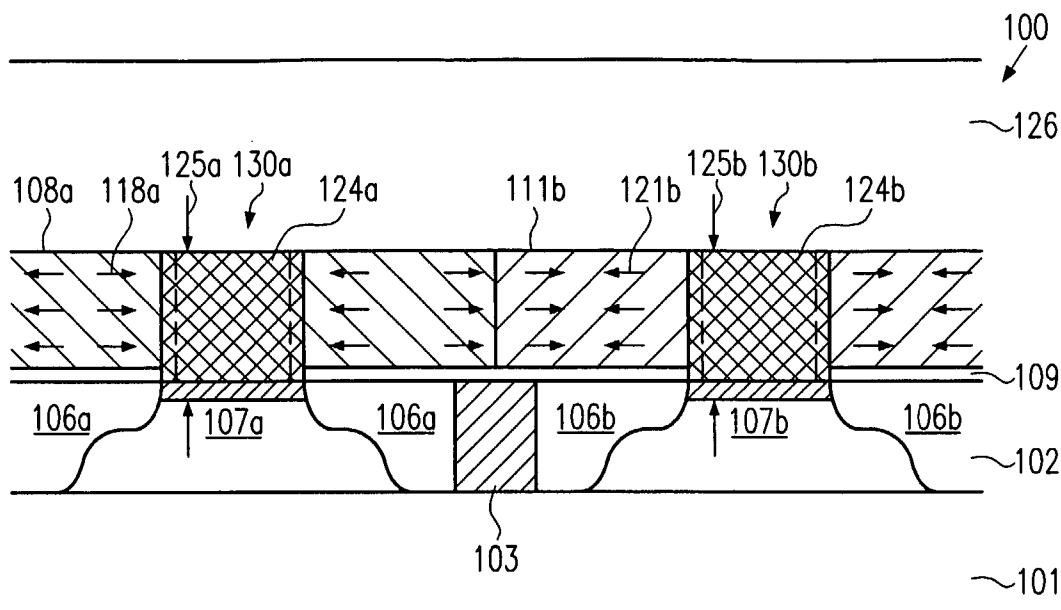
(71) **Applicant** (for all designated States except US): **ADVANCED MICRO DEVICES, INC.** [US/US]; One AMD Place, Mail Stop 68 P.O.Box 3453, Sunnyvale, CA 94088-3453 (US).

(72) Inventors; and

(75) **Inventors/Applicants (for US only): HORSTMANN, Manfred** [DE/DE]; Aussere Parkstrasse 25, 01833 Duerroehrsdorf-Dittersbach (DE). **PRUEFER, Ekkehard**

[Continued on next page]

(54) Title: A SEMICONDUCTOR DEVICE INCLUDING SEMICONDUCTOR REGIONS HAVING DIFFERENTLY STRAINED CHANNEL REGIONS AND A METHOD OF MANUFACTURING THE SAME



(S7) Abstract: By locally modifying the intrinsic stress of a dielectric layer laterally enclosing gate electrode structures of a transistor configuration formed in accordance with in-laid gate techniques, the charge carrier mobility of different transistor elements may individually be adjusted. In particular, in in-laid gate structure transistor architecture, NMOS transistors and PMOS transistors may receive a tensile and a compressive stress, respectively.

WO 2006/049834 A1



Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.